A DLL Based Clock Synthesizer with Locking Status Indicator

Young-Soo Ryu, Young-Shig Choi, *Member, KIMICS*

Abstract—In this paper, a new programmable DLL (delay locked loop) based clock synthesizer is proposed. DLL has several inherent advantages, such as no phase accumulation error, fast locking and easy integration of the loop filter. This paper proposes a new programmable DLL that includes a PFD(phase frequency detector), a LSI(lock status indicator), and a VCDL(voltage controlled delay line) to generate multiple clocks. It can generate clocks from 3 to 9 times of input clock with 2μs locking time. The proposed DLL operating in the frequency range of 300MHZ–900MHz is verified by the HSPICE simulation with a 0.35μm CMOS process.

Index Terms—DLL, clock synthesizer, frequency multiplication, VCDL.

I. INTRODUCTION

As the speed performance of VLSI systems increases, more emphasis is placed on the high-speed clock synthesizer. High-performance system such as CPU and DSP requires high-speed clocks to transfer data between blocks. Therefore, a system block that can generate high-speed on-chip clocks from the outside clocks is required. Generally, PLL (phase locked loop) is widely used for clock generation [1]-[4]. However, it is not easy to design because the PLL is a higher order closed-loop feedback structure. The loop bandwidth is easily influenced by the PVT (process, voltage, temperature) fluctuations. It can cause instability in PLL operation. Moreover, it has disadvantages such as being late for a locking time and phase accumulation error due to closed-loop feedback VCO (voltage controlled oscillator). On the other hands, the DLL using the VCDL instead of VCO is a first order system, and then always stable.

It also has several other advantages such as no phase accumulation error, easy integration of loop filter and fast locking time. Thus, DLL based clock synthesizer has been studied to overcome the difficulty of generating various clocks while keeping its inherent characteristics. In this paper, a new architecture DLL is proposed to be used as a clock synthesizer.

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II. CONVENTIONAL DLL BASED CLOCK SYNTHESIZER

A conventional DLL used as a local oscillator for PCS (personal communications service) applications has used an edge combiner for the frequency multiplication [5]. However, it requires a LC tank at the output to enhance the load impedance at the resonant frequency, which consumes a large chip area. Also, a low-Q inductor for low close in-phase noise draws a large tail current to achieve the required output swing.

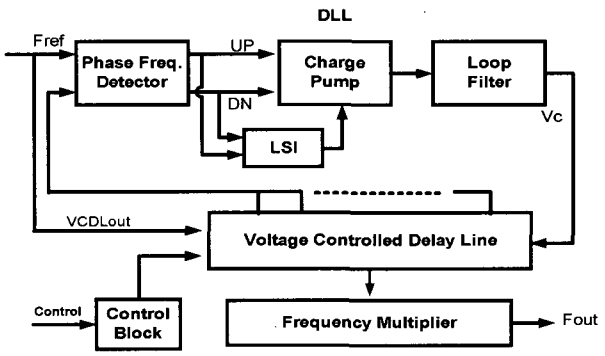


Fig. 1 Block diagram of proposed DLL based frequency synthesizer

Another drawback is that the frequency multiplication ratio is fixed once the LC tank component values are chosen. In other word, frequency tuning range is very narrow. Self-correcting DLL based clock synthesizer used AND-OR gates for the frequency multiplication [6]. The self-correction solves a fail locking problem such as 'stuck' and 'harmonic lock'. And also it has advantages such as a generation of multi-phase clocks and the fast locking. However, it requires 50% duty ratio of the input clock because it synthesizes clocks using signals generated by each delay cell for the required clock synthesis. It can generate only the multiples of three. Another DLL based clock synthesizer extracts rising edges of each delay cell and generates multiple clocks [7]. It has an advantage that the duty ratio of input clock should not be 50%. In this architecture, only one fixed multiple clocks can be generated if the number of delay cell is chosen.

III. DLL ARCHITECTURE

As shown in Fig. 1, the proposed DLL comprises of a PFD (phase frequency detector), a CP (charge pump), a lock state indicator (LSI), a loop filter (LF), a VCDL and a frequency multiplier. The PFD compares an external

reference clock and VCO output clock and it produces two digital signals (UP and DN) whose width is determined depending on the frequency and phase of the two signals. The CP converters the PFD output signal into a current that is fed into the LF determining the output LF voltage, Vc. Vc, a control voltage of VCDL, which is connected to each delay cell, controls the delay time of the delay cells. There is no jitter accumulation in DLL contrary to PLL because the input signal of DLL is used as the input signal to the VCDL. The delay range of VCDL caused by Vc can also be widened according to external control signals.

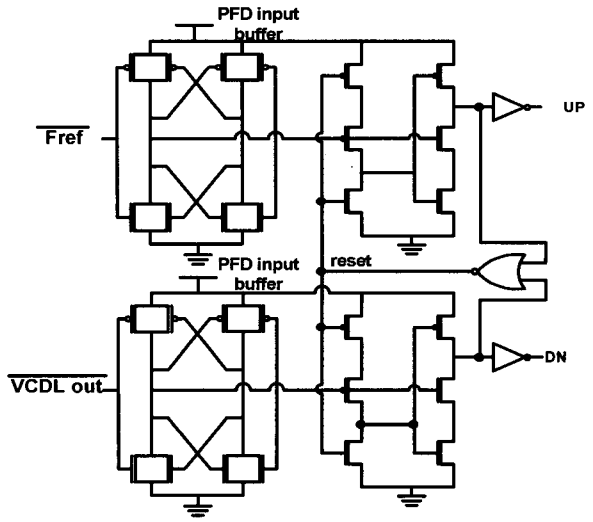


Fig. 2 Schematic of proposed PFD with input buffers

Finally, the frequency multiplier block produces the wanted clock with the signals from VCDL. Multiple clocks can be determined by Vc with the external control signal.

A. PFD with Input Buffers

It is important to lock the signal within one period of VCDL to generate multiple clocks in the proposed DLL based clock synthesizer. The PFD shown in Fig. 2 satisfy the previous condition. The proposed PFD has operation range of of $(-2\pi \sim +2\pi)$ wider than other phase detectors of $(-\pi \sim +\pi)$ in order to solve fail locking problem. The VCDL is very sensitive to capacitance existed in circuit because it controls the delay time of signals. To prevent from happening of unwanted delay in VCDL, the sum of capacitance at the input of next delay cell should be same. When the final output of VCDL is connected to the PFD, the sum of capacitance including the input capacitance of next delay cell and the input capacitance of the PFD is becoming larger. Hence, the delay time of last stage in VCDL is longer than that of previous stages.

This phenomenon continuously generates jitters at output of clock synthesizer. To solve the problem, the same buffer used in VCDL is added to the input of D F/F as shown in Fig. 2. The same buffer is also added to the input of other D F/F to make the same condition for the two signals, Fref and VCDL output. The buffer is made of the latch in Fig. 3(b). This scheme makes the capacitance equal at each delay cell in VCDL.

B. LSI for fast locking and low jitter characteristic

Locking Status Indicator consists of a NOR gate and a capacitor, an inverter and Schmitt triggers, as shown in Fig. 3 The NOR gate is used to combine the phase difference of both two signals (UP, DN). Cload's voltage, Va, is determined by current that flowing through transistors, MP1 and MN1. The Schmitt trigger generates signal S according to Va. When DLL is out-of lock, phase and frequency difference of two input signals of PFD is large. The output of NOR gate has longer "Low" signal than "High" signal. The output signal turns PMOS on longer than turns NMOS on. It increases the voltage of capacitance. When DLL is in-lock, on the contrary, it decreases Va. During the transition, Va fluctuates due to the irregular pulse period of the NOR gate output. The transistors charge and discharge the capacitance in random pattern. With Schmitt trigger, the robust signal, S, from LSI can be obtained. The signal S changes the current in CP according to the operating status. When DLL is out-of lock, the current in CP increases and fast locking achieves. When PLL is in-lock, the current in CP decreases and low jitter output signal obtains. In other words, loop bandwidth is changed according to the operating status.

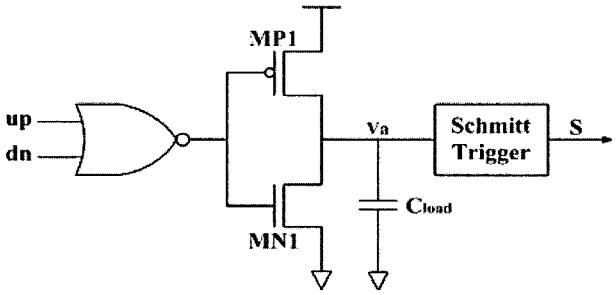
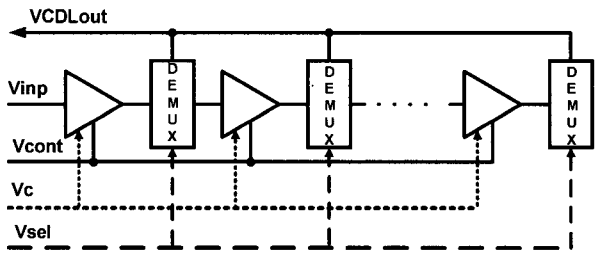


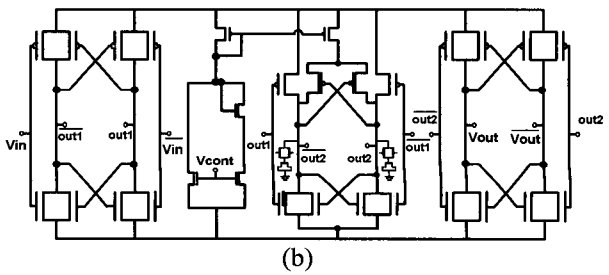
Fig. 3 Schematic diagram of LSI

C. Proposed VCDL with Variable Delay Range

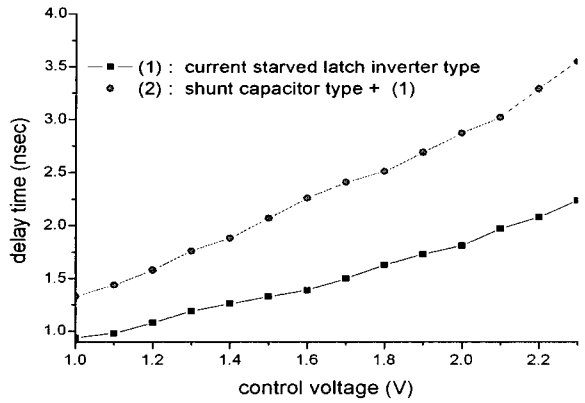
The schematic diagram of the VCDL with three features is shown in Fig. 4(a).



(a)



(b)



(c)

Fig. 4 Schematic diagram of (a) VCDL (b) the delay cell, and (c) Delay time vs control voltage

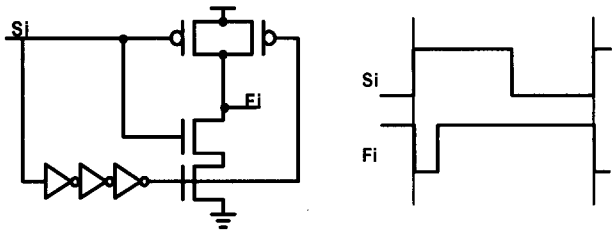
First, the desired number of delay cell can be chosen for the wanted clock. A DEMUX between delay cells receives the external control signal and chooses the number of the delay cell. This chosen number of delay cell becomes the desired multiplication ratios of frequency synthesis.

In order words, N delay cells should be chosen so as to generate the clock that is N multiples of the input frequency, Fref. The input signal Fref of VCDL exactly goes through N delay cells in one period. If the period of Fref is T, the delay of each delay cell is T/N when the DLL is in-lock. Thus, there are clock edges at each T/N point. Consequently, the edge detector will produce signals at every clock edges and those signals will be combined to generate N multiples of Fref. Second, it can control the delay range widely by appropriately using current starved latch inverter type delay cell and shunt capacitor type delay cell appropriately as shown in Fig. 4(b) [8].

Current starved inverter type delay cell have a good linearity characteristic by using voltage controlled resistor (VCR). As shown in Fig. 4(b), Shunt capacitor type delay cell used two MOS capacitors which are connected through the switches to the delay cells. The ON/OFF of the switches is controlled by the external control signals. These capacitors make VCDL having a wider delay range. Furthermore, the operating range of the Vc can be chosen to the range of CP output voltage that shows no current mismatch in CP and linear delay range of VCDL. Fig. 4(c) shows the delay time to the control voltage Vc. Third, the proposed delay cell uses a latch inverter to prevent the distortion of the waveform that can be caused when shunt capacitor type delay cell is used. This fact contributes to the linear delay operation of VCDL to Vc as shown in Fig. 4(c).

D. Frequency Multiplier with Edge Detector

The frequency multiplier comprises an edge detector and a logic circuit. The schematic of the edge detector is shown in Fig. 5(a). The edge detector makes one pulse signal by sensing the rising edge of the clock signal that is received from each delay cell of VCDL. It does not require 50% of the duty ratio of input signal Fref. As shown in Fig. 6, pulses generated in the edge detector are synthesized in the frequency multiplier to make one signal. Because the VCDL is exactly locked in one cycle, the final clock cycle of the frequency multiplier is T/N. If the input frequency is f, the output frequency of the DLL with N selected delay cells becomes Nf. The duty ratio may not be 50% but a duty ratio corrector to the output of the frequency multiplier can improve the duty ratio.



(a) (b)

Fig. 5 (a) Schematic of edge detector
(b) Waveforms of edge detector.

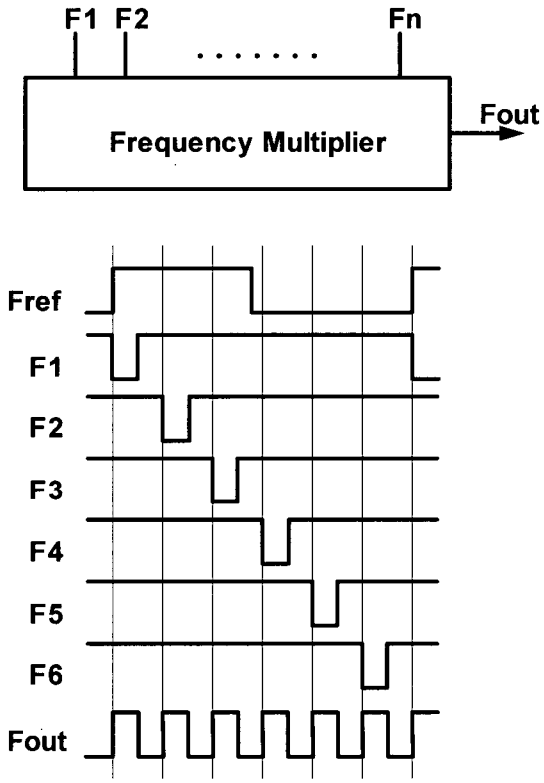


Fig. 6 Example of operation Fout the frequency multiplier

IV. SIMULATION RESULTS

To verify the proposed DLL based clock synthesizer, HSPICE simulation has been used with a 0.35μm CMOS. Fig. 7 shows the simulation results when the input frequency is 100MHz. Fig. 7(a) shows the simulation results of VCDL input voltage according to selection of the number of delay cell. The DLL based clock synthesizer demonstrates fast locking compared to the conventional PLL, approximately less than 2μs. Fig. 7(b) show the simulation results of 300MHz and 900MHz clock signals, respectively.

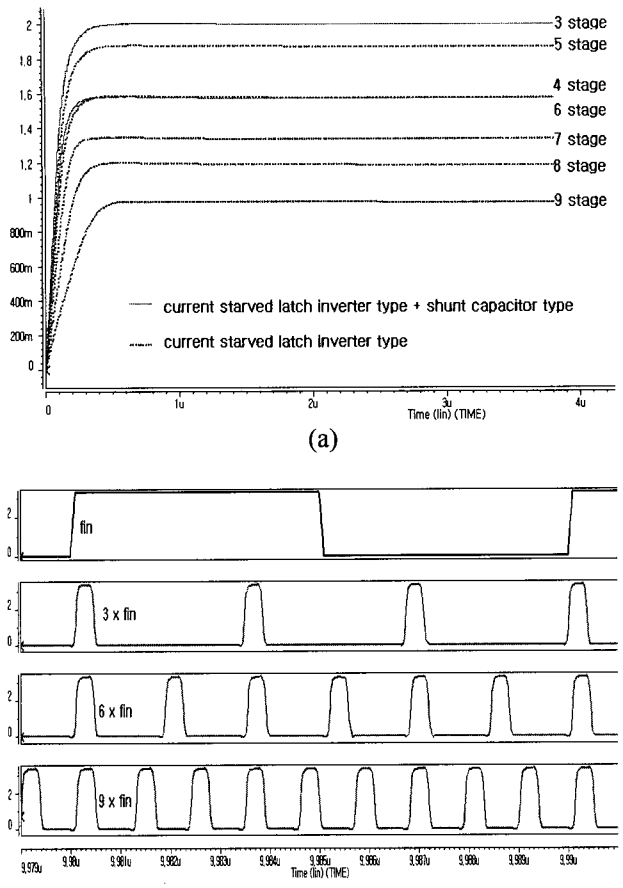


Fig. 7 Simulation waveforms of (a) locking time of the proposed DLL (b) 300MHz, 600MHz, 900MHz output clock.

V. CONCLUSIONS

The proposed DLL based clock synthesizer can generate multiple clocks like PLL. The locking time is less than 2μs. The VCDL has very large delay range by using current starved latch inverter type delay cell and shunt capacitor type delay cell. In the proposed DLL based clock synthesizer, the output clocks from 300MHz to 900Hz with 100MHz input signal can be generated. The inherent characteristics of DLL with LSI make the DLL based clock synthesizer having low jitter output signal and fast locking. This DLL based clock synthesizer has already achieved fast locking and low jitter characteristics with multiple clocks. Therefore, it can be easily modified to satisfy the specs what applications require without trading off locking time and low jitter characteristics because LSI changes the CP current depending on operating status.

REFERENCES

[1] K. Kurita, T. Hotta, and N. Kitamura, "PLL-based BiCMOS on-chip clock generator for very high-speed microprocessor", IEEE J. Solid State Circuits, vol. 26, pp. 585-589, APR. 1991.

[2] I. W. Young, J. K. Greason, and K. L. Wong, "A PLL clock generator with 5 to 110MHz of lock range for microprocessor"s, IEEE J. Solid State Circuits, vol. 34, pp.1599-1607, NOV. 1992.

[3] J. Alvarez, H. Sanchez, G. Gerosa, and R. Countryman, "A wide band width low voltage PLL for power PC microprocessors", IEEE J. Solid State Circuits, vol. 30, pp. 383-391, APR. 1995.

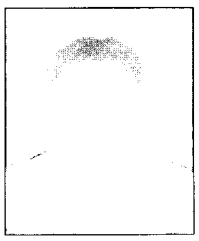
[4] V. R. von Kaenel, "A high speed, low power clock generator for a microprocessor application", IEEE J. Solid State Circuits, vol. 33, pp. 1634-1639, NOV. 1998.

[5] George Chien, Paul R. Gray, "A 900-MHz local oscillator using a DLL_based frequency multiplier technique for PCS applications", IEEE J. Solid State Circuits, vol. 35, pp. 1996-1999, DEC. 2000.

[6] David J. Foley, Michael P. Flynn, "CMOS DLL_based 2V 3.2ps jitter 1GHz clock synthesizer and temperature compensated tunable oscillator", IEEE J. Solid State Circuits, vol. 36, pp. 417-423, MARCH 2001.

[7] Chulwoo Kim, In-Chul Hwang, and Sung-Mo Kang, "A low power small area ±7.23ps jitter 1GHz DLL_based clock generator ", IEEE J. Solid State Circuits, vol.37, pp.1414-1420, NOV. 2002.

[8] Guang-Kaai Edhng, Jyh-Woei Lin, Shen-Iuan Liu, "A Fast-Lock Mixed-Mode DLL Using a 2-b SAR Algorithm", IEEE J. Solid State Circuits, vol. 36, pp. 1464-1471, OCT. 2001.



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