Effect of Soft Error Rate on SRAM with Metal Plate Capacitance

Do-Woo Kim†, Myeong-Kook Gong* and Jin-Suk Wang**

Abstract - We compared and analyzed ASER (Accelerated Soft Error Rate) for cell structures and metal plate capacitance in the fabricated 16M SRAM. Application of the BNW (Buried NWELL) lowered the ASER value compared to the normal well structure. By applying the metal plate capacitor with the BNW, the lowest ASER value can be obtained. The thinner oxide thickness of the metal plate capacitor provides higher capacitance and lower ASER value. The ASER is improved from 2200 FIT to 1000 FIT after sole application of the BNW. However, it is dramatically improved to 15 FIT once the metal plate capacitor is additionally applied.

Keywords: FIT, Metal Plate Capacitance, Soft Error Rate, SRAM

1. Introduction

With the advancement of semiconductor memory technology, the SER (Soft Error Rate) has become a focal point [1-3] due to the increase in density and decrease in operation voltage. As memory density increases, cell capacitance is naturally lowered due to the decreasing size of the capacitive elements. Static random access memory (SRAM) cells have tended to allow cell capacitance to drop as the density has increased. ASER measurements have been correlated in the storage node capacitance of cells and the various well structures [4-6].

Soft error is a memory cell failure occurred when the cell is written or read without physical defects, and it shows the random bit failure mode in the memory fail bit map. The main cause of soft error is the energetic α-particles radiated from the uranium, thorium and americium, etc. The charges that are produced by the electron-hole-pair (EHP) generated during the penetration of the alpha-particles through the semiconductor near the memory cell induce charge up-set. As such, the memory data are changed.

If an α- particle is incident on a silicon chip, the energy of the α- particle becomes partly lost when passing through dielectric layers, and about 10^6 of EHP's are generated with the alpha-particle passing through about 25μm with an energy of about 4MeV. This number of charges is enough to induce soft errors. There are numerous efforts that can be made to suppress ASER, such as, raising cell capacitance, introducing the third well as a diffusion and funneling barrier, or coating the polyimide as a protection layer [7, 8].

In this paper, the metal plate capacitor is proposed to raise the cell node capacitance, thereby reducing soft error rate on 16M SRAM. ASER is measured in this 16M SRAM with the metal plate and compared to with and without BNW.

2. Experimental

Fabricated 16M full CMOS SRAM is used to measure ASER. The radioactive material is Am241, and the α-particle flux is 1.35×10^5 particles/cm^2·min. A memory tester, Mosaid3480, measures the error rate. The voltage applied is 2.4 V and the type of test function is checkerboard, the sequence of operation is forward written and read and inverse write and read [9]. The operations are repeated enough to count the exact errors. The distance of the alpha source and the DUT (device under test) is 7 mm. The measurement configuration is shown in Fig. 1. The α-particle flux of EMC is presumed as 0.005 particles/ cm^2·hrs. Thus the ASER in the FIT (Failure in time) is calculated as follows.

In this experiment two well structures are considered, the normal double well structure and the triple well struc-

$$FIT = \frac{0.005\ \text{particles/cm}^2\text{.hrs} * \text{errors/min} * 10^9\ \text{hrs}}{1.3 * 10^5\ \text{particles/cm}^2\ .\ \text{min}}$$

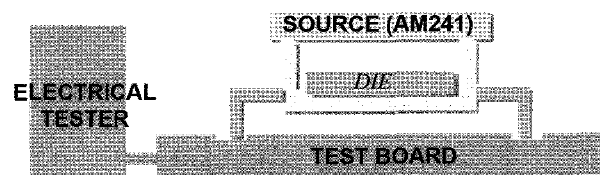

Fig. 1 Schematic diagram of electrical tester

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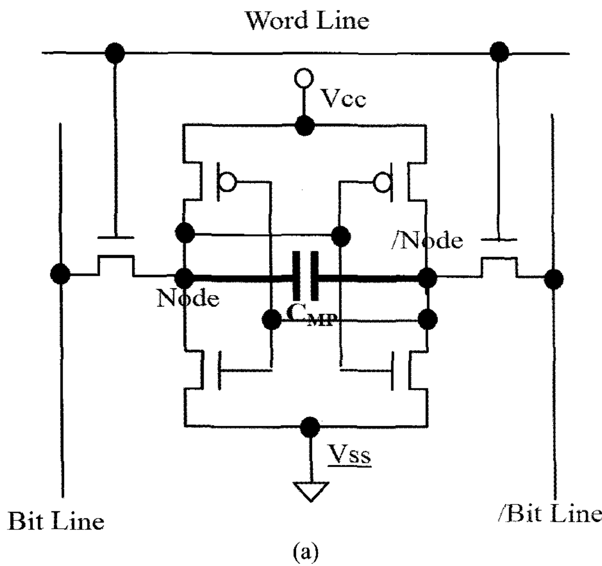
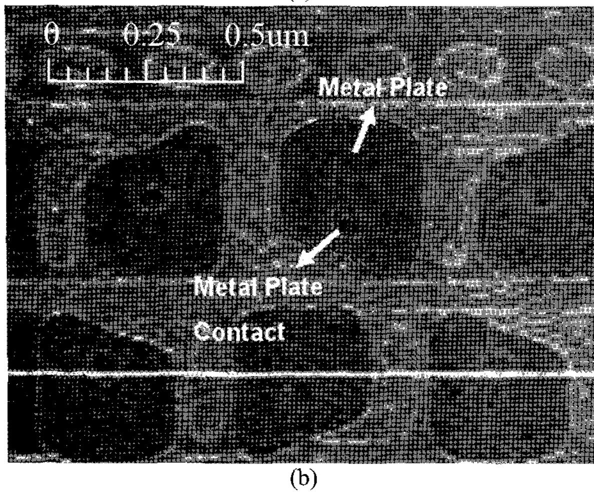
ture (buried N-well under the double well). And two cell structures are studied, the normal full CMOS SRAM and node capacitor increased SRAM, which in this paper is called the metal plate capacitor. The metal plate capacitor consists of only one contact on the one node local interconnection and the barrier metal Ti/TiN plate. The local interconnection is fabricated by the tungsten damascene process. The coupling capacitance is formed by simply overlapping the Ti/TiN metal plate with the W local interconnection. The thickness of the isolation oxide is controlled to meet the designed capacitance for the accelerated soft error rate specification.

Fig. 2 presents the SRAM cell circuit with the metal plate capacitance and the plane view of the metal plate capacitor.

The metal plate capacitor processes are applied after the metal process in which the transistors are already formed. The process sequence of 16M SRAM is shown in Fig. 3.



(a)



(b)

Fig. 2 SRAM cell with metal plate capacitor. (a) SRAM cell circuit and (b) SEM image showing metal plate capacitor

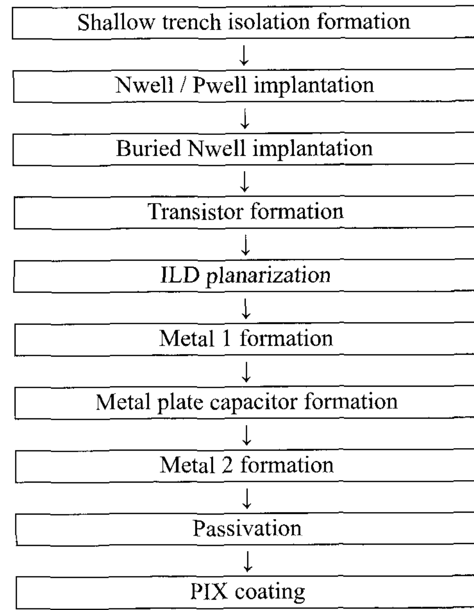


Fig. 3 Process flow sequence

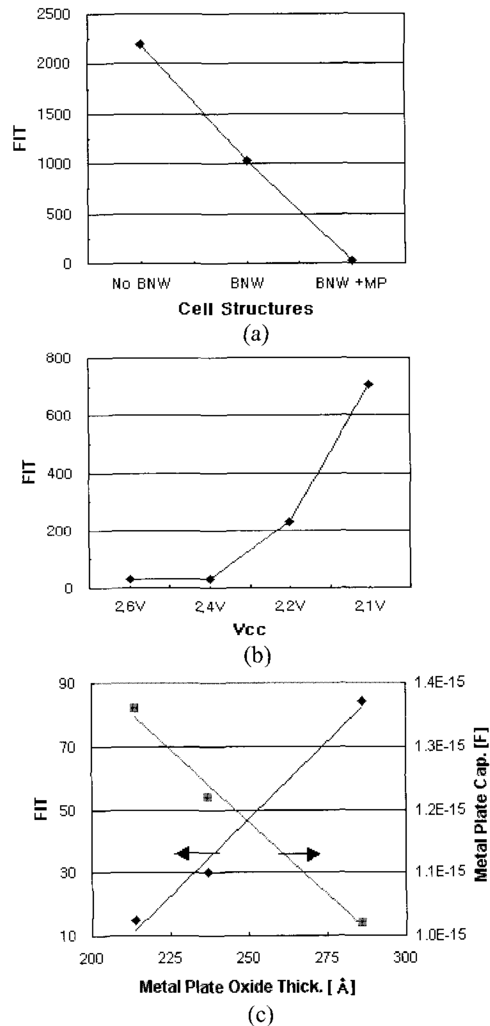


Fig. 4 Soft error rate according to (a) cell structures, (b) Vcc and (c) metal plate capacitance and metal plate oxide thickness

3. Results

Fig. 4(a) indicates the ASER values according to each cell structure. Without the BNW, the ASER is 2200 FIT. And with BNW applied in the cellblock, it is 1000 FIT. But the level is insufficient to meet the reliability specification in this 16M SRAM technology. If the metal plate (MP) is formed as mentioned in the previous paragraph with the BNW, the ASER is 15 FIT, which is almost two orders lower than the normal well structure.

In Fig. 4(b) Vcc dependence of the measured ASER is shown for the SRAM only with the metal plate capacitor. As Vcc lowers, the ASER exponentially increases such as 30 FIT on 2.6V and 700 FIT on 2.1 FIT.

In Fig. 4(c) the ASER is shown for the metal plate capacitance and the metal plate oxide thickness. The thickness of the isolation oxide is controlled by the RF etch before deposition of the barrier metal. The controlled thickness range is 200 through 300Å. The metal plate capacitance per unit cell is calculated by the value measured from the array of 0.5μmX 40μm metal plate test pattern on the local interconnection in the cell array. The capacitance range of the metal plate with the isolation thickness is 1.0 to 1.4 fF per unit cell. The capacitance is increasing while the thickness is decreasing. The lowest ASER value shown is 15 FIT when the isolation oxide thickness is 210Å.

4. Conclusion

The metal plate capacitor and BNW are applied on 16M SRAM. The capacitance and the ASER are measured according to the isolation oxide thickness. When the BNW is applied, the ASER is lowered to approximately 1 order of magnitude under the normal well structure. The metal plate capacitor also lowered the ASER to about 1 order of magnitude. Vcc dependence of the ASER for the SRAM with the metal plate capacitor and BNW shows exponential dependence as usual. The capacitance of the metal plate capacitor increases with the isolation oxide thickness. ASER of 15 FIT is obtained for the 210 Å, which is of very low level to meet the specification of 1000 FIT.

In this paper an effective and easy process for SRAM is proposed and a substantially low ASER value is obtained.

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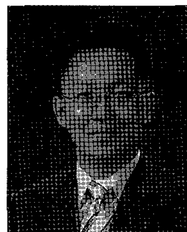

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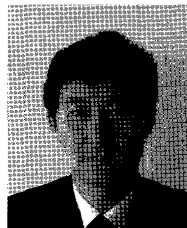

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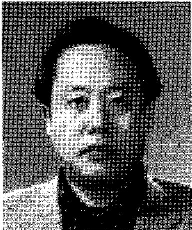

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He was born in Korea on June 23, 1945. He received his B.S., M.S., and Ph.D. degrees all in Electrical Engin-eering from Yonsei University, Seoul, Korea, in 1971, 1974, and 1981, res-pectively. In the Department of Engin-eering Science and Mechanics at Pennsylvania State University, University Park, PA, he worked as a Post-doctoral Fellow in passivation of dry etching damage using low energy hydrogen implants from 1982 to 1983. He joined the faculty at Chungna\m National University, Korea in 1975, where he served as Director of the Computer Center from 1979 to 1980 and is currently a Professor of Electrical and Computer Engineering. He spent his sabbatical leave as a Visiting Scientist at the Department of Engineering Science, Pennsylvania State University, PA in 2003 and 2004. His research interests lie in the general area of solid-state electronics, including semiconductor devices, materials, integrated circuits, photovoltaics, sensors, thin films and radiation effects. Dr. Wang is a member of the American Vacuum Society and the Institute of Electronics Engineers of Korea.