Gate Length Optimization for Minimum Forward Voltage Drop of IGBTs

Jin-Woo Moon†, Dong-Wook Park*, Yearn-Ik Choi and Sang-Koo Chung*****

Abstract - The forward voltage drop of IGBT is studied numerically and analytically as a function of gate length. An analytical expression is presented for the first time for the surface potential variation along the channel layer under the gate of IGBT. The surface potential drop and the carrier density near the surface allow calculation of the forward voltage drop of IGBT analytically as a function of the gate length. The voltage-drop in the drift region near the gate decreases exponentially, whereas that on the surface increases linearly with increasing the gate length, the sum of which exhibits an optimum gate length, resulting in a minimum forward voltage drop. Based on the surface potential drop, a remodelling of the forward voltage drop of IGBT is also proposed.

Keywords: IGBT, Surface Potential, Forward Voltage Drop

1. Introduction

Optimization of the gate length of IGBT is indispensable for improvement of both the trade-off characteristics and the high electrical withstand capability. In conventional IGBT, the forward voltage drop of $V_{ce,sat}$ measured usually at the total current density, $J=100[A/cm^2]$ has been known to be the sum of the voltage drops on four different regions; namely V_{ch} on the channel region, V_{acc} on the accumulation region, V_{epi} on the drift region, and V_j on the N-epi/p+ anode junction[1]. However, justification of V_{ch} and V_{acc} as the voltage drop terms for $V_{ce,sat}$ is questionable as will be shown shortly. A remodelling of $V_{ce,sat}$ is proposed. The relationship between the gate length and the forward voltage drop has been investigated experimentally[2]. The results show existence of an optimum gate length for a minimum forward voltage drop. No analytical approach for an optimum gate length has yet, however, been reported.

The aim of this paper is to present an analytical model for gate length dependence of the forward voltage drop of IGBT. Increase of the gate length increases the surface potential drop along the channel layer and enhances carrier accumulation underneath the poly-Si gate electrode, reducing the forward voltage drop in the drift region near the gate electrode. An exponential decay of the lateral surface field along the channel layer is presented to account for the simulation results. The attenuation constant of the surface field is found to be independent of applied gate voltage. Determination of an optimum gate length is followed which allows the minimum forward voltage drop for an IGBT. The two-dimensional simulations are carried out using ATLAS. The analytical results are compared with those from the simulations. Physical principles involved in the present analysis can be applied to all types of IGBT structure.

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2. Simulation Results

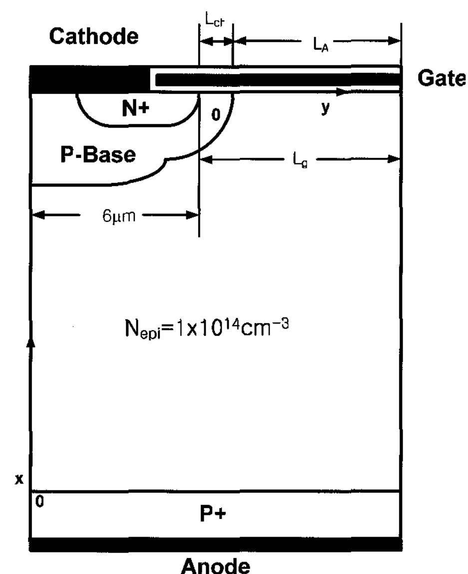


Fig. 1 Cross-section view of IGBT with parameters

A cross section of the half unit cell for a IGBT with N-epi drift region with a fixed impurity concentration of $N_{epi} = 10^{14} cm^{-3}$, a thickness of $95\mu m$, and a total width of $(6 + L_g)\mu m$ is used in the simulation as shown in Fig. 1, where a double diffused p body region has a diffusion depth of $5\mu m$ and peak concentrations of $2 \times 10^{19} cm^{-3}$ and $1 \times 10^{17} cm^{-3}$ at the cathode contact and the inversion layer, respectively. The carrier lifetimes used in the simulation for the drift region are taken as $\tau_{n0} = \tau_{p0} = 1\mu s$ with the ambipolar lifetime of $\tau_a = 2\mu s$. The device has a fixed channel length of $L_{ch} = 2\mu m$ and an accumulation layer length of L_a varied from $4\mu m$ to $48\mu m$ in the simulation, resulting in $L_g = L_a + L_{ch}$ for the gate length.

The gate oxide has a thickness of $0.1\mu m$. The p+ anode has a thickness of $30\mu m$ and a uniform distribution of the impurity with a concentration of $5 \times 10^{18} cm^{-3}$. Fig. 2 shows the simulation results for the electron, hole, and total current denoted as I_{mos}, I_p, and I_{anode}, respectively, as a function of the gate length when the anode current density is fixed at $J(0) = 100[A/cm^2]$. The total current for the present device is thus given by $I_{anode} = I_p + I_{mos} = 6 + L_g(\mu m)$ [μA], whereas the best fit for the electron current is found to be

$$I_{mos} = 3.3 + 0.65 L_g(\mu m) \; [\mu A] \qquad (1)$$

Fig. 3 (a) shows the simulation results for the variation of surface potential, $V_s(y)$ as a function of the surface distance y measured from the n+ cathode $(y = 0)$ with the gate voltage, V_g as a parameter when the n+ cathode is taken for grounded. The variation of the surface potential is contineous, making no distinction between the inversion and accumulation layer, indicating also that the lateral electric field on the surface decreases rapidly with increasing the distance, which contradicts to what can be expected for a MOS with a inversed layer alone, where the electric field on the surface increases with increasing distance towards to the drain. Fig. 3(b) shows the surface potential variation of $V_s(y)$ compared with the potential variation along the lateral path of n+ cathode-p body- N_{epi} at $0.3\mu m$ below the surface, where the condition of the conductivity modulation in the bulk drift region of IGBT holds. Here we have $V_s(L_g) = 1.5V$ at $V_g = 10V$, whereas the potential of the corresponding bulk region at $0.3\mu m$ below the surface is given by $V_w(L_g) = 1.36V$ at the same gate voltage. Thus, a reverse voltage of $V_R = V_s(L_g) - V_w(L_g)$ drops on the gap of the thickness of $t = 0.3\mu m$ between the semiconductor surface and the bulk drift region. The resulting $V_R = 0.14V$ remains almost unchanged for all gate lengths. This voltage drop acts as a potential barrier for holes preventing them flowing into the accumulation layer. From the discussions above we may draw a conclusion that the voltage sum of V_{ch} and V_{acc} ought to be replaced by the sum of $V_s(L_g)$ and V_R in the calculation of $V_{ce,sat}$.

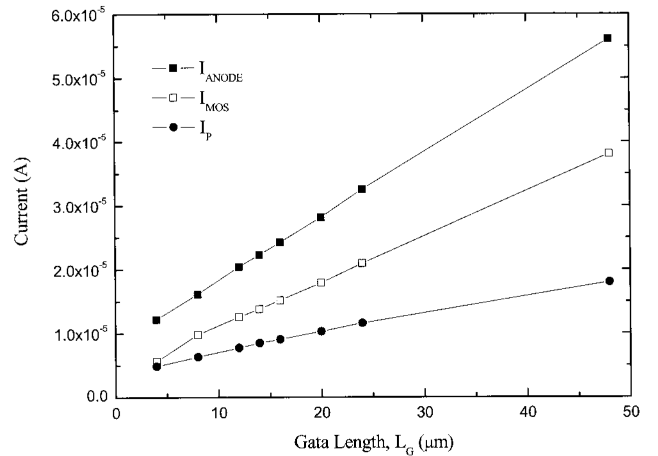
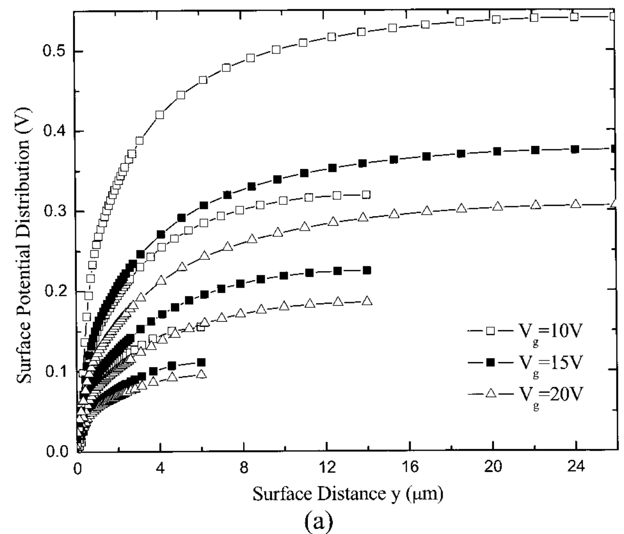
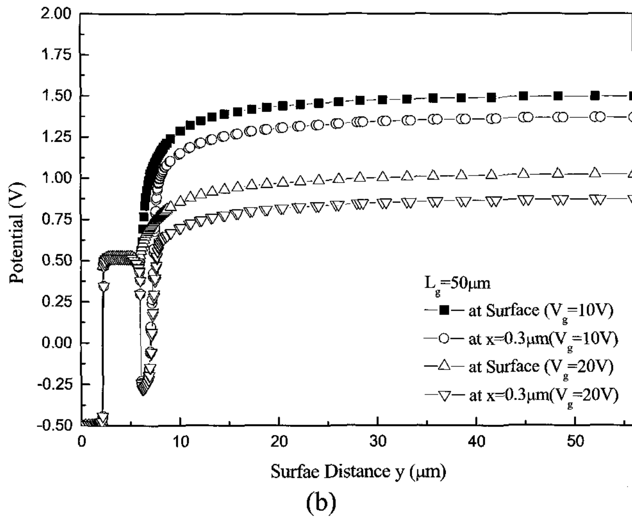


Fig. 2 Variation of electron, hole, and total current vs. gate length at $V_g = 15V$

The gate length dependence of the total surface voltage drop, $V_s(L_g)$ and the carrier density, $p(L_g)$ at $0.3\mu m$ below the surface are shown in Fig.4(a), where both of them are found to increase linearly with increasing L_g, whereas $p(L_g)$ increases but $V_s(L_g)$ decreases with increasing the gate voltage. The linear variations of

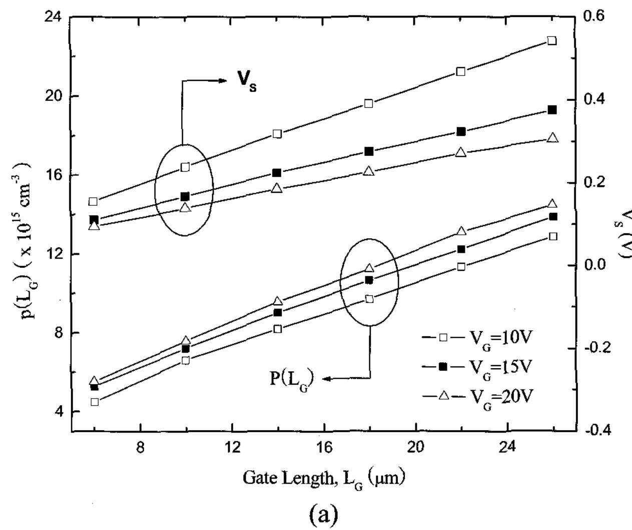


(a)

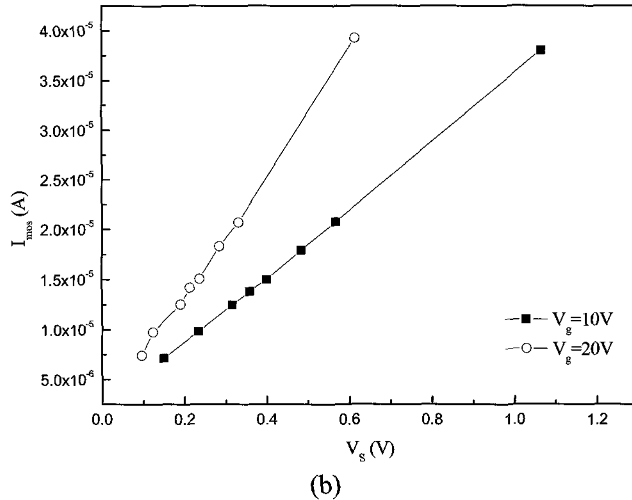


(b)

Fig. 3 (a) Surface potential variation along gate with V_g as a parameter (b) Comparison of surface and bulk potential variation along lateral path



(a)



(b)

Fig. 4 (a) Gate length dependence of surface voltage drop and carrier concentration (b) Relation between total electron current and total surface potential drop

$V_s(L_g)$ and $p(L_g)$ can be approaximated by $V_s(L_g) = 0.025 + \gamma L_g$ and $p(L_g) = p_c + 0.43\times10^{15} L_g$, respectively with $\gamma = 20.80\times10^{-3}$, 14.43×10^{-3}, and $11.76\times10^{-3}\mu m^{-1}$ and $p_c = 2\times10^{15}$, 2.7×10^{15}, and $3.0\times10^{15} cm^{-3}$ for V_g=10V, 15V, and 20V, respectively with L_g in μm. Fig. 4(b) shows a linear relationship between $V_s(L_g)$ and I_{mos} obtained from Fig. 4(a) using eq.(1), where the characteristic conductance of the layer defined by $g = I_{mos}/V_s(L_g)$ yields $g = 31$ and 55 [$\mu\Omega^{-1}$] for $V_g = 10$ and 20 [V], respectively.

3. Analysis and Discussion

The surface potential variation for IGBT as shown in Fig.3 can be obtained when the lateral surface electric field is in the form of $E(y) = E_0 e^{-\alpha y}$ which, in turn, allows expessions for the electron current as well as the surface potential as follows;

$$I(y) = -E(y)/R \tag{2}$$

$$V_S(y) = -(E_0/\alpha)(1 - e^{-\alpha y}) \tag{3}$$

where $R = 1/[W\mu_n\sigma_s][\Omega/cm]$ is used with α for a characteristic constant of the channel layer, W for the channel width of the device($W = 1\mu m$ in the simulation), and μ_n for an effective electron mobility in the layer. The induced charge density, $\sigma_s \cong C_{ox}[V_g - V_t]$ $[C/cm^2]$ on the semiconductor surface can be calculated using $C_{ox} = 3.452\times10^{-8}[F/cm^2]$ and $V_t = -2V$, respectively for the capacitance per unit area of the gate oxide and the layer threshold voltage of the present device. The values for $R = 4.83$ and 2.63 in $[k\Omega/\mu m]$ can be calculated for $V_g = 10$ and 20 [V], respectively, when we take $\mu_n = 500[cm^2/Vs]$, which is close to the value for the inversion layer.

As long as $1 \succ\succ e^{-\alpha L_g}$ satisfies in eq.(3), combination of eqs.(2) and (3) with $I(0) = I_{mos}$ may lead to a useful expression of $\alpha = gR$ for the attenuation constant of the surface field. Using the given values for g and R, the above relation yields $\alpha = 0.15[\mu m^{-1}]$ for both $V_g = 10$ and 20 [V], being independent of the gate voltage, allowing a complete calculation of $V_S(y)$ with $E_0 = -RI_{mos}$ in eq.

(2), and accounting also for the simulation result of the surface potential which increases with increasing gate length but decreases with increasing the gate voltage as shown in Fig. 3.

Fig. 5 shows the variation of the carrier density, $p(x)$ and the potential distributions, $V_{epi}(x)$ as a function of the distance measured from the gate at $y = L_g$ along the vertical direction towards the anode with the gate length as a parameter, where the forward biased voltage term on the anode junction, $V_j \approx 0.08[V]$ remains constant. The carrier density increases significantly in the proximity of the gate with increase of the gate length, reducing the voltage drop in the region accordingly, but remains unchanged in the rest of the drift region.

The analytic expression of the voltage drop V_{epi} for the region $0 \le x \le w$ has been reported recently[4]. An extra potential drop in the proximity of the gate may be obtained using the condition of $J_p(x) \approx 0$ in the region of $w \le x \le w + \Delta w$. The result is

$$\Delta V = v_T \ln[p(L_g)/p(w)] \quad (4)$$

where v_T is the thermal voltage.

Assuming $J(x)=J(0)$ in the region $w \le x \le w+\Delta w$ and using $J_p(x) \approx 0$ may also lead to $J(x) = [qD_a/c'](dp/dx)$, resulting in $p(w) = p(L_g) - [c'J(0)/qD_a]\Delta w$ where D_a is the ambipolar diffusion coefficient. $[c'J(0)/qD_a]\Delta w = 4.44 \times 10^{15} cm^{-3}$ may be obtained by taking $\Delta w \approx 5\mu m$ for the diffusion depth of the diffused p body and $D_a = 18.74[cm^2/s]$ corresponding to the drift region doping concentration of the present device.

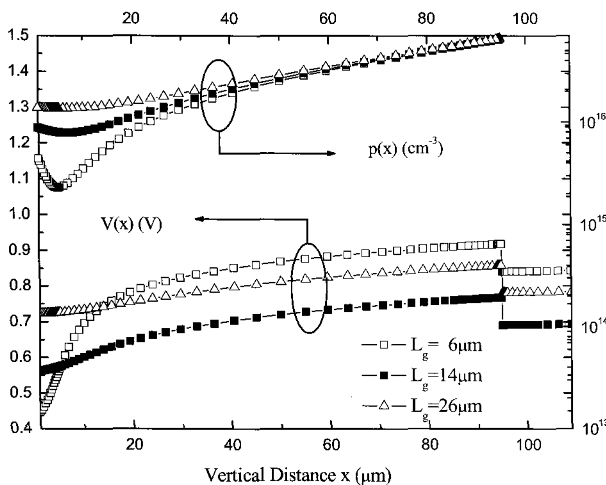


Fig. 5 Carrier density and potential distributions along drift region at $V_g = 15V$

Fig. 6 shows the calculation results for variation of $V_s(L_g)$, V_{epi}, and $V_{ce,sat}$ as a function of the gate length, where $V_{ce,sat} \approx 1.0 + V_s(L_g) - V_R + V_{epi} - V_j$ is calculated with $V_R \approx 0.14V$ and $V_j \approx 0.08V$ fixed and with the potential jump of 1.0V from the p-contact(-0.5V) to the n+ cathode(+0.5V) taken into account as may be observed in Fig. 3(b). A similar potential jump[3] along the vertical path of p-n-p structure near the cathode has been reported previously. A fair agreement with the simulation results may be observed for the forward voltage drop. The optimum gate length must exist since $V_s(L_g)$ increases but V_{epi} decreases with increasing L_g, while other terms remain almost constant. Thus, Fig.5 exhibits a minimum of $V_{ce,sat} = 1.16V$ at around $L_g = 14\mu m$ in the present case.

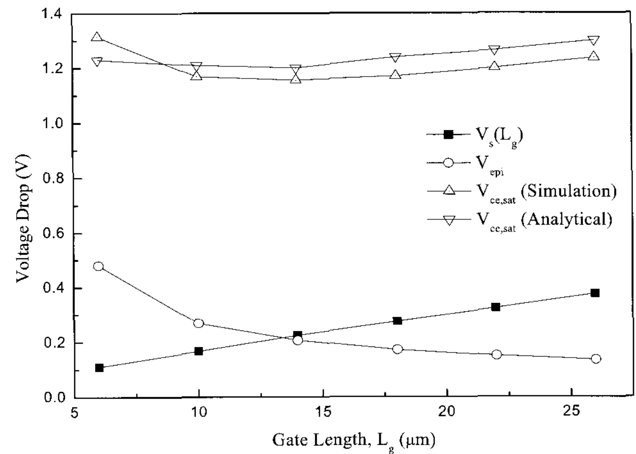


Fig. 6 Forward voltage drop with the voltage drops on surface and bulk drift region as a function of gate length

4. Conclusion

In conclusion, it has been demonstrated that the optimum gate length for the minimum forward voltage drop of IGBT can be obtained analytically. Analytical model for the surface potential effective for the channel layer of IGBT provided in the present work will be useful in IGBT design calculations.

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