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Optimal Design of Spiral Inductors on Silicon Substrates for RF ICs

Yeong-Joo Moon[1], Moon-Ho Choi[1], Kee-Yeol Na[1], Nam-Su Kim[1], and Yeong-Seuk Kim[1,a]

Abstract

Planar spiral inductors on silicon substrates were optimally designed using MATLAB, which is a tool to perform numerical computations with matrices. The equivalent circuit parameters of the spiral inductors were extracted from the data measured from the spiral inductors fabricated using a 0.18 ㎛ RF CMOS process. The metal width, which is a critical design parameter, was optimized for the maximum quality factor with respect to the operating frequency.

Key Words : Spiral inductor, RF ICs, Quality(Q) factor

1. INTRODUCTION

Spiral inductors have become the key passive component in the design of RF CMOS ICs. However, conventional CMOS processes do not provide a sufficient quality(Q)factor for spiral inductors due to the thinner dielectric, thinner top metal thicknesses and lossy silicon substrates. Therefore, changes in the CMOS processes such as employing a thicker top metal or using copper instead of aluminum to improve Q factor of spiral inductors for RF CMOS ICs have been reported. When we design RF CMOS ICs, the empirical models and layout parameters are provided by a semiconductor foundry. However it is unclear whether these layout parameters are optimal. For example, one of critical layout parameters, the metal width, is kept constant, e. g., 15 ㎛ regardless of the other design conditions. However, Post[1] reported that Q factor is a function of the metal width and the number of turns. In this brief, a simple methodology is proposed for the optimal design of spiral inductors. Equivalent circuit parameters[2] were analyzed to give the y-parameters which were converted into z-parameters using MATLAB[3]. The Q factor of spiral inductors was then calculated from these z-parameters. For a given inductance value, the metal width was varied to obtain a maximum Q factor at the operating frequency.

2. MODELING USING METLAB

Figure 1 shows an equivalent circuit model reported by Yue and Wong[2]. The reported formula by Greenhouse[4] were used to calculate the spiral inductances, L_s, and the other circuit parameters are given by

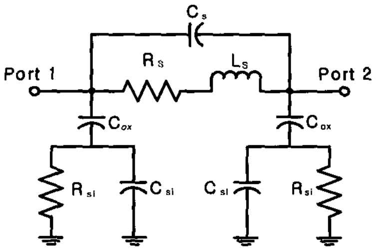

Fig. 1. Equivalent circuit model of the spiral inductors.

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1. School of Electrical and Computer Engineering, Chungbuk National University
(12 Gaesin-dong, Cheongju, Chungbuk, Korea)
a. Corresponding Author : kimys@cbu.ac.kr

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$$R_s (= 1/G_s) = \rho \cdot l / [w \cdot \delta \cdot (1 - e^{-t/\delta})] \quad (1)$$

$$C_{ox} = l \cdot w \cdot \varepsilon_{ox} \cdot t_{ox} / 2 \quad (2)$$

$$C_{si} = l \cdot w \cdot C_{sub} / 2 \quad (3)$$

$$R_{si} (= 1/G_{si}) = 2/(l \cdot w \cdot G_{sub}) \quad (4)$$

where l, w, t, t_{ox}, ρ, δ are the metal length, width, thickness, thickness of the oxide layer between the inductor and substrate, the metal resistivity, the metal skin depth, respectively. C_{sub} and G_{sub} are the empirical parameters extracted from the measured data. These equivalent circuit model parameters were used to calculate the y-parameters as follow :

$$\begin{aligned} y_{11} &= y_{22} = y_s + y_p \\ &= jwC_s + \frac{G_s}{1 + jwL\,G_s} - \frac{w^2 C_{si} C_{ox} - jwC_{ox} C_{si}}{G_{si} + jw(C_{ox} + C_{si})} \end{aligned} \quad (5)$$

$$y_{12} = y_{21} = -y_s = -jwC_s - \frac{G_s}{1 + jwL\,G_s} \quad (6)$$

The y-parameters were transformed into z-parameters and the input impedance z_{in} was calculated to give the Q factor of the spiral inductors.

$$z_{in} = z_{11} - \frac{z_{22}}{z_{12} \cdot z_{21}} \quad (7)$$

$$Q = \frac{z_{in\_imag}}{z_{in\_real}} \quad (8)$$

3. PARAMETER EXTRACTION

In order to verify the model, the empirical parameters were extracted from the measured data. G_{sub} was extracted from the graph of G_{si} versus lw (area). The slope of this graph represents $2/G_{sub}$. Simultaneously C_{sub} was extracted from the graph of C_{si} versus lw (area) and the slope is $C_{sub}/2$. The extracted parameters were t_{ox}=9.25 ㎛, ρ=3.60x10^{-6} Ωcm, G_{sub} =70.8 S/cm^2, C_{sub}=1.33x10^{-10} F/cm^2 for the 0.18 ㎛ RF CMOS process. Using these parameters and the calculated inductances from MATLAB, the measured and simulated Q factor versus frequency were plotted in Fig. 2. The results show a fairly good fit demonstrating the validity of the model.

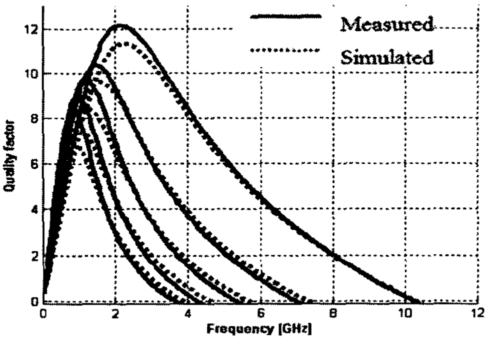

Fig. 2. Measured and simulated quality factor versus frequency.

4. OPTIMAL DESIGN

The optimum design parameters such as the metal width of the spiral inductors were determined using the model and the extracted circuit parameters. Figure 3 shows a flowchart of the optimization process. The reference structure is provided from the design kit of a RF CMOS foundry. The inductance value and operating frequency is given from the design specifications. The metal width was increased in order to obtain the optimal value. However, the inductance value also increased. Therefore, the radius was decreased in order to maintain a constant inductance value. The equivalent circuit parameters were then calculated using the circuit parameter equations and the measured data. In addition, the inductance was computed by the MATLAB routine, which uses the algorithm reported by Greenhouse. If the inductance value is within the design tolerance, Q factor is calculated using the MATLAB routine.

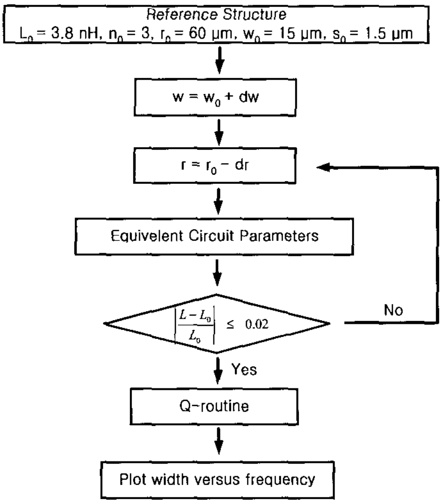

Fig. 3. The flowchart of the optimization process.

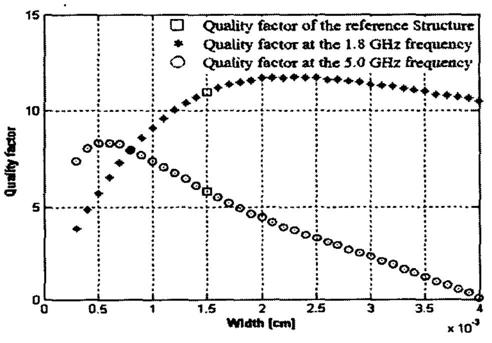

Fig. 4. Quality factor versus the metal width.

From these calculations, a plot of Q factor versus the metal width was performed, as shown in Fig. 4. Figure 5 shows Q factor versus the frequency. For a spiral inductor of 3.73 nH operating at 1.8 GHz, the optimal metal width from Fig. 4 is 23 ㎛ instead of 15 ㎛ suggested from the foundry and Q factor at 1.8 GHz from Fig. 5 is 11.74 compared to Q factor of the reference structure of 10.95. For a spiral inductor of 3.73 nH operating at 5 GHz, the optimal metal width from Fig. 4 is 6 ㎛, which is much lower than the reference width, and Q factor at 5.0 GHz from Fig. 5 was 8.32 compared with Q factor in the reference structure of 5.84.

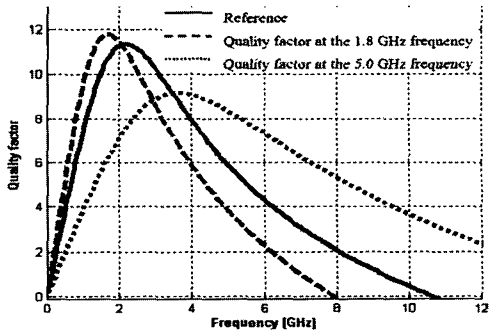

Fig. 5. Quality factor versus the frequency.

5. SUMMARY

Planar spiral inductors were optimally designed using the MATLAB model and the extracted equivalent circuit parameters. The Q factor of the 3.73 nH inductor operating at 1.8 GHz and 5.0 GHz using the 0.18 ㎛ RF CMOS process increased to 7.21 % and 42.47 % compared with Q factor from the reference structure, respectively.

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