Novel Design Methodology using Automated Model Parameter Generation by Virtual Device Fabrication

Jun-Ha Lee† and Hoong-Joo Lee*

Abstract - In this paper, an automated methodology for generating model parameters considering real manufacturing processes is presented with verified results. In addition, the outcomes of applications to the next generation of flash memory devices using the parameters calibrated from the process specification decision are analyzed. The test vehicle is replaced with a well-calibrated TCAD simulation. First, the calibration methodology is introduced and tested for a flash memory device. The calibration errors are less than 5% of a full chip operation, which is acceptable to designers. The results of the calibration are then used to predict the I-V curves and the model parameters of various transistors for the design of flash devices.

Keywords: design methodology, flash memory, model parameter, semiconductor simulation

1. Introduction

The specification generation and circuit design for a new upgraded version of a flash memory transistor has yet been unable to equal improvements made in the area of device performance. This is simply due to the fact that the length of time required for the manufacturing process for the test vehicle for circuit design has not physically decreased. From the view of circuit design, the SPICE model parameters cannot be obtained once the initial process specification has been established. Thus, a temporary blueprint using the model parameters of a previous generation or of similar transistors is required until the model parameters from the test vehicle have been extracted [1]. After a comparison of the model parameters taken from the test vehicle has been made with the predicted parameters, the main circuit design can be proceeded with by considering the discrepancies between them. In this type of main design flow, it is difficult to secure the design margin and to anticipate the performance improvement. If the model parameters at the primary stage of process specification generation reflect the real manufacturing process, a rapid and stable design of the main circuit is possible [2].

This paper presents a concept and a methodology realizing automated generation of model parameters within the limits of a real process by using TCAD to determine the specifications for the test vehicle [3]. First of all, an accurate TCAD simulation is essential to conduct the proposed flow. If the accuracy of the TCAD simulation is to be evaluated, the calibration methodology for the process and the device simulators must be embodied. Although the time required depends on the devices, in the cases of five types of flash memory devices, the design engineer can utilize the model parameters generated within five days. A point requiring care is that TCAD cannot consider all phenomena related to newly adopted manufacturing processes for next-generation devices. Nevertheless, the difference can be minimized when process engineers make good use of TCAD results as targets in process optimization. Additionally, from the design engineer's point of view, when sufficient information and time for design is provided, a stable circuit with sufficient margin can designed.

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2. The Novel Design Flow

The proposed innovative concept of design flow is depicted in Fig. 1. In the existing design flow, without electrical measurements, rough model parameters, which are modified from a previous generation or from similar devices, have been delivered for circuit design. With these rough parameters, the circuit design proceeds, and the test vehicle is manufactured. However, in this case, the manufacturing process for the TEG (test engineering group) module costs as much as the entire main-chip process because the test vehicle does not include the main-chip design. Therefore, the manufacturing process must have requirements for the model parameters. It is impossible to proceed with an accurate design without the

model parameters, and additional revision will be needed. That is to say, during the first run, process engineers and design engineers are fabricated in a standby state [4]. Once the test vehicle has been composed and the model parameters have been delivered to the design engineers, the process engineers begin their duties of process optimization and improvement of device performance.

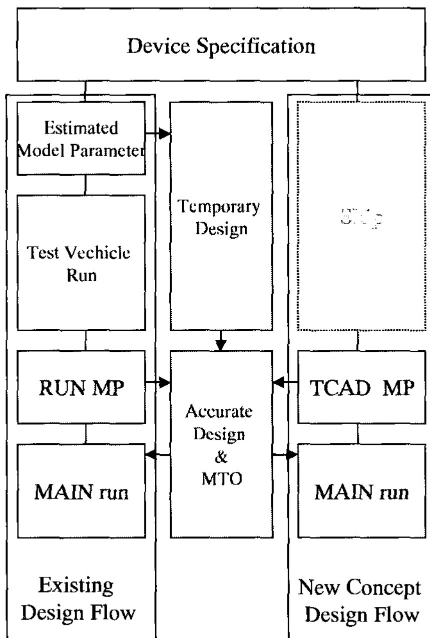


Fig. 1 New concept of design flow using TCAD without a test vehicle run compared to the existing design flow.

3. Simulator Calibration Method

A calibration methodology using a process simulator, TSUPREM4, and a device simulator, MEDICI, are presented in this work [5].

Fig. 2 presents the calibration flow using TCAD simulators. The calibration actually starts with accurate information on the manufacturing process flow and the electrical characteristics. Then, the thickness of the gate-oxide layer and the doping concentration of the gate polysilicon layer, which can be decided independently of accurate process specification, are set up. This is based on two facts. The first is that the capacitance of the deep accumulation region depends on the thickness of the oxide, tox, without the effect of the channel doping profile. The second one is that the capacitance of the deep depletion region depends on the surface doping levels of the oxide layer and the polysilicon [6]. Therefore, through a simulation considering the polysilicon depletion and the quantum effect, these values are determined with a target value of the CV curve measured at the inversion pattern of a large area. The calibration of the one-dimensional process simulator, TSUPREM4, is performed considering the fact that the back bias effect for a long channel depends on the vertical channel doping profile rather than on the mobility value. At this step, because the characteristic related to the channel dose is very critical, numerous target values of the channel dose split must be provided. For medium-channel and short-channel lengths, a 2-dimensional process simulator calibration is applied using the target values of Reverse-Short-Channel-Effect/Short-Channel-Effect (RSCE/SCE) and back-bias effect [7]. For a 1D/2D process calibration, the threshold voltage variation due to the mobility value without calibration can be reduced by replacing RSCE/SCE and the back-bias effect with a gate bias allowing a specific sub-threshold current.

Once the process calibration is completed, the mobility calibration proceeds with the target values of the on-current from the Id-Vg and Id-Vd curves. The transverse mobility is calibrated first with a target from the Id-Vg characteristics and is not relevant to the carrier saturation velocity; then, the high-field mobility, including saturation velocity, is calibrated with the target from the Id-Vd characteristics [8-10]. The calibrations of the parameters related to carrier lifetime, field-dependant lifetime and impact ionization with the target values from the BV curve finally make accurate simulations for Ioff and BVdss possible.

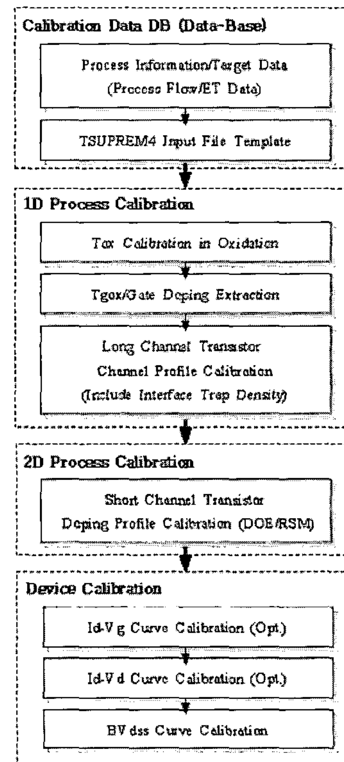
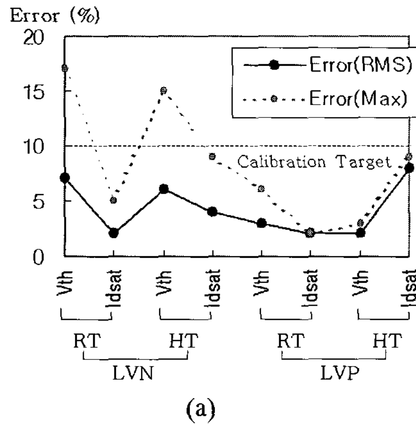


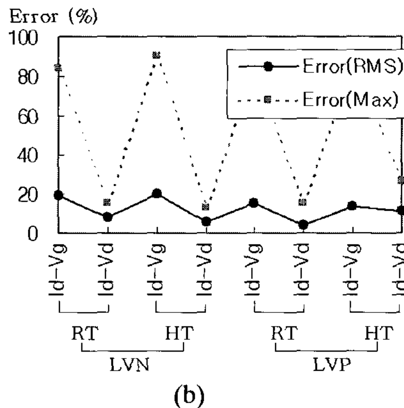
Fig. 2 TCAD calibration flow.

4. Model Parameter Generation

After the TCAD simulator calibration for the flash memory device has been completed using the proposed calibration methodology, model parameter extraction for the next generation device is then performed. Flash memory devices are classified into a low-voltage type of nMOS(LVN) and pMOS(LVP) device, a high-voltage type of nMOS(HVN) and pMOS(HVP) device, and a depletion type of nMOS(DPL) device. Complete model-parameter extraction for the full-chip design requires I-V data of all the transistors mentioned. Therefore, the calibration was performed for five types of flash memory devices. Fig. 3 presents the calibration errors for LVN and LVP: average errors between measured values and simulation results of (a) Vth and Idsat for various gate lengths and of (b) Id-Vg and Id-Vd for various bias conditions. The average error value is calculated from the summed average of individual errors. The channel length split has 6 cases: 0.1 μm, 0.2 μm, 0.5 μm, 0.54 μm, and 5.0 μm. Also, the bias condition spilt contains an assortment of cases within the device operating conditions.



(a)



(b)

Fig. 3 Calibration errors for LVN and LVP. Average errors between measured values and simulation results of (a) Vth and Idsat for gate lengths and (b) Id-Vg and Id-Vd for bias conditions.

Table 1 demonstrates a comparison between the simulation and the extracted parameters from the TEG measurement of the test vehicle in which the errors are less than 5%. The five typical items of comparison are as shown in Table 1. At circuit design, not all curves are needed for an accurate simulation of chip performance. Table 2 indicates the electrical characteristics essential to circuit design for each device. Because the model parameters do not ideally speak for the electrical characteristics, the allowable errors between the real characteristic value and the model parameter are defined in Table 2. In addition, the rates of correctness of the TCAD simulation for characteristic values of each actual device are given.

Table 1 Sensing time comparison for model parameters between the simulation and the run.

	Ax ~ ATD invoke(IO_SUM)	Discharge (nPDIS)	Precharge (nPEG)	Sensing (nPEG ~DOT)	I/O drive (DOT ~ I/O)
Simulation	3.8r	18.6n	23.5n	10.2n	11.6n
Run	3.6n	18.5n	23n	10n	11.6n

Table 2 Average errors of the TCAD simulation and tolerable error of design for device characteristics.

	Vth [V]		Idsat [uA/um]		Swing [mv/dec]		Body Effect [V]@Vb=3	
	Design	TCAD	Design	TCAD	Design	TCAD	Design	TCAD
LVP	10%	15%	10%	15%	20%	15%	20%	15%
LVN	10%		15%		10%		10%	
HVP	15%		15%		20%		25%	
HVN	10%		15%		20%		5%	
Depl	15%		15%		10%		10%	

After the process specification for the next generation of flash memory devices has been completed, the expected values of Vth (threshold voltage) and Idsat (saturation current) are obtained using a simulation. The simulations for some types of next generation devices have not met the engineers' expectations. The reason for this is derived from process changes, such as in the case of furnace annealing being replaced with RTA (rapid thermal annealing) and the thickness of the silicon surface consumed by sacrificial oxidation varing. Another reason could be the fact that the RTA simulation has not been properly calibrated to the corresponding process specification. In this work, supposing that the identical heat budget is set up for RTA as for furnace annealing, an RTA simulation model, which is the same as furnace annealing, has been adopted. However, the simulation results have somewhat missed the expected target values of the electrical characteristics. In this simulation, the expected values of Vth can be brought into agreement with the measurements by adjusting the dose value of ion implantation for the threshold voltage. A comparison of the expected values with the simulation ones for LVN and LVP after the proposed calibration and simulation flow have been completed is shown in Table 3.

Normal simulation means a simulation without calibration. The proposed simulation with a calibration flow has been verified through a comparison of the simulated results with measurements for real devices.

Table 3 TCAD simulation results for the threshold voltage and the saturation current for a flash memory: (a) LVN device and (b) LVP device.

(a)

LVN			
Item	Estimate	Normal Sim.	Calibrated Sim.
dose	3.1×10^{12}		3.3×10^{12}
Vth	0.53	0.51	0.53
Idsat	375	326	320

(b)

LVP			
Item	Estimate	Normal Sim.	Calibrated Sim.
dose	3.0×10^{12}		1.8×10^{12}
Vth	-0.53	-0.70	-0.54
Idsat	-187	-117	-152

5. Conclusion

This paper has presented SPICE model parameter generation by using a TCAD simulation rather than a test vehicle. This procedure has cut the design time by approximately two months. With the existing case, the model parameters are extracted from the test vehicle. With this flow, the model parameters can be provided at the same time as the decision on the device specification. Therefore, from the early stage of circuit design, model parameters reflecting the actual process can be used in the circuit design. In the case of products such as flash memories requiring a wide range of operating voltages and various types of devices, since it is difficult to predict the device characteristics under shrinkage, model parameter generation requires a test vehicle. Therefore, model parameter generation by using TCAD simulations can be more effective for flash memory products. The accuracy of the TCAD simulations has been reported so that the proposed simulation flow could be applied to flash products. Also, the characteristic values expected in the specification decision for next-generation flash memory devices have been shown to be similar to those from simulations of the process.

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