A High-Frequency Signal Test Method for Embedded CMOS Op-amps

Kang Chul Kim, Seok Bung Han, *Member, KIMICS*

Abstract—In this paper, we propose a novel test method to effectively detect hard and soft faults in CMOS 2-stage op-amps. The proposed method uses a very high frequency sinusoidal signal that exceeds unit gain bandwidth to maximize the fault effects. Since the proposed test method doesn't require any complex algorithms to generate the test pattern and uses only a single test pattern to detect all target faults, therefore test costs can be much reduced. The area overhead is also very small because the CUT is converted to a unit gain amplifier. Using HSPICE simulation, the results indicated a high degree of fault coverage for hard and soft faults in CMOS 2-stage op-amps. To verify this proposed method, we fabricated a CMOS op-amp that contained various short and open faults through the Hyundai 0.65-um 2-poly 2-metal CMOS process. Exper- imental results for the fabricated chip have shown that the proposed test method can effectively detect hard and soft faults in CMOS op-amps.

Index Terms—fault, high frequency test, mixed-signal testing, analog testing.

I. INTRODUCTION

Due to the development of VLSI technology and market requirements, the trend in designing mixed-signal ASICs has been increased. Analog testing is a challenging task and is considered as one of the most serious problems in analog and mixed-signal ASIC design[1,2]. But unlike the digital systems that use a binary test pattern, analog systems are complex and use a non-Boolean test pattern.

Degraded circuits performance as well as nonfunctional operation must be checked. Thus, circuit complexity rather than volume complexity is the dominant problem in analog test. As a result, analog testing is more difficult and requires a longer testing time than testing purely digital circuits[3,4].

The integrated op-amp is the most widely used active linear circuit in today's analog systems. For functional analog blocks with embedded op-amps, the test procedure will be easier and the fault coverage will be higher if it is proven that the op-amps are fault-free [5].

Manuscript received November 4, 2004

Kang Chul Kim is with Department of Computer Engineering, Yosu National University, Yosu, Chonnam, Korea.

Seok Bung Han is with Department of Electronic Engineering, Gyeongsang National University, Jinju, Gyeongnam, Korea.

Specification testing, a common test method for analog circuits, is usually very expensive, and resulting in a long testing time and requiring dedicated test equipment. Therefore, a more efficient test pattern generation algorithm and DFT technique were required. Fault modeling of op-amps can be classified into two main categories, hard (catastrophic) faults and soft (parametric) faults. Hard faults are shorts and open circuits between the terminals of a transistor. These faults are caused by random defects (e.g. dust particles) and result in a complete malfunction of the circuit. Soft faults are deviations of the nominal parameter values that exceed the attributed tolerance bands. These faults are caused by statistical fluctuations in the manufacturing process and result in functional circuits with degraded specifications.

Many researchers have addressed the problem of testing integrated op-amps. Op-amp power supply control has been proposed in [6]. Because it requires varying the power supply voltage of the CUT, its integrated implementation causes some problems. IDDQ testing technique [7] has resulted in fault detection coverage of less than 90%. Current sensing circuits necessitate at least one transistor be cascaded with the CUT between supply rails, which introduces performance degradation. The fault coverage of DC voltage tests [8] is around 80% excluding the capacitor faults which cannot be detected by DC voltage. The oscillation-test method [5,9,10] converts op-amps to oscillators and the oscillation frequency is measured to monitor faults. As the CUT is converted to an oscillator, the area overhead for DFT is high. The Multisine test method [11] combines individual sinusoidal test signals into a single waveform without sacrificing fault coverage. This method requires complex algorithms to generate a single test pattern. Another common problem in the above methods is that soft faults are not considered.

In an attempt to overcome some of the above-mentioned limitations, we propose a new test method using a unique frequency characteristic for CMOS 2-stage op-amps, which can detect soft faults as well as hard faults. Test pattern generation is easy and the area overhead is low. Total test cost are therefore much lower because a single test pattern is used to detect all target faults.

II. HIGH-FREQUENCY TEST METHOD

The proposed test method uses a single high frequency sinusoidal test pattern input. Soft faults are more difficult

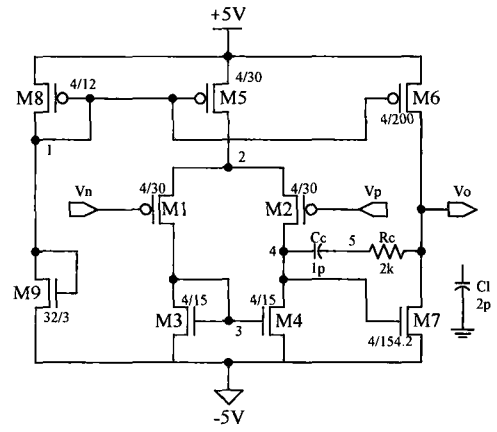


Fig. 1 Compensated CMOS 2-stage op-amp. This op-amp is the benchmark circuit.

to detect than hard faults because they only affect the normal operation of op-amps to a small degree within the frequency range of a unit-gain bandwidth. We therefore attempted to generate an efficient test pattern for soft faults as well as hard faults by analyzing the resulting change in frequency characteristic of the affected faults.

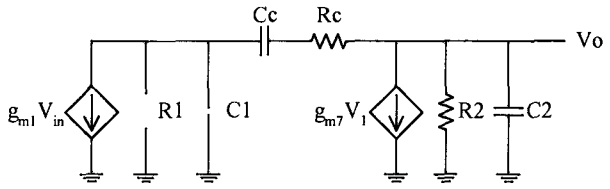


Fig. 2 A small-signal model of the CMOS 2-stage op-amp.

Figure 1 shows the schematic of the CMOS 2-stage op-amp that is considered as the CUT. This op-amp is the benchmark circuits used for researching and evaluating analog testing methods developed by the IEEE Mixed-Signal Technical Activity Committee [12]. A simplified small-signal model for this op-amp is shown in figure 2, where each components is given values as shown:

$$R_1 = r_{ds4} \| r_{ds2} \tag{1}$$

$$C_1 = C_{db2} + C_{db4} + C_{gs7} \tag{2}$$

$$R_2 = r_{ds6} \| r_{ds7} \tag{3}$$

$$C_2 = C_{db7} + C_{db6} + C_L \tag{4}$$

The dominant pole frequency, ω_{p1}, and non-dominant pole frequency, ω_{p2}, are given by

$$\omega_{p1} \cong \frac{1}{R_1[C_1 + C_c(1 + g_{m7}R_2)] + R_2(C_2 + C_c)} \tag{5}$$

$$\omega_{p2} \cong \frac{g_{m7}C_c}{C_1C_2 + C_2C_c + C_1C_c} \tag{6}$$

If soft and/or hard faults exist in the CUT, r_{dsi}, C_{dbi}, C_{gsi} and g_{mi} of the transistors are changed. This results in variations in equations from (1) to (4) for R_1, R_2, C_1, and C_2. Hence, ω_{p1} and ω_{p2} in equations (5) and (6) are changed by hard and soft faults. Using this variation in frequency characteristic between good and faulty circuits, we search for the optimal frequency for the test pattern to detect hard and soft faults in CMOS op-amps.

Within the frequency of the unit-gain bandwidth, the effect of soft faults seldom appears because soft faults are not serious. But when a frequency is higher than the unit-gain bandwidth, the fault effect increases because the frequency characteristic changes differently between good and faulty circuits. Therefore, to maximize the fault effect, the frequency of the test pattern has to be selected that is higher than the frequency ω_{p2}.

In the test mode, the CUT is converted to a unit-gain op-amp using analog switches, and the sinusoidal signal with a higher frequency than ω_{p2} is applied. As the frequency of ω_{p2} becomes higher than unit-gain bandwidth, the peak voltage of the output becomes smaller than that of the input. Therefore, the peak voltage for the test pattern should be set as high as possible.

III. DESIGN OF TEST IC

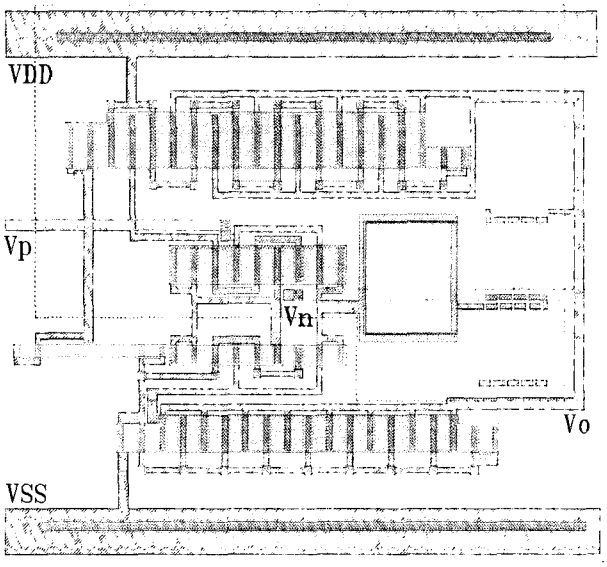


Fig. 3 Physical layout for CMOS op-amp.

To verify the proposed method, we designed the CMOS op-amp as shown in figure 1 with a 0.65-㎛ 2-poly 2-metal process. Figure 3 shows the layout of the circuit. Also, faulty circuits containing short and open faults were included to test the various fault effects. Faults were introduced using a MOSFET or a metal layer.

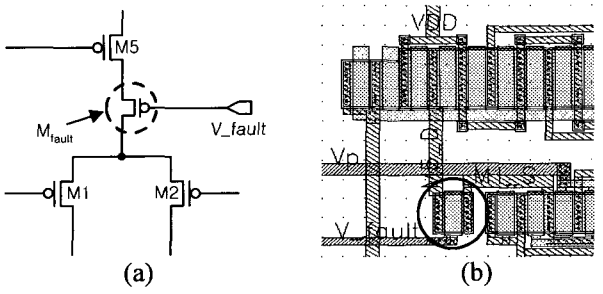


Fig. 4 Drain-open fault for the M5 transistor using a pMOSFET. (a) Schematic and (b) Layout

Figure 4 shows a drain-open fault for the M5 transistor using a pMOSFET. The M5 drain is connected to the source of the M_{fault} transistor and the sources of the M1 and M2 transistors are connected to the drain of the M_{fault} transistor. The V_fault node that is the gate of the M_{fault} transistor is connected outside of the chip to control it. If a 0V signal is applied to the V_fault node, the M_{fault} transistor turns on and op-amp operates as a normal circuit. But if a +5V signal is applied to the V_fault node, the M_{fault} transistor turns off and the op-amp does not operated normally. Similar to the open fault mentioned above, a short fault can be simulated using a MOSFET. Such an injected fault is not a realistic feature for a fault, but it provides a good comparison between a good and faulty op-amp.

Figure 5 shows a drain-source short fault in the M1 transistor using a metal layer. To produce the short fault, an extra metal layer is applied between the drain and source metal layers of the M1 transistor. Also, an open fault is easily simulated by removing the metal layer. This type of fault is realistic.

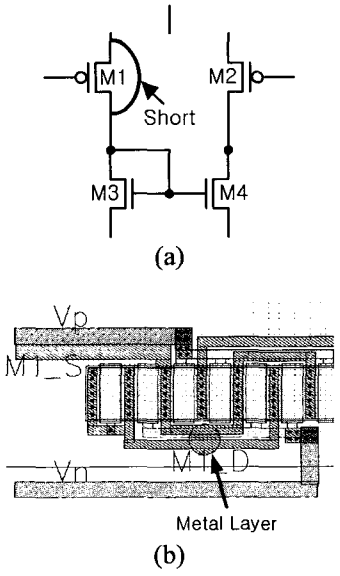


Fig. 5 Drain-source short fault injection of the M1 transistor using a metal layer. (a) Schematic and (b) Layout

Using these two kinds of fault simulation methods, we designed faulty op-amps that contained various short and open faults to verify the proposed test method.

IV. SIMULATION RESULTS

The proposed test method was verified by using the HSPICE simulation and the Hyundai 0.65-㎛, 2-poly, 2-metal process. Short faults were modeled using a 1Ω resistance setting. Open faults were modeled using an off-state MOSFET, whose source and drain terminals were left open. Soft faults were simulated by varying the W/L ratio and Vth by 30%.

The optimal frequency of test pattern was 25㎒ when output load capacitance was 45pF and a peak voltage of ±3V was used. The Vmax was between 243㎷□408㎷ for the output tolerance of a good circuit and the Vmin was between -308㎷□-444㎷. These values were determined using simulations of best-case and worst-case process parameters. Note however that the test pattern and tolerance band used in this paper should be changed if a different CUT and process parameters are used.

Figure 6 shows the output waveforms of drain-source short faults. Most outputs of the faulty circuits indicate a DC voltage and some faults have sinusoidal waveforms. The outputs of faulty circuits with sinusoidal waveforms have voltage levels exceeding the tolerance band, and therefore the fault can be easily detected. Table 1 shows the simulation results of hard faults. The outputs of eight faults shown in Table 1 have sinusoidal waveforms, but the output voltages exceed the tolerance band. The outputs of faults other than these eight have DC voltages or distorted waveforms. Thus the fault coverage for hard faults is 100%.

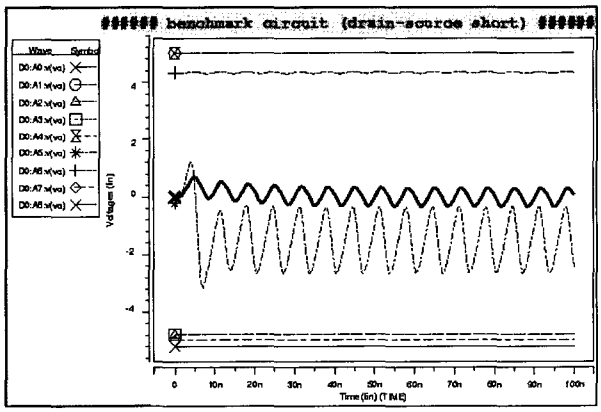


Fig. 6 Output waveforms of drain-source short faults

Table 1. Simulation results for hard faults (mV)

Fault	Vmin	Vmax	Fault	Vmin	Vmax
M5 ds-s*	-2653	-369	M8 s-o	-1426	1041
M5 gd-s	-1699	-590	M5 g-o	-1666	428
M6 gd-s	-813	445	M6 g-o	-640	661
M8 d-o	-1456	1058	M7 g-o	-257	260
All other faults		DC voltage or distorted waveforms			

* M5 ds-s: drain-source short fault of M5 transistor

Tables 2 and 3 show the simulation results using deviation faults for Vth of ±30% and for W/L ratio of ±30%, respectively. For soft faults, the outputs all have sinusoidal waveforms. Other than for the M7 transistor and the +30% W/L ratio fault for the M6 transistor, all of the soft faults have voltage levels exceeding the tolerance band, resulting in an 84% fault coverage.

Table 2. Simulation results for Vth deviation faults (mV)

	Vth 30% decrement		Vth 30% increment	
	Vmin	Vmax	Vmin	Vmax
M1	-9	683	-729	-44
M2	-726	-39	-14	676
M3	-1246	-623	518	1196
M4	529	1210	-1243	-621
M5	-525	433	-251	216
M6	-425	418	-308	219
M7	-384	320	-356	318
M8	-235	170	-545	506

Table 3. Simulation results for W/L ratio deviation faults (mV)

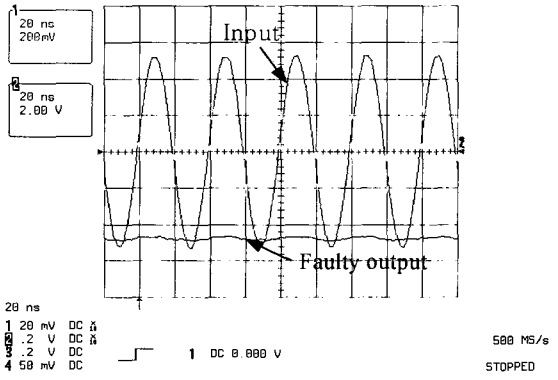
	W/L 30% decrement		W/L 30% increment	
	Vmin	Vmax	Vmin	Vmax
M1	-557	168	-285	371
M2	-177	456	-455	280
M3	459	1185	-977	-348
M4	-1196	-583	264	966
M5	-244	240	-485	408
M6	-322	231	-404	391
M7	-358	330	-365	298
M8	-559	521	-272	212

V. EXPERIMENTAL RESULTS FOR THE FABRICATED PROTOTYPE IC

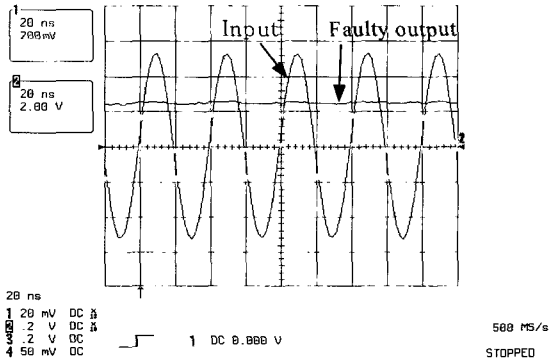
The test IC was fabricated using the Hyundai 0.65-㎛, 2-poly, 2-metal CMOS process. Because the actual output load capacitor of the integrated op-amp is about 40pF, the test pattern was regenerated using a frequency to consider a 40pF load capacitor. The frequency of the test pattern used to test the fabricated IC was 25㎒ and the peak input voltage was ±0.5V.

The output waveforms for the high frequency tests are shown in figure 7. As the output waveforms for the M1 drain open fault and the M1-M2 drain short fault are DC voltages, these faults can be easily detected using the proposed test method.

Figure 8 shows the output waveforms for the M5 gate-drain short fault. Figure 8(a) shows the output waveforms for the test pattern using a frequency of f=25㎒, and a Vpp=±0.5V. Because the difference between the good and faulty output waveforms is so small, it's difficult to distinguish the faulty circuit. However when the peak input voltage of the test pattern is increased to ±3V with the same frequency, the difference between the good and faulty outputs is about 0.5V as shown in figure 8(b).



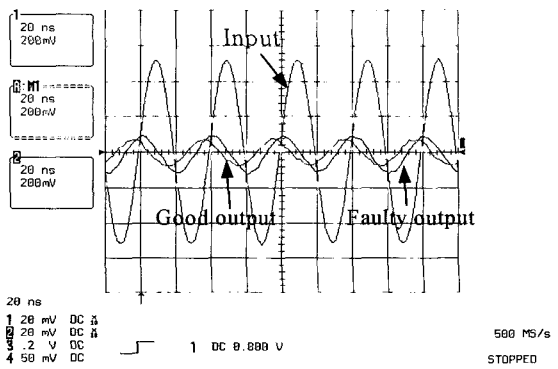
(a)



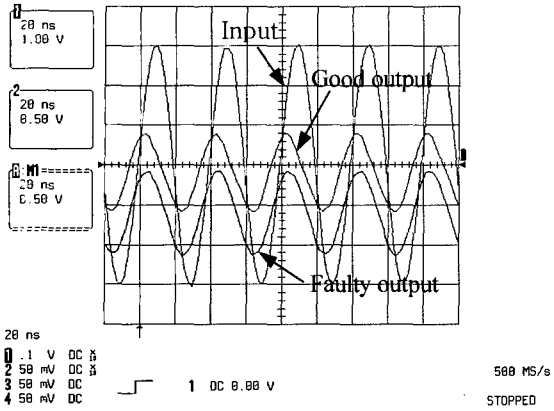
(b)

Fig. 7 Output waveforms for high frequency tesst using the fabricated IC with (a) M1 drain open fault and (b) M1-M2 drain-short fault

Although all faults that can occur in CMOS op-amps have not been simulated in the test IC and tested by the proposed method, we know that these test methods are very effective because the experimental results are very similar to the expected simulation results.



(a)



(b)

Fig. 8 Output waveforms of M5 gate-drain short fault (a) Frequency = 25㎒, Vpp = ±0.5V and (b) Frequency = 25㎒, Vpp = ±3V

VI. CONCLUSION

A new test method was proposed to effectively detect hard and soft faults in CMOS 2-stage op-amps. The proposed method uses a very high frequency sinusoidal signal that exceeds the frequency of ω_{p2} to maximize the fault effect. If the CUT has a fault, its output is not normally a sinusoidal wave but resulting a DC voltage or a distorted signal. But if its output signal is sinusoidal, the voltage level is different from that of a good circuit. Since the proposed test method doesn't require any complex algorithms to generate the test pattern, the time to generate it is short, and therefore, test costs are reduced using a single test pattern for all target faults. The area overhead is also very small because the CUT is converted to a unit gain amplifier using few devices. Using the HSPICE simulation, 100% fault coverage was detected for given hard faults and 84% for soft faults. Experimental results for the fabricated chip have shown that the proposed test method can effectively detect hard and soft faults in CMOS op-amps. Therefore, the proposed method is highly recommended for testing CMOS op-amps.

REFERENCES

[1] Mark Burns and Gordon W. Roberts, An Introduction to Mixed-Signal IC Test and Measurement, Oxford University Press, 2001

[2] Feng Jianhua, SunYihe, Li Shuguo, "Design of Mixed-Signal Circuit for Testability," IEEE Proceedings of ASIC, pp. 616-619, 2001.

[3] David San Segundo Bello, Ronald Tangelder, Hans Kerkhoff, "Modeling a Verification Test System for Mixed-Signal Circuits," IEEE Design &Test of Computers, pp. 63 – 71, Jan.-Feb. 2002.

[4] C. Marzocca and F. Corsi, "Mixed-Signal Circuit Classification in a Pseudorandom Testing Scheme," Proceedings of Online Workshop, pp. 219-225, July 2001.

[5] [5] K. Arabi and B. Kaminska, "Oscillation-test strategy for analog and mixed-signal integrated circuits," *IEEE VLSI Test Symp.*, pp. 476-482, 1996.

[6] [6] A.K.B. A'ain, A.H. Bratt, and A.P. Dorey, "Testing analog circuits by power supply voltage control," *Electronic Letters*, Vol. 30. No. 3. pp. 214-215, 1994.

[7] [7] M. Roca and A. Rubio, "Selftesting CMOS operational amplifier," *Electronic Letters*, vol. 28, no. 15, pp. 1452-1454, 1995.

[8] [8] M. Soma, "Fault coverage of DC parametric tests for embedded analog amplifiers," *IEEE ITC.*, pp. 566-573, 1993.

[9] [9] K. Arabi and B. Kaminska, "Testing analog mixed-signal integrated circuits using oscillation-test method," *IEEE Tran. on CAD.*, vol. 16, no. 7, pp.745-753, 1997.

[10] [10] Gloria Huertas, Diego Vazquez, Eduardo J. Peralias, Adoracion Rueda, and Jose Luis Huertas, "Practical Oscillation-Based Test of Integrated Filters," IEEE Design &Test of Computers, pp. 64 – 72, Nov.-Dec. 2002.

[11] [11] N. Nagi, A. Chatterjee, A. Balivada, and J. A. Abraham, "Efficient multisine testing of analog circuits," *Int. conf. on VLSI Design*, pp. 234-238, 1995.

[12] [12] TTTC Mixed-signal testing Technical Activity Committee. "Analog and mixed-signal benchmark circuits-first release," *IEEE ITC.* pp. 183-190, 1997.

Kang Chul Kim
Received his B.S. and M.S degrees in Electronic Engineering from Sogang University and Ph.D degree in Electronic Engineering for Gyeongsang National University. He worked for ETRI, Samsung Advanced Institute of Technology, Department of Computer Engineering in Jinju National University, and has been an associate professor of Computer Engineering in Yosu National University.

Seok-Bung Han
Received B.S., M.S., and Ph.D degree in Electronic engineering from the Hanyang University, Seoul, Korea, in 1982, 1984 and 1988 respectively. In 1988, he joined the faculty of Gyeongsang National University where he is currently a professor in Department of Electronic Engineering. He was joined RFIC Design Lab. of Cornell University as visiting professor from Dec. 2002 to Dec. 2003. His areas of interest are VLSI Design & Test, RFIC Design & Test, Fault modeling, BIST.