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Stability of Hydrogenated Amorphous Silicon TFT Driver

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Abstract

Gate and data drivers are essential for driving active matrix display. In this study, we integrate drivers with a-Si:H to develop a compact, better reliability and cost effective display. We design and fabricate drivers with conventional a-Si:H thin film transistors (TFTs). The output voltages are investigated according to the input voltage, temperature and operation time. Based on these studies, we propose here a new driver to prevent gate line from the floated state. For the external coupled voltage fluctuation, the proposed driver shows better stability.

Keywords : amorphous silicon, driver, stability, integrated circuit, display

1. Introduction

Hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFT's) have poor electrical property, that is, it displays high threshold voltage and low mobility. Yet, it is considered to be suitable for the pixel addressing elements in active matrix liquid crystal displays (AMLCD's).

Since poly crystalline silicon has high mobility that is sufficient to be used in a driver, it is used for the integrated drivers of LCD. Amorphous silicon integrated circuits have also been studied to achieve cost reduction, fine pitch, compact packaging and reliability [1-8].

In contrast with silicon wafer CMOS process and circuits, a-Si:H TFT shows low hole mobility, making it difficult to implement CMOS circuit due to the lack of P-channel a-Si:H TFT. Furthermore, the depletion type a-Si:H TFT is impossible due to the many defect states. Since only N-channel enhancement type TFT in a-Si:H process can be used, an inverter with N-TFT is generally used for basic logic gate in which a load transistor is an a-Si:H TFT with gate connected to the drain. This type of inverter is inefficient for charging the output node to a positive voltage because output voltage lowering occurs due to the voltage drop at the load transistor.

To overcome low mobility and inefficiency of a-Si:H circuitry, bootstrapping operation is used for a-Si:H TFT circuits [5-6]. The bootstrapping circuits accelerate charging to load capacitor in spite of the low mobility of below 1 cm^2/Vs [6]. In the scheme by Thomson [6], however, the output node is a floating node that is not connected to any voltage source during the non-selection time.

Since floating node is unstable and easily influenced by voltage coupling from other voltage sources, numerous suggestions have been made to prevent the floating. In the case of TFT LCD, the variation of the voltages gives rise to the variation of transmittance; and thus, this voltage variation should be suppressed. To this end, we suggested modifying the circuit to prevent the output node from floating. In the proposed circuit, the output node is connected to a certain voltage source. This proposed scheme can reduce the fluctuation of the gate voltage during off-time.

After designing and fabricating both the conventional and proposed drivers, their characteristics were evaluated and compared. Since the amorphous silicon TFT shows some instability, we investigated the stabilities of a-Si:H TFT drive circuits.

2. Experiments

TFT is an inverted staggered, back-etched type and processed on glass substrate. After cleaning the substrate, a 100 nm thick chrome which is a bottom gate metal was deposited by DC magnetron sputtering. After patterning the

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chrome gate electrode, three layers of the SiNx (400 nm), a-Si:H (150 nm) and n+ a-Si:H (50 nm) were deposited consecutively in a PECVD reactor at the substrate temperature of 280 °C. SiNx was deposited with a mixture of SiH_4 (50 sccm), N_2 (200 sccm) and NH_3 (100 sccm). Undoped a-Si:H was deposited with a mixture of SiH_4 (300 sccm) and H_2 (100 sccm). Then, n+ a-Si:H was deposited with a mixture of SiH_4 (300 sccm) and PH_3 (90 sccm). The n+ a-Si:H layer was used to ensure an ohmic contact between undoped a-Si:H and metal. The active area for TFT was defined by NF_3 plasma etching. A chrome layer (150 nm) for data lines and source/drain electrode of TFTs was deposited by sputtering. After patterning the chrome layer by wet etching, the n+ a-Si:H layer between the source and drain was etched away by NF_3 plasma etching. Silicon nitride was used to form a passivation layer.

Shift registers were designed and the operation of them was evaluated after fabricating them.

3. Results and Discussion

Two kinds of drivers were investigated to verify their stabilities. One of them shown in Fig. 1(a), and the other is shown in Fig. 1(b). Fig. 1 (a) shows the unit drive circuit suggested by Thomson to overcome low mobility and inefficiency of a-Si:H circuitry, and bootstrapping operation was used for this a-Si:H TFT circuits[3]. Output drive ability was achieved by bootstrapping the voltages at the node P. Since the node P is a float, Vp increases simultaneously when output voltage increases and the increase of Vp decrease the on resistance of T3, therefore, rise time of output pulse decreases while maintaining a full output amplitude.

This output becomes the input in the next stage, and the output of this next stage becomes the input for the reset. The reset transistors T2 and T4 become off state after this reset, and lastly, the gate line becomes floated. The gate line is easily affected by the coupled noise due to the floating state.

To reduce capacitive coupling, we added two transistors and one capacitor as shown in Fig. 1(b). After high voltage output to the n-th output node, the output node resets to off voltage by the high voltage input from the next (n+1)-th output node. Reset voltage is the input high

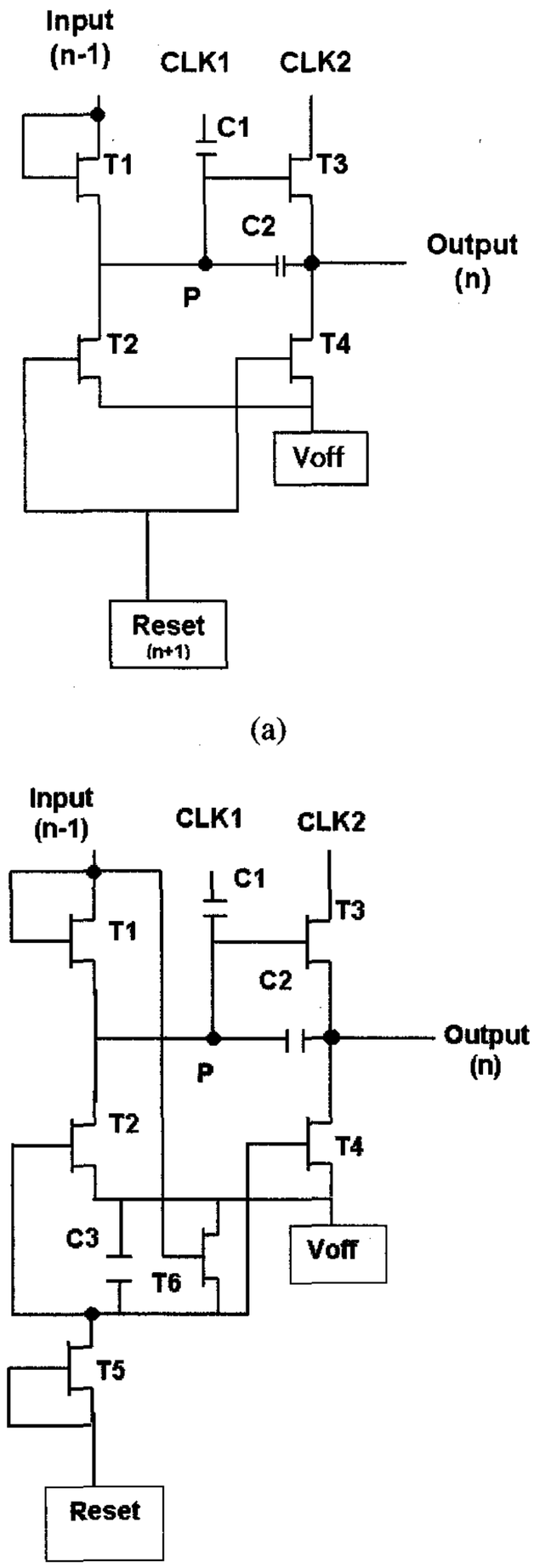
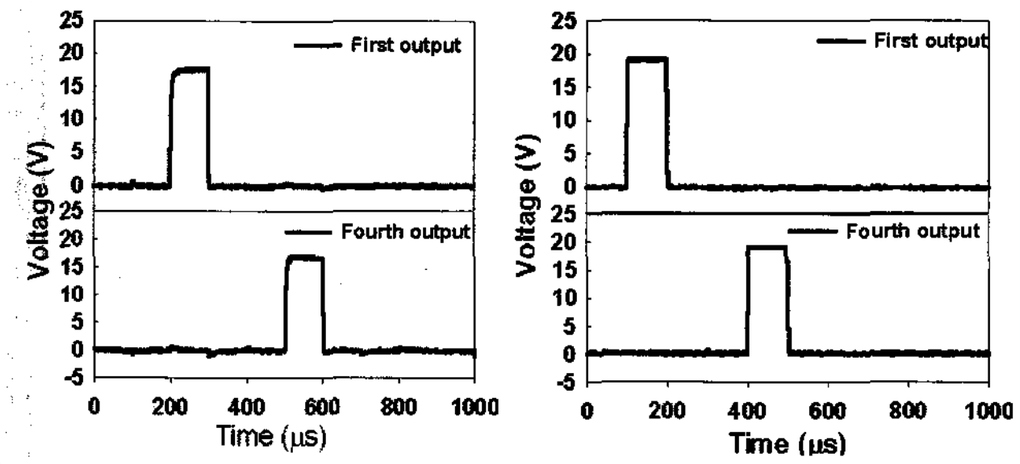


Fig. 1. A circuit diagram of the integrated dirver: (a):the single stage shift register by Thomson and, (b): the proposed shift register by KHU.

voltage from next (n+1)-th output node and switches on the reset transistor T2 and T4. The reset voltage is stored at the capacitor C3 at the same time. The stored reset voltage is applied to the gates of reset transistors T2 and T4 before the next input voltage is transmitted. Therefore, the output node is connected electrically to the off voltage through the reset transistor T4. When the input voltage passes through the input(n-1) port of the circuit, this input voltage is applied simultaneously to the gate of transistor T6 and switches on the transistor T6. Switch-on of T6 results in



(a) (b)

Fig. 2. The output wave forms of the shift registers, (a) : the first and fourth outputs of the shift register of Figs. 1 (a), (b) : the first and fourth outputs of the shift register of Fig. 1 (b).

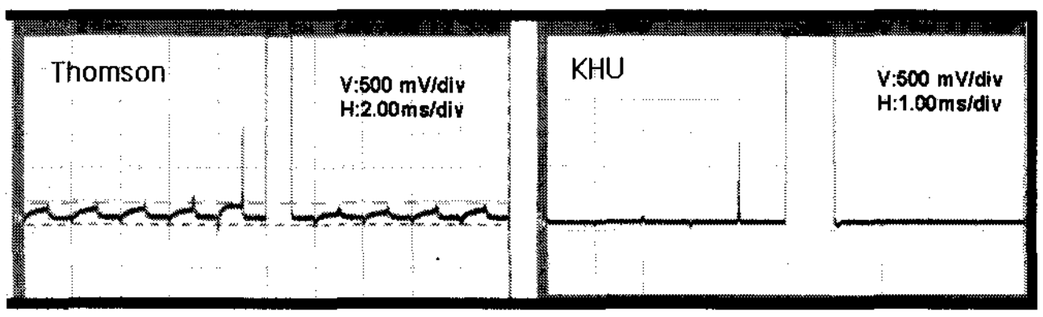
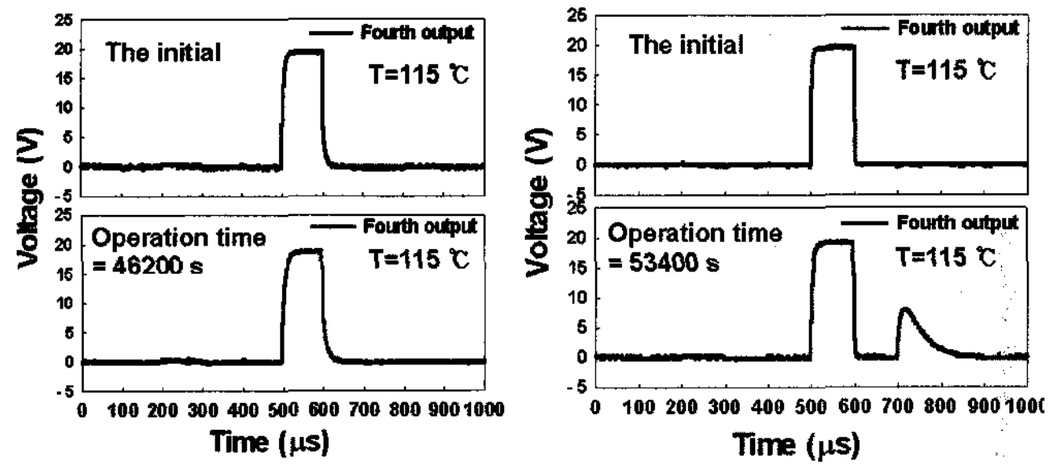


Fig. 3. The effects of light illumination on the drivers. The left is the output of the Thomson type and the right is that of the KHU type. Since the light illumination decreases the off resistances of transistors, the coupling to the other voltage sources increases. Thomson's circuit gives higher coupling to the gate line because it is floating.

discharge of C3 and turns off the reset-transistors T4 and T2. Turning off the reset transistor T4 enables the input voltage to charge up the output node by preventing leakage due to the reset transistor T4.

Fig. 2 shows the outputs of both the Thomson type driver and the KHU (Kyung Hee University) type. The first and fourth stage outputs are shown. The clock and input start pulse were 20 V. Fig. 2 (a) is the output of the Thomson type and (b) is that of the KHU type. The KHU shows less noise at the low voltage as the floating is prevented.

Fig. 3 shows the outputs of the drivers while illuminating the light on the drivers. Since the photo conductivity is high in the amorphous silicon, off-resistances of the a-Si:H transistors decrease. This decrease results in the increase of coupling to the other voltage sources, especially to the clocks. The thomson type shows larger coupling effect compared to the KHU. Since the output node is connected to the off-voltage source in the KHU type, the output node is more stable than Thomson's style.



(a) (b)

Fig. 4. The outputs of the driver after continuous operation with a clock and input start pulse width 100 μs and input start pulse period of 3.2 ms: (a) : Thomson type and (b) : KHU type.

Fig. 4 (a) and (b) show the outputs after some operation time elapsed. The temperature was as high as 115 ℃ when for the acceleration of stability test was conducted. Since the threshold voltage of the amorphous silicon TFT changes during the bias stress[10], the output waveform changes after prolonged operation. The width of the start pulse was 100 μs and the period was 3.2 ms, which means the output width was also 100 μs and the period was 3.2 ms.

Fig. 4(a) shows the outputs of the Thomson type. The upper part shows the output before the prolonged operation, and the lower one shows the output after the operation has progressed for 46200 s. The rise time increased from 9.0 μs to 15.0 μs and the fall time increased from 11.0 μs to 14.2 μs. The output voltage decreased from 19.4 V to 18.8 V. Since the positive gate bias stress increases the threshold voltage of a-Si:H TFT, the on-resistance of TFT also increases. The increase of on-resistance results in the increase of rise and fall time, but decreases the output voltage.

Fig. 4(b) shows the output of the KHU type. The upper part shows the output and the lower shows the output after the operation has progressed for 53400 s. The rise and fall time increased from 5.0 μs, and 2.0 μs to 10.0 μs and 4.0 μs, respectively. The output voltage decreased from 19.7 V to 19.2 V. After the operation ran for 53400 s, the second small pulse was observed after a pulse width later. This abnormal second pulse is attributed to the threshold voltage increase of the reset transistor T2.

In the case of Thomson type, the applied time of the gate voltage to the reset transistor is relatively short because the gate voltage is high only when the gate line is selected. However, in the case of KHU type, the gate

voltage to the reset transistor remains relatively long because the gate voltage is high even during even the non-selection time of gate line. Therefore, threshold voltage shift is relatively larger due to the longer gate voltage stress and the increase of the on-resistance of reset transistor.

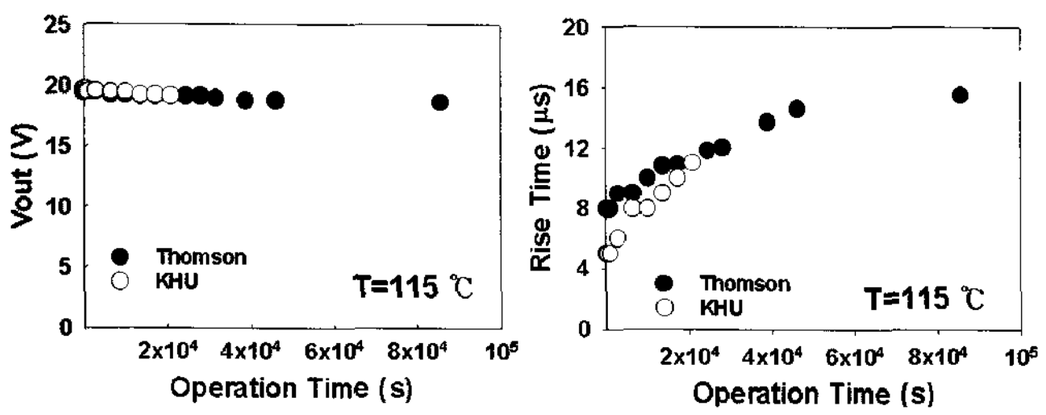
Due to the increase of on-resistance, the voltage at the node P is not completely discharged. In fact, some amount of voltage remains. Due to this small voltage, T3 is not at a perfect off-state. Therefore, the small output voltage appears at the output node during the next rise of the clock voltage on T3. The small pulse disappear at the next rise of the clock voltage on T3 because the remaing voltage of the node P is discharged out during this.

To increase the life time of the driver, the insufficient discharge at the node P during the reset should be prevented. One way is by improving the TFT stability and the other is widening the channel width of the reset transistors. By doing so, we can keep the on-current high enough for the discharge, even when the threshold voltage increases.

Fig. 5 shows the time dependence of V_{out} and the rise time on the operation time. Output pulse to a gate line of TFT LCD switches on all pixel transistors connected to the gate line. If another peak appears again as shown in Fig. 4, this peak voltage is applied to the gate line during the off-time of gate line. For this reason, the measurement was discontinued when the second pulse voltage reached 10% of V_{out}.

As the threshold voltage increases with operation time, the V_{out} decreases while the rise time increases. In terms of rise time, T3 and T1 are important. The average bias between the gate and the source of T1 is negative if the input voltage is low while the node P is boosted up. The negative gate voltage pulses decrease the threshold voltage of the T1. But, the threshold voltage of T3 increases because of the average plus voltage between the gate and the source. Therefore, the threshold voltage increase of T3 is a major cause for the increase in the rise time during the operation.

Output voltage decrease is similar for both types of drivers. The rise time of the KHU was relatively shorter than the Thomson and this rise time increases as a time of operation. The measurement was discontinued at around 2 $\times 10^4$ s due to the appearance of the tail pulse. To avoid the tail pulse, we should increase the width of the T2 transistor, which in turn causes the on current to increase even with the increase of the threshold voltage.



(a) (b)

Fig. 5. (a) : Vout changes with operation time. Vout decreases as the threshold voltage of the TFT increases with operation time. (b) : rise time changes with operation time.

4. Conclusion

We proposed a new a-Si:H TFT driver to prevent the output node from floating. The proposed circuit was designed and fabricated through the conventional a-Si:H TFT process. In addition, by adding the storage capacitor and control transistors, we achieved electrical connection of the output node to an off state voltage during non-selection time. We then compared the coupling effects on the output nodes, and the measurement showed that our proposed circuit fluctuated less than the conventional one. In that respect, the proposed circuit is not influenced by the couple external fluctuation of voltage. However, small additional pulse was observed after a prolonged operation time at the proposed driver, and this is attributed to the insufficient discharge at the node P caused by the increase of on resistance of reset transistor. To overcome this limitation, we suggested widening the channel width of the reset transistor. As the operation time increased, the rise time increased while the output voltage decreased. We also verified that the threshold voltage change of T3 is the primary factor that ensure stability of the driver.

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