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New Dynamic Logic Gate Design Method for Improved TFT Circuit Performance

Ju Young Jeong* **and Jae-Geun Kim****

Abstract

We explored a new way of designing dynamic logic gates with low temperature polysilicon thin film transistors to increase the speed. The proposed architecture of logic gates utilizes the structural advantage of smaller junction capacitance of thin film transistors. This method effectively blocks leakage of current through the thin film transistors. Furthermore, the number of transistors used in logic gates is reduced thereby reducing power consumption and chip area. Through HSPICE simulation, it is confirmed that the circuit speed is also improved in all logic gates designed.

Keywords : thin film transistor, logic gate, SOI, simulation

1. Introduction

The improvement of the characteristics of thin film transistor (TFT) on low temperature polysilicon (LTPS) ushers flat panel display into the digital system area. More functions such as driver IC, timing controllers, etc., have been designed and integrated into the active matrix LCD panel with LTPS TFT's [1~3]. Previously, these functions were implemented by a single crystal silicon VLSI's which were attached to the display panel by flip chip bonding or similar techniques. These single crystal silicon VLSI's are expensive and takes a long time to fabricate since they are designed and fabricated by separate semiconductor manufacturers. Moreover, as the flat panel display resolution increases, more connections are needed between the VLSI's and display panel, and thereby raising new challenges in terms of reliability [4~5].

The concept of system-on-panel (SOP), which integrates digital and/or analog circuits at the periphery of flat panel displays, emerged as a feasible solution to resolve the above-mentioned problems associated with single crystal silicon VLSI's. Basic SOP contains display area as well as driving circuit blocks as shown in Fig. 1. It is composed of driver IC's[6], timing controller, image scaler, and memory built inside the display panel by using LTPS TFT's. A more complex SOP may include more complex digital block such as microprocessors, digital signal processing engine, etc [7~9].

A key ingredient of the SOP is high performance TFT. Recently, many display manufacturers have reported low temperature polycrystalline silicon (LTPS) TFT's with electron mobility higher than 100 cm^2/V-sec. Even though this is much higher than that of amorphous silicon TFT's, it is still not high enough to implement high speed logic blocks like timing controller, image scaler, etc. Therefore,

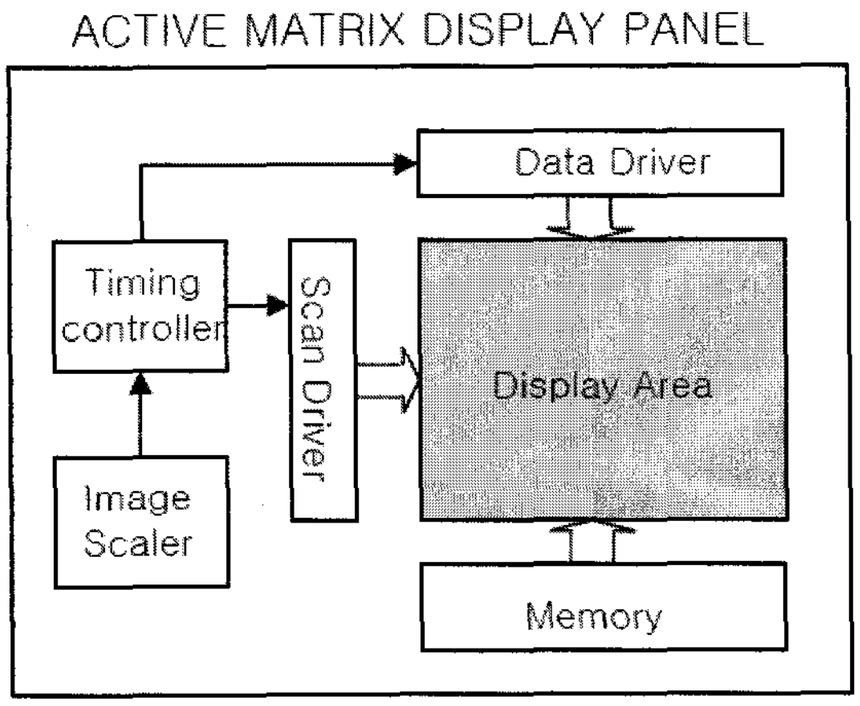

Fig. 1. Block diagram of basic SOP.

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* Member, KIDS; ** Student Member, KIDS.
Corresponding Author : Ju Young Jeong
Dept. of Electronics Engineering, The University of Suwon San 2-2 Wau-ri, Bongdam-eub, Hwasung-si, Kyongki-do 445-743, Korea.
E-mail : jyjeong@suwon.ac.kr **Tel** : +31 220-2168 **Fax** : +31 220-2494

there is need to find a way to design faster TFT Logic circuit with given TFT properties [2~4].

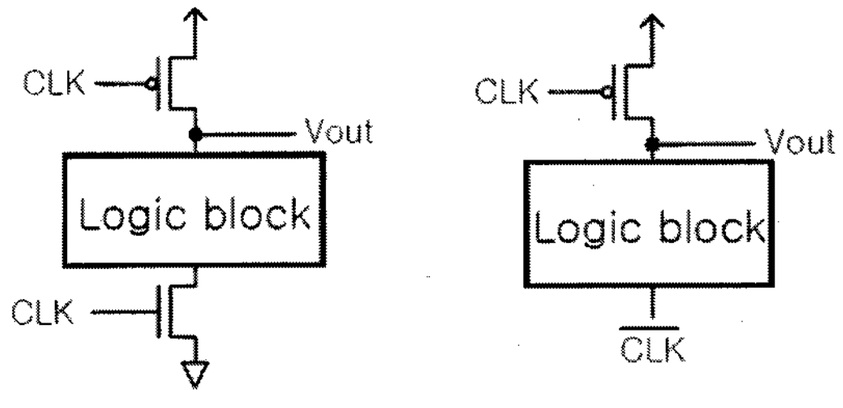
In this paper, we propose a new dynamic digital logic called "clocked ground logic". This circuit style takes advantage of partially depleted SOI MOSFET properties which the LTPS TFT's share. The discussion of this paper will progress as follow. In Section 2, we will discuss the idea of new design style from a device characteristics point of view. In Section 3, we will present dynamic inverter designed with the clocked ground logic and discuss the advantages gained. Then, we will present the performance of various dynamic logic gates in terms of power consumption, speed, and leakage current.

2. Clocked Ground Logic for TFT Dynamic Logic Design

Currently, most TFT circuits implemented in display panel follow identical design style as bulk MOSFET circuits. However, in principle, TFT is a partially depleted silicon-on-insulator (PDSOI) MOSFET device with poor mobility. The PDSOI MOSFET's have infamous floating body effect (FBE) [10], yet have much smaller junction capacitance compared to bulk MOSFET's. Therefore, we studied about circuit architectures that can reduce the FBE-related leakage current by taking advantage of smaller junction capacitance.

The most serious problem generated by FBE is undesirable current flow from intermediate or output node to the ground. In dynamic logic, output node is charged to logic high during the precharge period and leakage current can flow in the pull-down path. Since all logic gates enter the precharge period simultaneously, the sum of the leakage current can become significant especially in the case of devices with poor turn off characteristics such as LTPS TFT. This leads to larger DC power consumption as well as logic state change errors in TFT circuits.

In addition, there is the floating body effect in TFTs due to insufficient depletion of its channel during operation. When carriers are accumulated in the channel, that is electrically floating, it can turn on TFTs, causing significant erroneous currents to flow through the device and consequently causing logic error in the system. This FBE-related failure or current flow is observed in TFT's when the potential difference between drain and source is large.



(a) (b)

Fig. 2. Architectures of dynamic logic gates. (a) conventional dynamic logic and (b) clocked ground dynamic logic.

To prevented the above-mentioned problems from occuring and to reduce the chip size, we propose here a clocked ground logic design style for dynamic logic gates made of TFTs. The conventional dynamic gates contains a header PMOSFET and a footer NMOSFET connected to the clock signal as shown in Fig. 2 (a). Logic block is located between the header and the footer. When the output of the logic gate is high, the footer NMOSFET becomes susceptible to the leakage current, possibly resulting in the output voltage to drop erroneously.

The clocked ground logic is shown in Fig. 2 (b). It does not contain the footer NMOSFET. Instead, the clock signal, which is complementary to the PMOSFET gate input, is applied to the bottom of logic block. With this configuration, no leakage current path exists during precharge where clk signal is logic zero. Since there is no current path during the precharge period, there is no FBE-related current flow during this period, making the circuits to be more reliable. This architecture takes advantage of very small source drain junction capacitance in TFT's and thus is not practical for bulk MOSFET circuits where the junction capacitance is large. With regards to the /clk signal, one can use conventional logic ground metal line to deliver and no additional /clk signal generator is required for systems that use multi-phase clocking.

3. Circuit Performance of the Clocked Ground Logic Gates

For the conventional dynamic inverter (Fig. 3 (a)), M3 is turned off during the precharge period where CLK is logic low. But if Vin is high, leakage current can flow through M3 due to the floating body effect. On the other

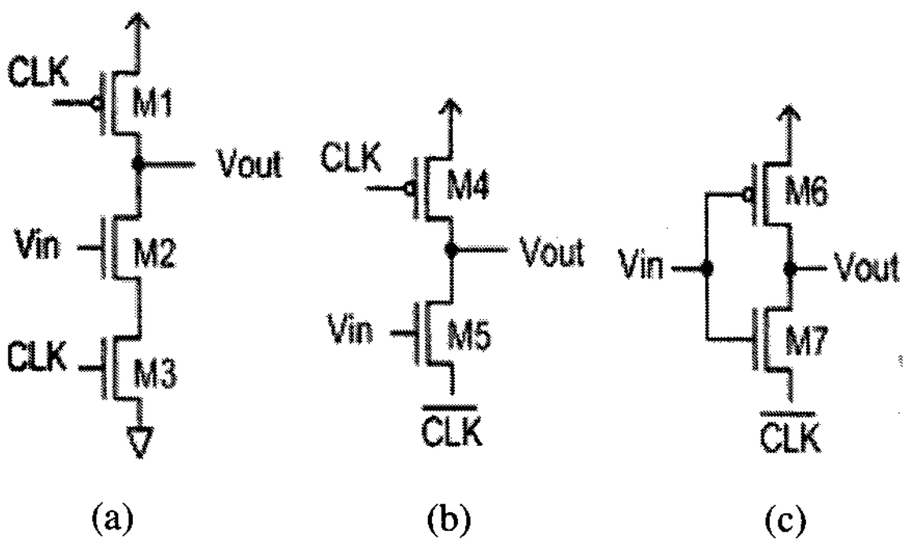
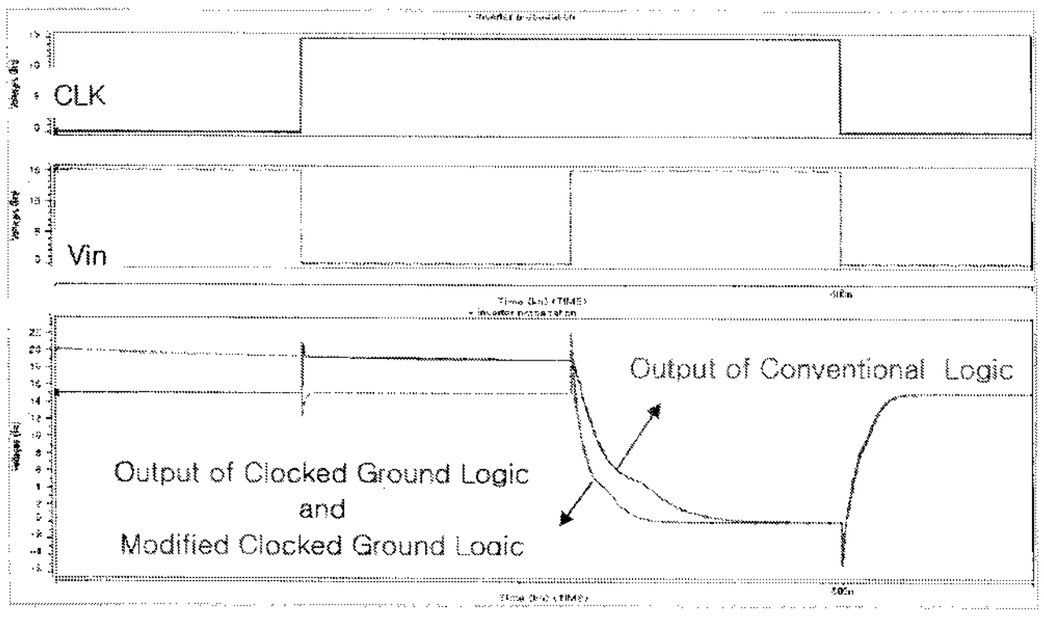
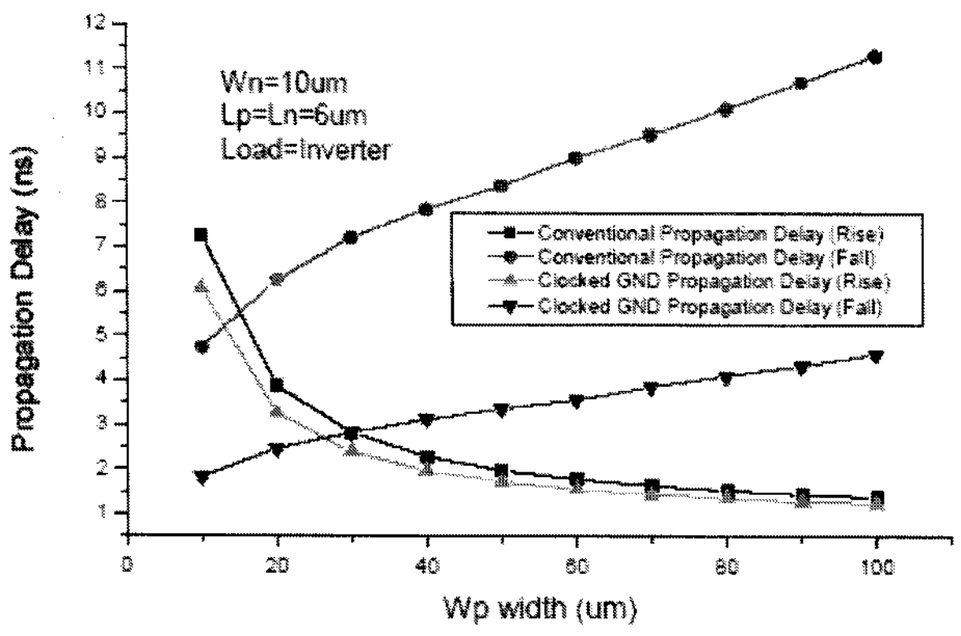


Fig. 3. (a) Conventional dynamic inverter, (b) Clocked ground dynamic inverter, and (c) Modified clocked ground dynamic inverter.



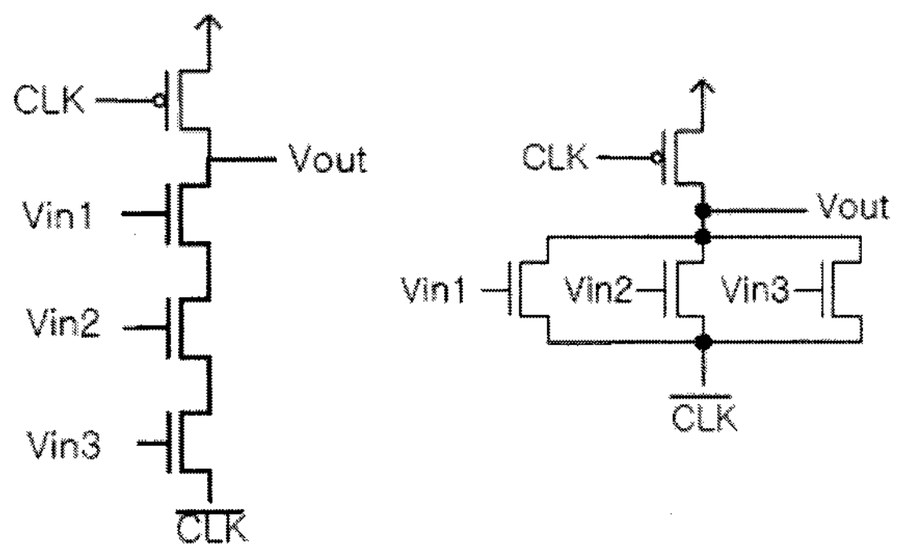
(a)



(b)

Fig. 4. (a) Pull-down and pull-up characteristics of conventional inverter and two types of the clocked ground inverters, (b) propagation delay of conventional and clocked ground inverters for various pTFT width.

hand, in the clocked ground dynamic inverter in Fig. 3 (b), the leakage current can be effectively reduced using smaller number of MOSFET's. During the precharge period, the



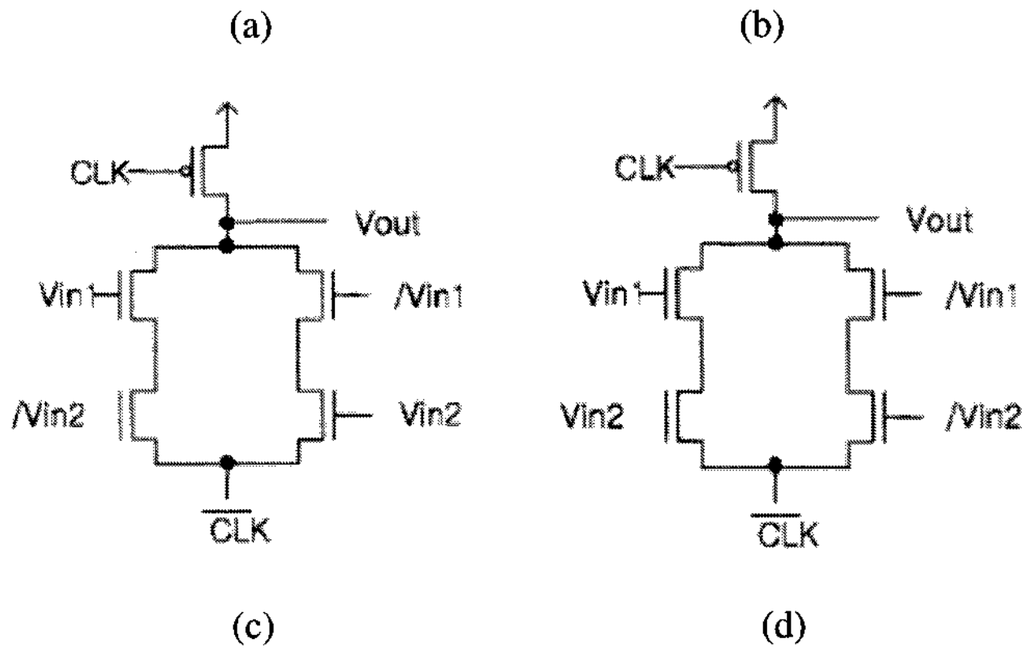
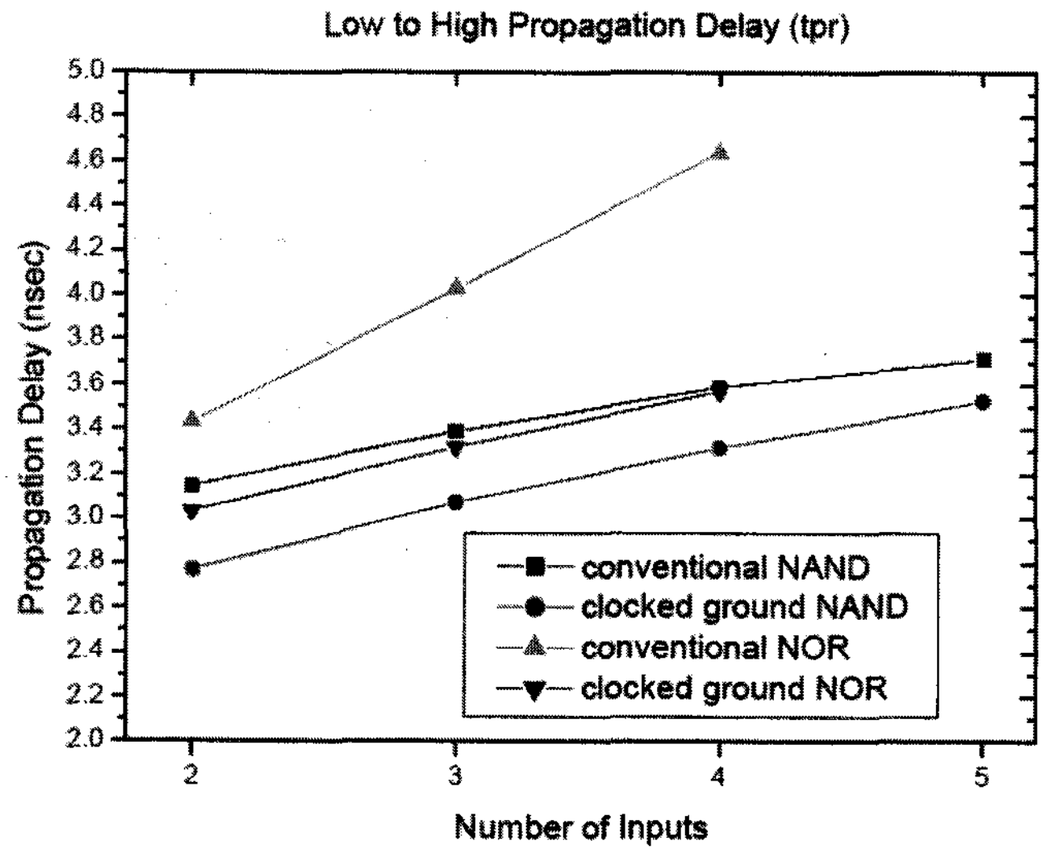


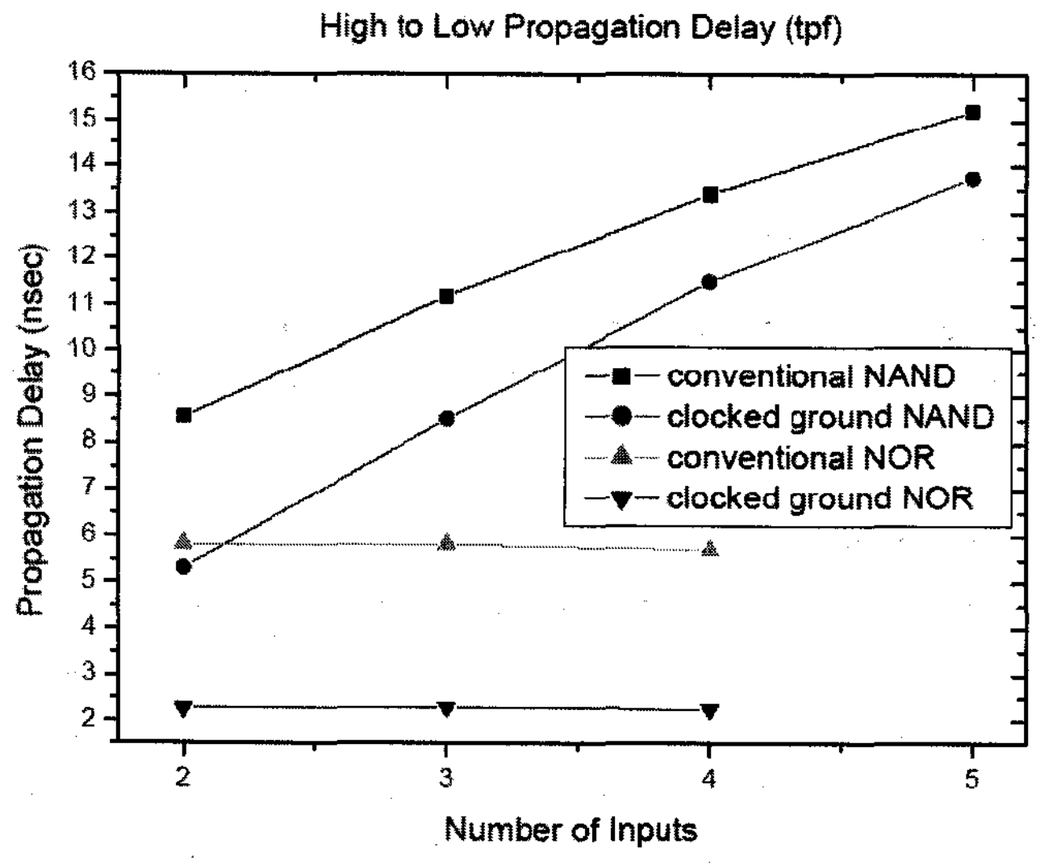
Fig. 5. Various clocked ground logic gate schematics. (a) three input NAND gate, (b) three input NOR gate, (c) two input XOR gate, and (d) two input XNOR gate.

source of M5 is high and no leakage current can occur. This configuration is more attractive since it uses one less MOSFET than the conventional case. Fig. 3 (c) shows a modified clocked ground dynamic inverter with less control interconnects. During the precharge period, the output node is charged to high. If Vin is high, the output become charged to high through M7 since /clk signal is high during precharge. When Vin is low, the output is charged to high (Vdd) through M6.

To probe the circuit performance, we performed HSPICE simulation by RPI TFT model. The model parameters were extracted from measurement data of 6 um channel length TFT's. Fig. 4 (a) shows the simulated waveform of dynamic inverter gates as in Fig. 3. the output waveform of the clocked ground dynamic inverter and the modified clocked ground dynamic inverter is almost identical as expected. Compared with the conventional inverter, the pull down delay of the gate is improved from 6.4 ns to 2.5 ns in the clocked ground inverter. On the other hand, pull up delay remains the same. The pull down characteristic improvement is further enhanced for larger



(a)



(b)

Fig. 6. Propagation delay characteristics of clocked ground NAND and NOR gate as a function of input numbers (a) low to high propagation delay (tpr), (b) high to low propagation delay (tpf).

pTFTs as shown in Fig. 4 (b).

We designed various clocked ground logic gates and tested them. The schematics of certain gates are shown in Fig. 5 and their HSPICE simulation results of propagation delay in comparison with the conventional logic CMOS dynamic gates are summarized in Fig. 6 and Table 1. All the gates can be seen to have identical load of CMOS inverter with Wp = 2Wn = 20 um and L = 6 um. In this figure, tpr stands for propagation delay of output node

Table 1. Performance comparison of XOR and XNOR gates

Conventional Circuit				
	tpr (ns)	tpf (ns)	tr (ns)	tf (ns)
XOR 2	2.633	9.049	6.405	25.259
XNOR 3	3.515	11.794	7.47	25.255

Clocked Ground Circuit				
	tpr (ns)	tpf (ns)	tr (ns)	tf (ns)
XOR 2	2.688	5.577	6.33	16.073
XNOR 3	2.012	6.535	5.684	16.074

Table 2. Leakage current of conventional and clocked ground logic gates

	Conventional Logic Leakage Current (nA)	**Clocked Ground Logic Leakage Current (nA)**	**Chip Area Ratio (Clocked Ground / Conventional)**
Inverter	**166.5**	**40.5**	**0.67**
3 input NAND	**349.7**	**127.1**	**0.52**
3 input NOR	**117.5**	**15.9**	**0.73**
2 input XOR	**85.9**	**41.6**	**0.85**
2 input XNOR	**86.0**	**27.6**	**0.84**

charging while tpf stand for propagation delay of output node discharging. Also, tr and tf stand for rise and fall time of the output node, respectively. From Fig. 6, it is clear that the output discharging propagation delays of the clocked ground logic are superior to those of con-ventional logic in all cases. Note that the device sizes are identical for conventional and clocked ground logic. A more significant improvement in performance was observed in NOR gate. For conventional dynamic logic style, footer NMOS showed a bottle neck of output node discharging when multiple NMOSFET's in pull down path were turned on. This explains why the output discharging propagation delay is proportional to the number of inputs as shown in square symbols in Fig. 6 (b). However, for the clocked ground

NOR gates, there is no footer NMOSFET and therefore, discharging is more efficient.

Another important advantage of the clocked ground logic is that the leakage current is reduced. We took five gate types and measured the peak leakage current as shown in Table 2. As expected, the leakage current reduced significantly in clocked ground logic in all five test circuits. However, the three input NAND gate's leakage current was higher than we expected. We had initially assumed that the leakage current would be very low as the gate has three NMOSFETs connected in series. We believe that the high leakage current is due to the floating body effect because this gate has floating node in the pull down path and is more susceptible to excessive leakage current. However, even in this case, the clocked ground logic NAND showed a much lower leakage current than the conventional one.

4. Conclusion

We proposed a new dynamic logic design method suitable for TFT's with low junction capacitance. By using extracted TFT device parameters and HSPICE simulation, we verified that the new method provides faster circuit with lower leakage current. Among the various gates that were tested, NOR gates exhibited the best performance improvements.

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