A Low Dark Current CMOS Image Sensor Pixel with a Photodiode Structure Enclosed by P-well

Sang-Wook Han, Seong-Jin Kim and Euisik Yoon

Abstract—**A low dark current CMOS image sensor (CIS) pixel without any process modification is developed. Dark current is mainly generated at the interface region of shallow trench isolation (STI) structure. Proposed pixel reduces the dark current effectively by separating the STI region from the photodiode junction using simple layout modification. Test sensor array that has both proposed and conventional pixels is fabricated using 0.18μm CMOS process and the characteristics of the sensor are measured. The result shows that the dark current of the proposed pixel is 0.93fA/pixel that is two times lower than the conventional design.**

Index Terms—**CMOS image sensor, low dark current, photodiode enclosed by P-well, isolation of junction from STI**

I. Introduction

CMOS image sensors are attractive devices because of their advantages, such as ability of on-chip signal processing, low cost and low power consumption [1]. However, the high dark current problem compared with CCD prevents CIS from being a prevailing technology for high-end applications. It is well known that the dark current is mainly generated from the interface defects that are located at the side of STI region and the depletion region of the photodiode edge at the surface [2]-[5]. There have been many efforts to reduce the dark current of CIS pixels. Although the pinned photodiode [5]-[7] shows a superior dark signal characteristic, it requires additional complex processes that may increase the cost and reduce the yield. With minimum process modification, a low dark current 3 transistors (3T) pixel has been developed [4]. Also without any process modification, a low dark current 3T pixel using n+ ring reset was reported [2]. They could reduce dark current effectively however the conversion gain may be decreased due to the large overlap capacitance between the reset ring gate and the photodiode.

In this paper we will report a 3T-based low dark current pixel without any process modification and without sacrifice of conversion gain. Proposed pixel can be implemented by using simple layout modification. Measurement results of test image sensor that adopts proposed pixels show a superior dark current characteristic without any other significant performance degradation.

II. Pixel Structure

As the pixel size is getting smaller, the total dark current of photodiode is more affected by the perimeter component than the area one. Therefore, it is becoming more important to minimize the dark current generated at the perimeter. Manly the perimeter component of a photodiode dark current is generated from the interface defects that are located at the contact region between photodiode junction and STI. It has been shown that the separation of the depletion region from the STI reduces the dark current efficiently in [2], [4], [5].

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Dept. EECS, Korea Advanced Institute of Science and Technology 373-1 Gusung-dong Yusong-gu, Daejon 305-701, Korea.
E-mail : swhan@iml.kaist.ac.kr

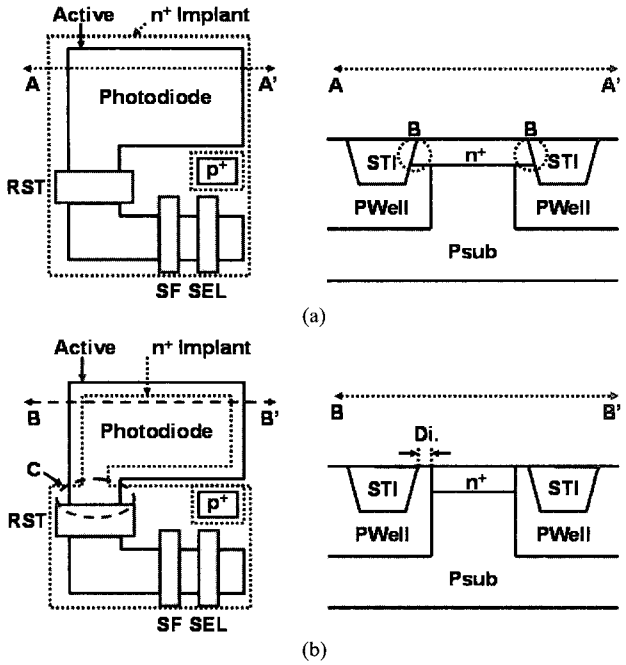


Fig. 1. Active pixel based on 3 transistors layout of (a) conventional and (b) proposed structure

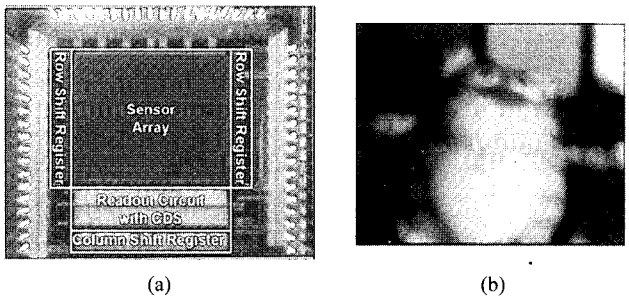


Fig. 2. (a) Microphotograph of 352×288 test sensor and (b) sample image from the test sensor

Figure 1 illustrates the conventional and proposed pixel structure. We just modify the layout in a way that the n+ implant mask is enclosed by the active region. This modification prevents the depletion region of photodiode from contacting the STI region without any process modification. Because the STI region is enclosed by PWell, electrons thermally generated at the side of STI region are recombined with the majority carriers of PWell. Therefore the photodiode n+ sensing node voltage is not affected. In the region C in Fig. 1 the active mask does not enclose the n+ implant mask due to the reset transistor gate poly implantation that causes the photodiode to contact the STI region. However, the effect of this region is not significant because it takes only little portion of the total photodiode perimeter. The proposed pixel sacrifices a photodiode fill factor by a small amount as shown in Fig. 1. But optical fill factor is not changed and the conversion gain, on the contrary, is increased, therefore the sensitivity is not affected significantly.

III. Fabrication and Measurement Results

To verify the proposed pixel performance, a 352×288 sensor array has been designed and fabricated using 0.18μm 1P4M CMOS logic process as shown in Figure 2(a). The test sensor is composed of sensing array, row and column shift register, correlation double sampling circuit and chip amplifier. The sensor is divided into several different arrays for various testing. The size of proposed pixel is 3.6μm×3.6μm and the array size for imaging is 130×84. Figure 2 (b) shows the image from proposed pixel array.

Fig. 3 shows the readout path of a test CIS sensor including propoed pixel structure. Because the pixel size is small, it is difficult to accommodate a column parallel CDS circuit in a small column pitch. Thereofore we have devised that simple and area-efficient CDS circuit as

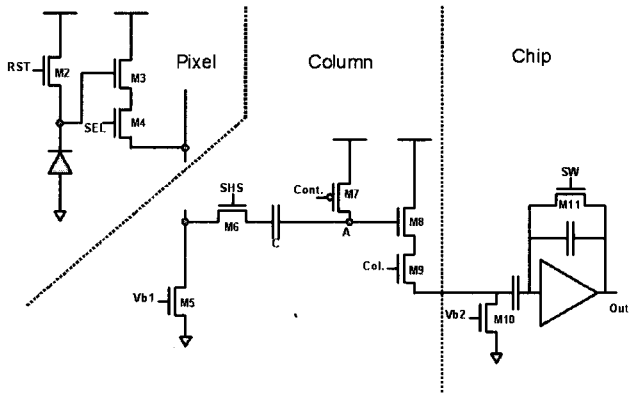


Fig. 3. Readout path of a test CIS sensor including the proposed pixel structure

shown in the Fig. 3. Because this CDS scheme uses only one sampling capacitor, it can be compactly implemented in a small column pitch.

The operation timing of the sensor is shown in Fig. 4. Pixel FPN, which is manly caused by the mismatches in reset and source follower transistors in each pixel, can be

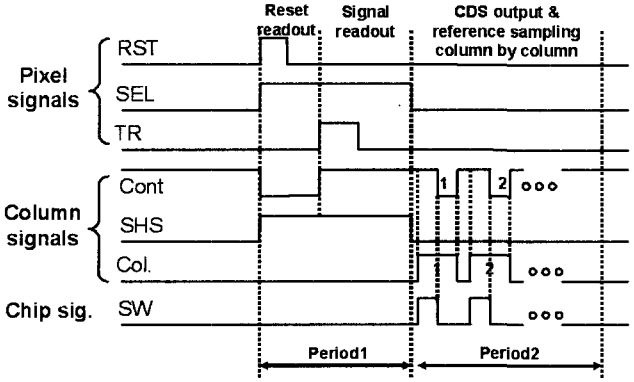
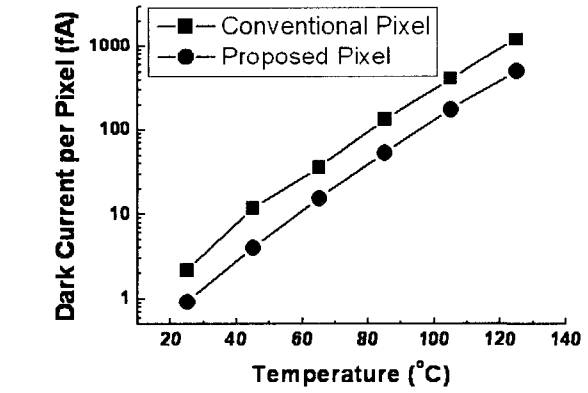
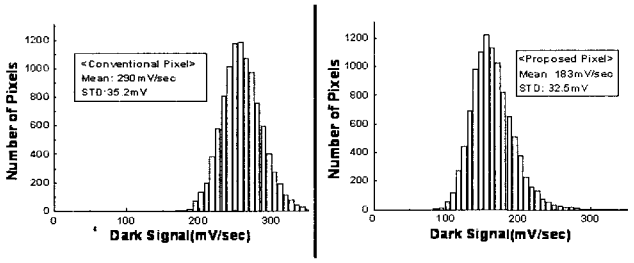


Fig. 4. Operation timing diagram for the test sensor

removed by the double sampling during period 1. Column FPN that results from a CDS circuit mismatching can be also eliminated by the operation of a switched capacitor amplifier as follows. After the stored voltage (V_A) at the node A is read, it is reset to the reference voltage V_{DD}. In this case, V_A has the difference between the pixel reference voltage and a signal value. Next, the reference voltage is read and subtracted from the V_A. Because the both readout signals, i.e. the reference and V_A include the same offset of a CDS circuit, the final output of chip amplifier has the offset free characteristic. These operations are



(a)



(b)

Fig. 5. Measurement results of (a) dark current vs. temperature and (b) histogram of dark signal

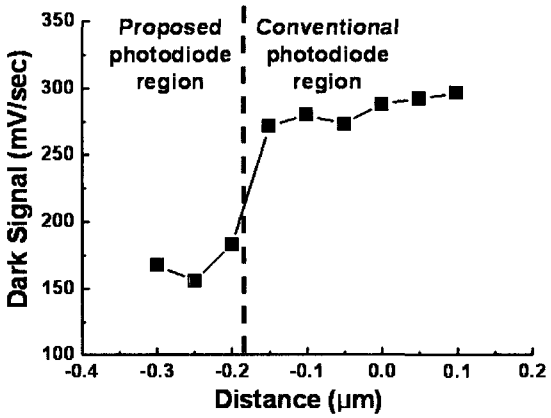


Fig. 6. Dark current results vs. the distance (Di) that is between the n+ implant and active mask

Table. 1. Test sensor characteristics

	Conventional	Proposed
Process	0.18um 1P4M CMOS	
Pixel	3.6μmX3.6μm, 3T	
Array Size	130X84	
Saturation Level	0.84V	
FPN (Excluding dark)	0.46%	
Photodiode Perimeter	10.16 (μm)	8.72 (μm)
Optical Fill Factor	6.32um² (48.8%)	5.53um² (42.7%)
Dark Current (@ 25°C)	2.18 (fA/pixel)	0.93 (fA/pixel)
Conversion Gain	23(μV/e-)	30(μV/e-)
Sensitivity	0.55 (V/lux·sec)	0.48 (V/lux·sec)

consecutively executed column by column.

By on-chip probing the dark current has been measured as shown in Figure 5 (a). At 25°C, the dark current of the proposed pixel is 0.93fA/pixel that is two times lower than the conventional design, 2.18fA/pixel. In overall range of temperature, proposed pixel shows the superior dark current characteristic. On the other hand, the variation of the dark current level from the test sensor arrays is similar to that of the conventional one, while the average dark current level is less than the conventional one as shown in Figure 3 (b).

In the proposed pixel structure, the distance between active and n+ implant mask (Di shown in Figure 1) is important because it significantly affects the amount of dark current. Figure 6 shows the relation between the dark signal and Di. In the graph, there is an abrupt transition between -0.15μm and -0.2μm. This means that the design

margin not to contact between STI and photodiode junction of the fabricated process is about -0.2μm. If the distance is longer than -0.2μm, it is expected to reduce dark current more. However it may also results in a low photodiode fill factor. Therefore we need to compromise between the two. For the imaging array, we have chosen Di as -0.2μm. The characteristics of the test sensor are listed in Table 1. The photodiode perimeter of the proposed pixel is 85% of the conventional one; on the contrary, the dark current is two times lower.

IV. CONCLUSIONS

A low dark current CIS pixel without any process modification has been fabricated and characterized successfully. The separation of STI from the photodiode region that can be done by a simple layout modification makes the dark current be reduced. The proposed pixel shows a dark current two times lower than the conventional one without significant sacrifice of fill factor and sensitivity. The proposed pixel can be applied for low cost and high performance CIS applications.

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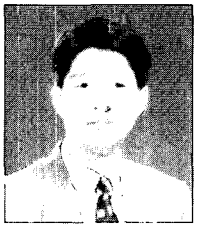
Sang-Wook Han He was born in Seoul, Korea, in 1975. He received the B.S. and M.S degrees from Korea Advanced Institute of Science and Technology (KAIST) in 1999 and 2001 respectively. He has been working toward Ph.D. degree at KAIST. His current research interests include CMOS image sensor, fingerprint sensor, tactile sensor, embedded image processor and computer arithmetic unit design.

Seong-Jin Kim He was born in Seoul, Korea, in 1978. He received the B.S. degree in electrical engineering from POSTECH (Pohang University of Science and Technology), Pohang, Korea, in 2001, and the M.S. degree from KAIST. He is currently pursuing the Ph.D. degree in KAIST (Korea Advanced Institute of Science and Technology), Daejon, Korea. His current research interests include image processor, CMOS image sensor and VLSI system design.



Euisik Yoon He received the B.S. and M.S. degrees in electronics engineering from Seoul National University in 1982 and 1984, respectively, and Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, in 1990. From 1990 to 1994 he was with the Fairchild Research Center of National Semiconductor Corp., Santa Clara, CA, where he was engaged in researches on deep submicron CMOS integration and advanced gate dielectrics. From 1994 to 1996 he was a Member of Technical Staff at Silicon Graphics Inc., Mountain View, CA, working on the design of the MIPS microprocessor R4300i and the RCP 3-D graphic coprocessor. In 1996 he joined the Department of Electrical Engineering at Korea Advanced Institute of Science and Technology (KAIST), Taejon, Korea, where he is now an associate professor. His present research interests are in MEMS, integrated microsystems, and VLSI circuit design. Dr. Yoon was the co-recipient of the Student Paper Award at the IEEE International Microwave Symposium in 1999 and 2000, respectively, concerning the topics on MEMS inductors and RF MEMS switch work. He served in various Technical Program Committees including Microprocesses and Nanotechnology Conference, International Sensor Conference and IEEE AP ASIC Conference. Currently, he is serving in IEEE ISSCC program committee and Transducers technical program committee.