A Design Evaluation of Strained Si-SiGe on Insulator (SSOI) Based Sub-50 nm nMOSFETs

Muhammad Nawaz* and Mikael Östling**

***Abstract*—A theoretical design evaluation based on a hydrodynamic transport simulation of strained *Si-SiGe* on insulator (*SSOI*) type nMOSFETs is reported. Although, the net performance improvement is quite limited by the short channel effects, simulation results clearly show that the strained *Si-SiGe* type nMOSFETs are well-suited for gate lengths down to 20 *nm*. Simulation results show that the improvement in the transconductance with decreasing gate length is limited by the long-range Coulomb scattering. An influence of lateral and vertical diffusion of shallow dopants in the source/drain extension regions on the device performance (i.e., *threshold voltage shift, subthreshold* slope, current drivability and transconductance) is quantitatively assessed. An optimum layer thickness (t_{si} of 5 and t_{sg} of 10 *nm*) with shallow junction depth (5-10 *nm*) and controlled lateral diffusion with steep doping gradient is needed to realize the sub-50 *nm* gate strained *Si-SiGe* type nMOSFETs.**

***Index Terms*--Strained Si-nMOSFETs, Device Simulation, Strained Si-SiGe nMOSFETs, Nanoscale nMOSFETs, Device Modelling**

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*Solid State Device Laboratory, IMIT, Royal Institute of Technology (KTH), SE-16440 Kista, Sweden
**Infineon Technologies Sweden AB, Isafjordsgatan 16, SE-16481 Kista, Sweden
E-mail : muhammad.nawaz@infineon.com

I. Introduction

Because of excellent carrier transport enhancement properties over *Si*-control devices, introducing strained-*Si* and *SiGe* into MOSFETs has led to much interest recently [1- 6]. A thin layer of silicon pseudomorphically grown on a relaxed *SiGe* layer, produces a tensile strain in the *Si* layer which lifts the 6-fold degeneracy in the Δ ellipsoidal valleys in the conduction band of *Si* as well as the degeneracy between the heavy and light hole bands in the valence band. As a result, inter-valley/band scattering is suppressed, and effective transport mass is reduced, leading to enhancements in electron and hole mobilities in strained *Si* layer. Compared to conventional *Si* bulk devices, an enhancement in electron mobility of 60 -80% and enhancement in hole mobility of approximately 30 % has been reported at room temperature [2, 8, 9]. This benefit of superior transport properties over conventional *Si* devices has recently been used in various designs of long and short channel *n* and *p*-MOSFETs [5 - 7]. Besides this, the gate tunneling current in nMOS slightly decreases with an increase in strain because of the increase in the barrier height due to band splitting which can be another benefit to lower power consumption [1]. On the other hand, possible problems in device design of strained *Si* lead to some trade-offs such as strained *Si* thickness among strain relaxation, mobility reduction and consumption of *Si* layers and thermal budget etc [7 - 9]. Although, the device design in the sub-100 *nm* regime calls for a combined layer thickness (i.e., strained *Si* and *SiGe*) of less than 50 *nm*, a reduction in the electron and hole (at room temperature) mobility in thin strained *Si* structures has been reported [10]. This is attributed to the

increase in the phonon scattering caused by the quantum mechanical confinement (QMC) effects of the inversion electrons in the strained *Si*-channel.

Various channel design such as bulk strained *Si-SiGe* [2, 7], strained *Si-SiGe* on insulator [9], strained *Si*/strained Ge dual channel heterostructures [8] have shown that the performance improvement can be retained down to 100 *nm* channel lengths. Similarly, Fan et al., [3] has performed the Monte Carlo simulation of strained *Si-SiGe* type 0.25 μm nMOSFETs with full-band structure including the quantum correction term and has addressed the potential of using strained *Si-SiGe* technology down to 50 *nm* gate length. The enhancement in the carrier effective mobility, carrier velocity and hence current drivability with various Ge mole fractions was reported.

This paper deals with the first evaluation of using strained *Si* and relaxed *SiGe* on insulator (*SSOI*) type nMOSFETs with gate lengths from 50 to 10 *nm*. Two dimensional self-consistent hydrodynamic transport simulations have been used to study the device performance in terms of the drain current enhancement, and short channel effects and with various layer thicknesses. Furthermore, the influence of lateral diffusion of shallow dopants in the source/drain extension regions close to the gate and vertical junction depth is studied to quantitatively assess the impact on the device performance.

II. Device Structure and Simulations

Figure 1 shows the layer structure of the simulated device. The *p*-type *Si* substrate has a doping concentration of 1.0 x 10^{15} cm^{-3}. A graded *SiGe* (Ge content: *x*=0.0 to 0.2) layer has 0.7 μm thickness. Over this, a 100 *nm* buried oxide layer was sandwiched between relaxed *SiGe* (*x*=0.2) layers. Bottom relaxed *SiGe* layer was 100 *nm* thick, while the thickness of the top relaxed *SiGe* (5, 7, 10, 15 nm) and strained *Si* (3, 5, 7, 10 nm) channel layers was varied in the simulation. The doping concentration in the *SiGe* and strained *Si* channel layers was 1.0 x 10^{18} and 5.0 x 10^{16} cm^{-3}, respectively. A 2 *nm* thick gate oxide was assumed in the simulation. A 180 *nm* thick poly-*Si* gate with a doping concentration of 1.0 x 10^{20} cm^{-3} was used. Similar to real

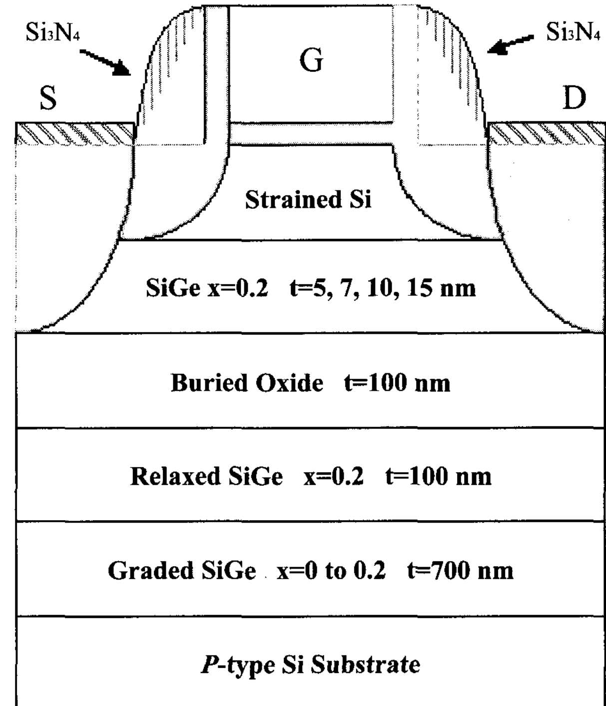


Fig. 1. Layer structure of the simulated device

devices, a thin oxide (25 *nm*) and nitride (100 *nm*) spacers were defined around the gate region. Boron (*B*) was used as a *p*-type dopant in the bulk layer structure while arsenic (*As*) was used as an *n*-type dopant in the source-drain deep contact and shallow extension regions. The peak doping concentration (*As*) in the shallow *S/D* extension regions was 1.0 x 10^{19} cm^{-3} and in the source drain contact region was 1.0 x 10^{20} cm^{-3}. The junction depth under the S/D contact was set to the appropriate layer thickness (i.e., t_{si} and t_{sg}), while the shallow S/D extension junction depth was treated as a variable in the simulation. In general, the simulated structure looks similar to that of typical processed devices [1, 5, 9, 10].

Because of very short channel lengths, a hydrodynamic transport model has been used in this study. Simulations have been conducted by two dimensional commercial device software (i.e., *DESSIS*) [17]. Various mobility models used in the hydrodynamic transport simulations take into account the doping dependence (i.,e Masetti model), the normal electric field dependence (i.e. Lombardi model) and high field saturation dependence (i.,e hydrodynamic Canali model). Similarly, bandgap narrowing effect using old Slotboom model and electronic size quantization effect using density gradient model was used in the simulation. Other physical effects such as Schokley-Read-Hall (*SRH*)

recombination (with doping dependent life times), Auger recombination and electron and hole avalanche generation were also included in the simulation. In addition to this, strain dependent effects on the carrier transport in the strained *Si* channel were studied using Egley transport mobility model, taking into account the deformation potential theory [17]. Similar to other well-known mobility models (i.e., Masetti, Lombardi, Canali etc), strain dependent Egley transport mobility model has also been tested with experimental data for 250 *nm* gate length strained *Si-SiGe* device, and has shown excellent agreement in terms of predicting drain current drivability and threshold voltage [18]. A list of model physical parameters are given in the table 1 and detailed description can be found elsewhere [17]. At a given temperature, interface state density increases from 1.0 x 10^{10} to 5.0 x 10^{11} cm^{-2} with the decrease of strained *Si* channel thickness [10] from 25 to 7 *nm*, an interface state density of 5 x 10^{10} cm^{-2} was therefore assumed in the simulation. All simulations have been carried out at room temperature. At each bias step, a set of five equations (i.e., Poisson, electron and hole current continuity, eQuantum potential, eTemperature) have been solved self-consistently.

Table. 1.

(a) *parameters in the Masetti model*

symbol	parameter name	electrons	holes	units
$\mu min1$	mumin1	52.2	44.9	cm^2 /V.s
$\mu min2$	mumin2	52.2	0	cm^2 /V.s
$\mu 1$	mu1	43.4	29.0	cm^2 /V.s
P_c	Pc	0	9.23 x 10^{16}	cm^{-3}
C_r	Cr	9.68 x 10^{16}	2.23 x 10^{17}	cm^{-3}
C_s	Cs	3.44 x 10^{20}	6.1 x 10^{20}	cm^{-3}
α	alpha	0.68	0.719	1
β		2	2	1

(b) *parameters in the Lambardi model*

symbol	parameter name	electrons	holes	units
B	b	4.75 x 10^7	9.925 x 10^6	cm/s
C	c	5.8 x 10^2	2.947 x 10^3	$cm^{(5/3)}/(V^{(2/3)}s)$
N_o	N0	1	1	cm^{-3}
λ	lambda	0.1250	0.0317	1
k	k	1	1	1
δ	delta			cm^2/Vs
A	A	2	2	1
$\alpha\perp$	alpha			cm^3
N1	N1	1	1	cm^{-3}

(c) *parameters in the hydrodynamic canali model*

symbol	parameter name	electrons	holes	units
β_0	beta0	1.109	1.2131	1
β_{exp}	betaexp	0.66	0.17	1
$v_{sat,0}$	--	1.07 x 10^7	8.37 x 10^6	cm/s
$v_{sat,exp}$	---	0.87	0.52	Cm/s

(d) *parameters in the Egley strain-induced mobility model*

symbol	me_lt	elec_100	elec_010	elec_001	mh_lh	mobh_l	hole_heavy	hole_light
value	4.81	1	2	3	0.32653	2.79	2	1

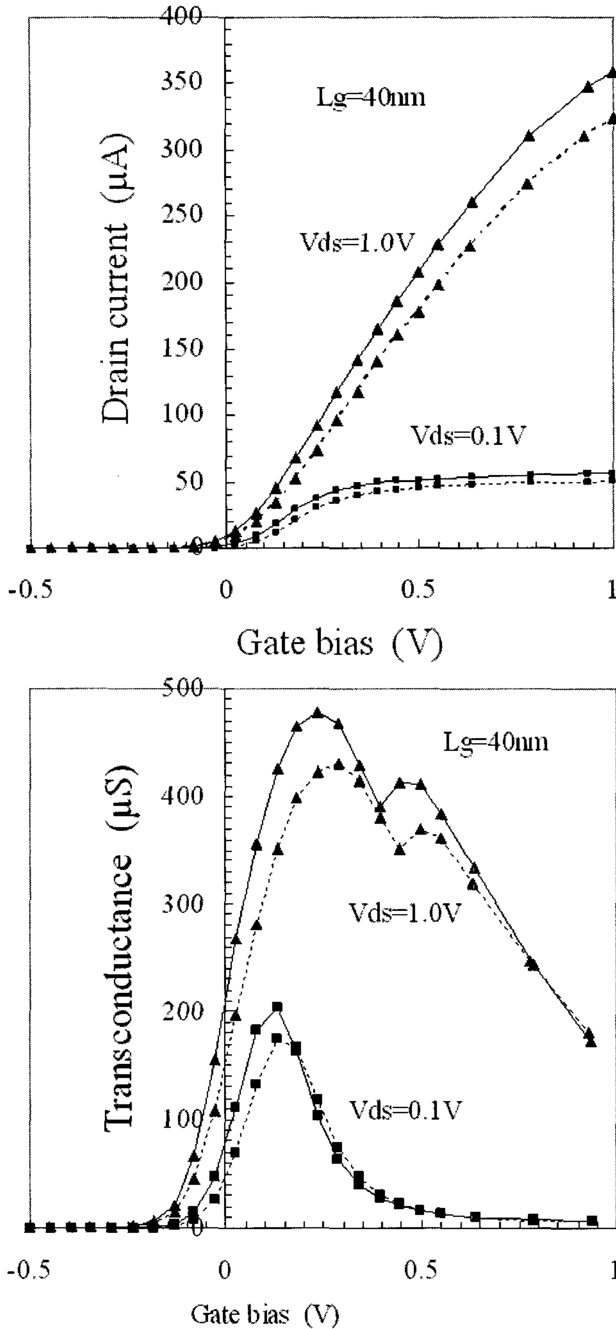


Fig. 2. Drain current (top) and transconductance (bottom) as a function of the gate bias for 40 nm gate device. Solid lines are strained Si/SiGe channel and dotted lines are control Si device

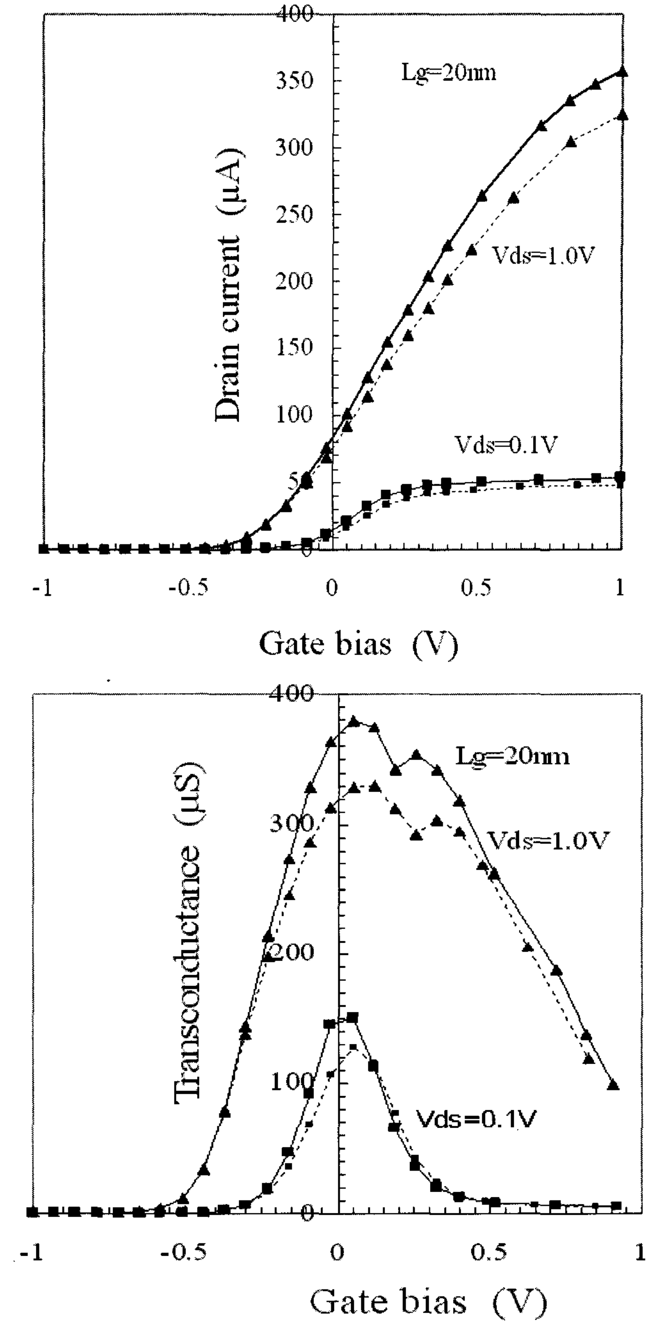
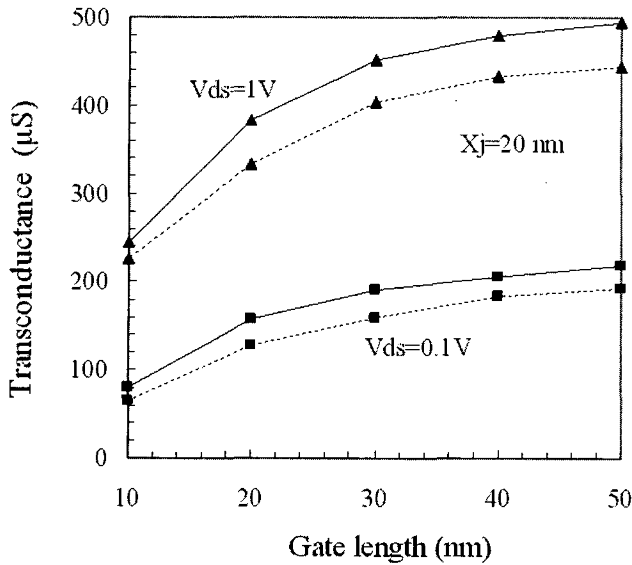


Fig. 3. Drain current (top) and transconductance (bottom) as a function of the gate bias for 20 nm gate device. Solid lines are strained Si/SiGe channel and dotted lines are control Si device

III. Results and Discussion

Figure 2 and 3 show the drain-source current and transconductance as a function of the gate bias for 40 (fig.2) and 20 *nm* (fig. 3) gate length device with a strained *Si* channel (t_{si}) of 5 and *SiGe* (t_{sg}) layer of 15 *nm* thick. Compared to conventional control device, strained *Si-SiGe* device gives larger drain current drivability over the whole gate bias region. With the same layer physical (thickness, doping) and geometrical parameters (gate length, junction depths), *Si* control device was simulated using conventional mobility models (i.e., doping dependence, normal electric field and high field saturation dependence) without taking



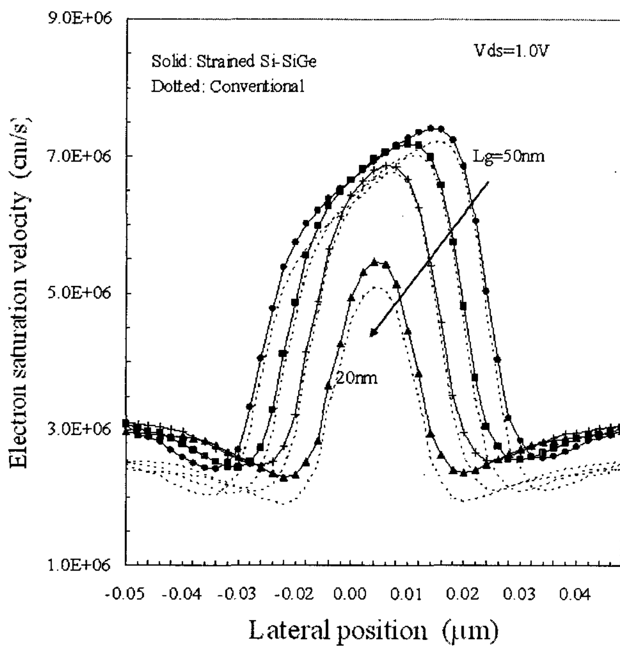
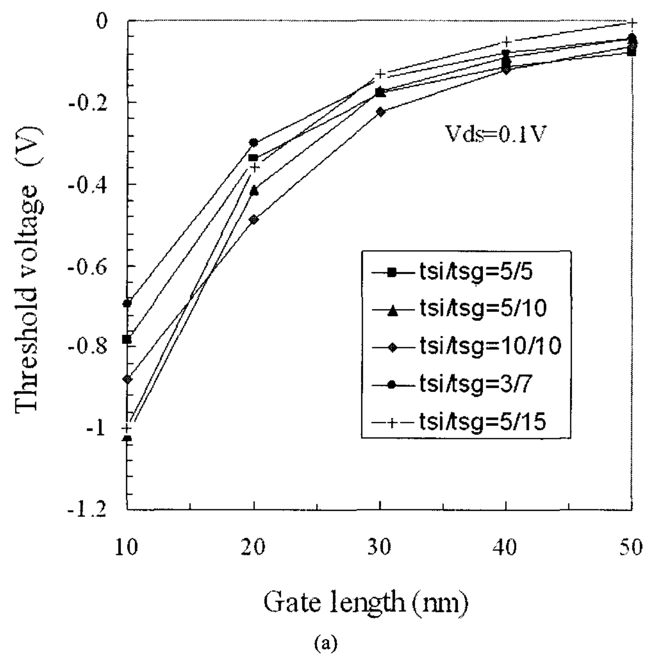


Fig. 4. Maximum transconductance (top) and electron saturation velocity (bottom) for various gate length at Vds of 1.0V. Solid lines are strained Si/SiGe and dotted lines are control Si device. Vds is equal to 0.9V for 20 and 10 nm gates

strain effects into account. Compared to control device, larger transconductance values for strained *Si-SiGe* device have been obtained for all gate lengths. Transconductance and electron saturation velocity as a function of the gate length is shown in figure 4. For a given drain bias, an improvement in the transconductance of 10-15% is retained for all gate lengths of strained *Si-SiGe* channel over *Si* control device. Similar to previous theoretical [8] and experimental observations [9-10] of strained *Si-SiGe* based nMOSFETs, we believe that the improvement in the current drivability and transconductance is due to the enhancement in the electron mobility and electron saturation velocity. Note also that the electron saturation velocity is still higher than that of the *Si* control device for all gate lengths. For example, a peak electron saturation velocity of 7.6 x 10^6 and 7.0 x 10^6 cm/sec was obtained for 50 nm strained *Si-SiGe* and *Si* control device, respectively. Fan et al., [3] has performed full-band Monte Carlo simulations and reported a value of 8.5 x 10^6 and 5 x 10^6 cm/sec for 250 nm gate strained *Si* and unstrained *Si* device, respectively. Similarly Rim et al., [6] has extracted a value of 1 x 10^7 and 8.5 x 10^6 cm/sec from the measured DC data for 100 nm gate strained *Si* and control *Si* device, respectively. The calculated electron saturation velocity by hydrodynamic transport simulations was 8 x 106 cm/sec for the same device [6]. The present simulation work of electron saturation velocity shows fairly close agreement to this data.

In order to study the suitability of the device from the view point of improved short channel effects and transconductance, different layer combinations of strained *Si* channel (t_{si}) and *SiGe* layer (t_{sg}) have been evaluated and for different gate lengths. Two sets of layer combinations (i.e., deep junctions and shallow junctions) have been simulated. Figure 5a and b deals with the deep source/drain extension junctions, where the shallow



(a)

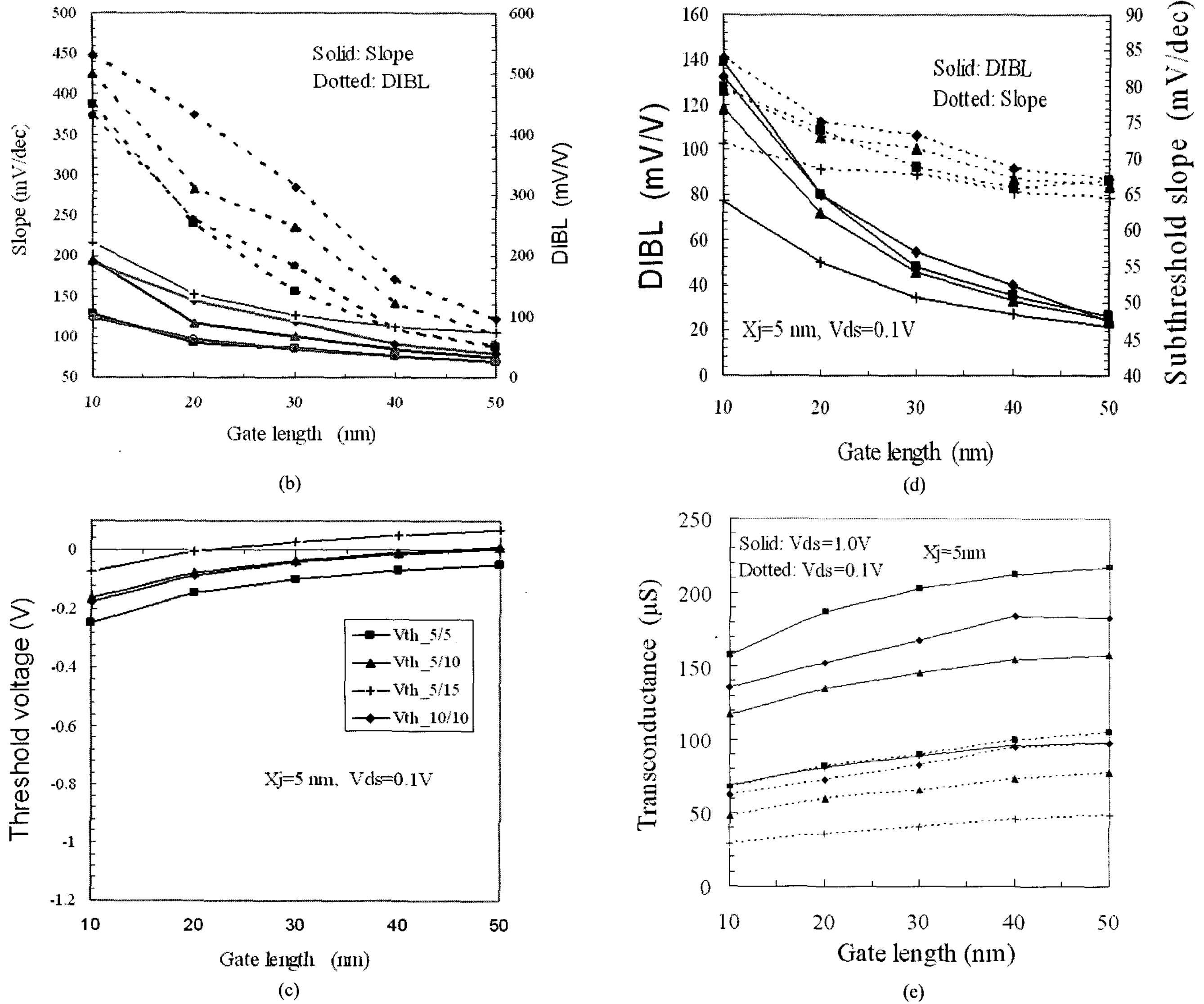


Fig. 5. Threshold voltage, subthreshold voltage slope S, transconductance and DIBL as a function of the gate length. Threshold voltage (a) and S, DIBL (b) for deep extension junction. Threshold voltage (c), S,DIBL (d), and transconductance (e) for shallow extension junction (Xj=5nm). In all figures, squares for (t_{si}/t_{sg}) 5/5 nm, triangles for 5/10 nm, diamonds for 10/10 nm , circles for 3/7 nm and plus for 5/15 nm

junction depth is equal to the appropriate layer thickness (worst case scenario) and figure 5c, 5d, 5e deals with the shallow junctions (5 nm depth) for all layer combinations. Compared to shallow junction, higher drain current and larger transconductance is expected for deeper junctions. However, the performance is limited by the severe short channel effects as observed in our simulation for deeper *S/D* extension junctions, where the *Vth* roll-off and increase in the subthreshold voltage slope *S* and *DIBL* (drain induced barrier lowering) is quite significant with decreasing gate length. For a given gate length, thicker layer (t_{si} and t_{sg}) combination increases the subthreshold voltage slope *S* and *DIBL*. Although a high electron mobility and hence larger drain current drivability is achieved with thick strained *Si* channel [9], increased short channel effects limit the device performance in practical applications. On the other hand, thin or shallow (i.e., 5 *nm* in fig. 5c, 5d, 5e) source/drain extension junction significantly improves the *Vth* roll-off, subthreshold voltage slope *S* and *DIBL* for all gate lengths and for different layer combinations. Although, the layer combination with t_{si}/t_{sg} of 5/15 *nm* thickness produces the lowest *S* (i.e., 64 to 72 *mV/dec*) and *DIBL* (i.e., 21 to 77 *mV/V*) values for all gate lengths, the tranconductance is quite degraded because of the increase in the total resistance of the device with shallow source/drain

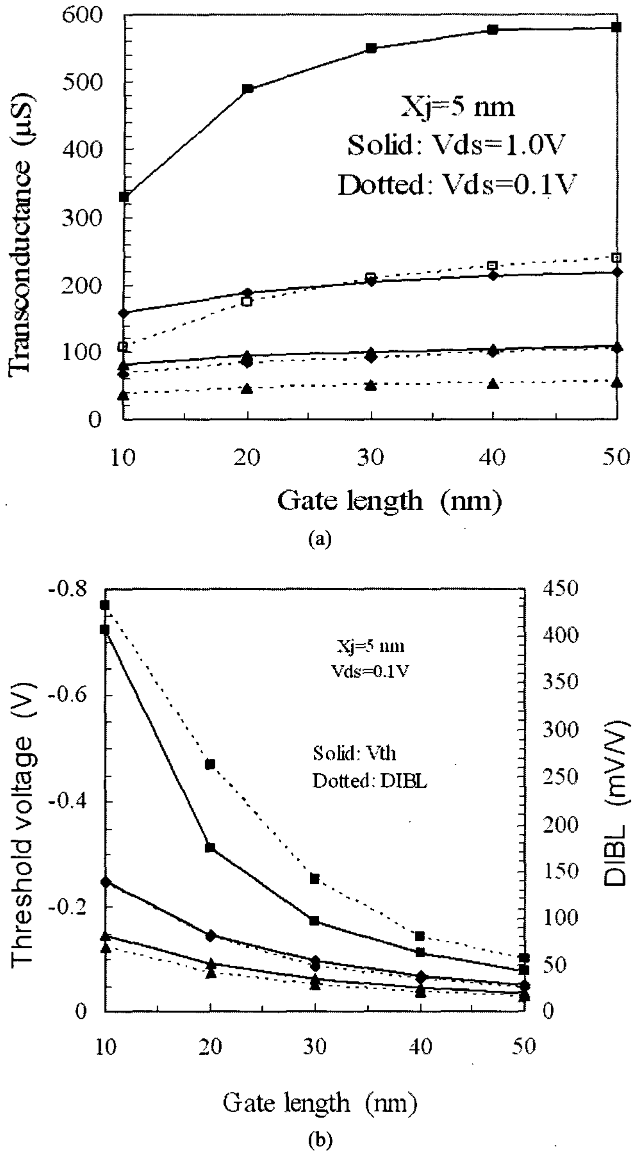
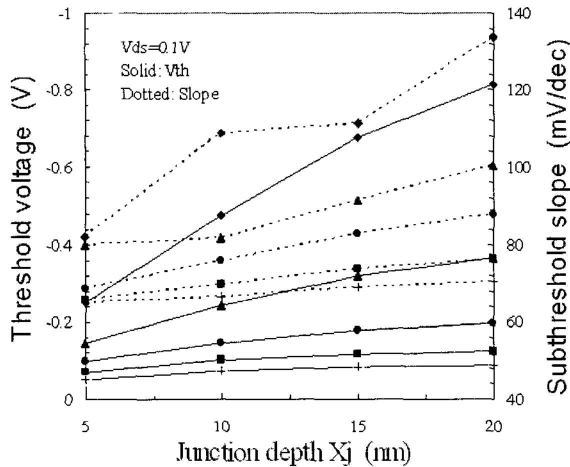


Fig. 6. Maximum transconductance (a) and threshold voltage, DIBL (b) as a function of the gate length for various doping concentration. Squares (5 x 10^{19} cm^{-3}), diamonds (1 x 10^{19} cm^{-3}) and triangles (5 x 10^{18} cm^{-3})

extension junctions. Compared to t_{si}/t_{sg} of 5/15 *nm* thickness, a layer combination with t_{si}/t_{sg} of 5/5 *nm* thickness has shown higher transconductance with acceptable *S* and *DIBL* values of 66 to 79 *mV/dec* and 26 to 139 *mV/V*, respectively from 50 to 10 *nm* gate length. For example, a reduction in the drain source current and transconductance at *Vds* and *Vgs* of 1.0 *V* was about 50 % for t_{si}/t_{sg} of 5/15 than that of t_{si}/t_{sg} of 5/5 *nm* thickness. Although, a high electron mobility demands thick strained *Si* channel layer, mobility degradation concerns have been reported for thin strained *Si* layers [1, 4, 10] as required for sub-100 *nm* nMOS realization. Takagi et al., [1] has shown that the origins of severe reduction in the electron mobility with thin strained *Si* layer are interface states and fixed charges, attributed with the *Ge* atoms diffusion from *Si/SiGe* interface to the MOS interface. Similarly, Mizuno et al., [10] has demonstrated that the reduction in the electron mobility with thinning of the strained -*Si* layer is attributed to the quantum mechanical confinement effect in the strained *Si* layer. Based on these experimental findings and supported from our simulation study, a lower limit of strained *Si* layer thickness of 4 -5 *nm* has been proposed.

For a given layer thickness and constant *S/D* extension junction depth and doping, the transconductance decreases with the gate length in our simulation. The decrease in the transconductance with the gate length is illustrated in figure 6 for different *S/D* doping concentration in the extension region. All other parameters have been fixed and only *S/D* doping in the shallow extension region was varied. At *Vds* of 0.1 and 1.0 *V*, the decay in the transconductance was 55 and 43 % with varying gate length from 50 to 10 *nm* at 5.0 x 10^{19} cm^{-3}. The transconductance decay was reduced to 35 and 27 % at *Vds* of 0.1 and 1.0 *V* for 1.0 x 10^{19} cm^{-3}. Note that the decrease in the transconductance is minimal for 5.0 x 10^{18} cm^{-3}. For a given gate length, *Vth* and *DIBL* increase with the doping concentration (fig. 6b). At Vds of 0.1*V*, the subthreshold voltage slope *S* (not shown here) changes from 72 to 130 and 65 to 73 *mV/dec* with varying doping concentration from 5.0 x 10^{18} to 5.0 x 10^{19} cm^{-3} for 10 and 50 *nm* gate, respectively. The decrease in the transconductance and saturation velocity observed in our simulation is attributed to the long range Coulomb interaction. Fischetti [22] has performed self-consistent Monte Carlo simulation and demonstrated that the *Si* devices with channel length shorter than about 40 *nm* and gate oxide thinner than 2.5 *nm* suffer from long-range Coulomb interactions of channel electrons with electrons in the heavily doped *S* and *D* regions. These interactions cause a reduction in the electron saturation velocity by more than a factor of 2. Pinto [23] has performed numerical simulations of deep submicron devices including velocity overshoot effects and demonstrated that the saturated transconductance deviates from a strict μ_{eff}/L_g dependence. Similarly, other experimental and theoretical [12] findings have shown that the mobility and electron



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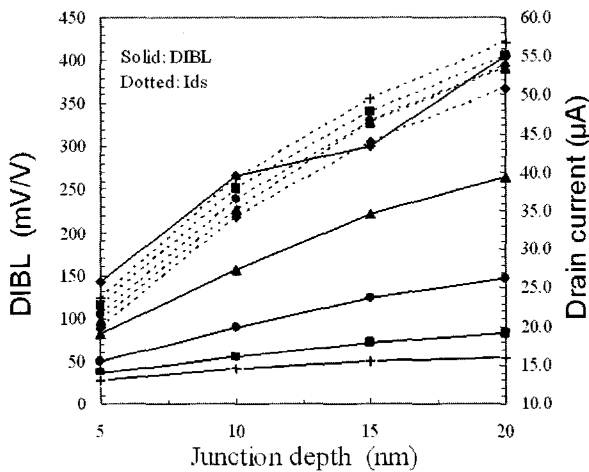

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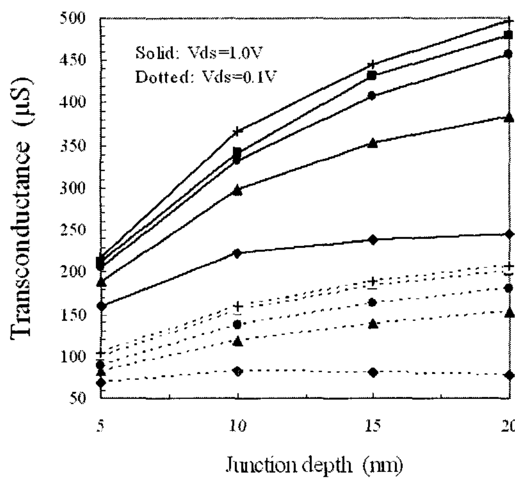


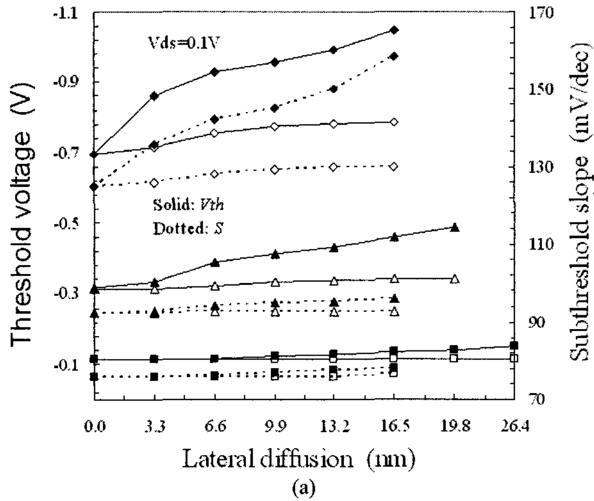
(c)

Fig. 7. Threshold voltage (a), DIBL, Ids (b) and transconductance (c) as a function of the junction depth for various gate lengths. Plus (50 nm), squares (40 nm), circles (30 nm), triangles (20 nm), and diamonds (10 nm)

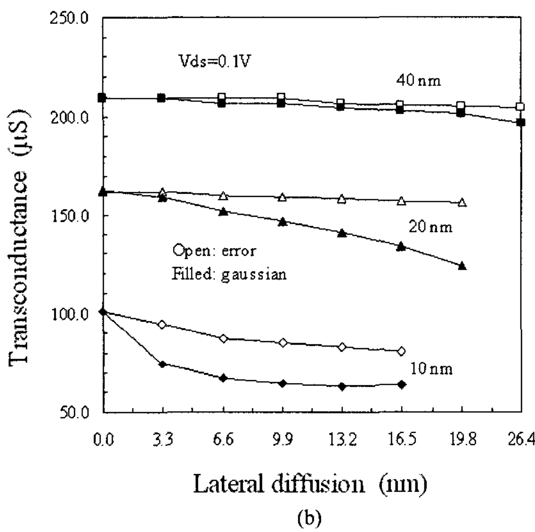
velocity decrease with the gate length because of strong Coulomb interactions and increased surface scatterings at short channel lengths.

With fixed layer thickness (t_{si}/t_{sg}=5/15 *nm*) and doping concentration (1.0 x 10^{19} cm^{-3}) in the *S/D* extension region, the junction depth (*Xj*) has been varied and for different gate lengths. Previous studies [13, 19, 21] have shown that the *S/D* extension junction depth *Xj* as low as 10 *nm* is needed to realize sub-100 *nm* gate nMOS devices, since too shallow junction depth can lead to a high external resistance, which in turn results in Idsat degradation. Thus, the fundamental trade-off exist between short channel effects and series resistance in the *S/D* extension region in the sub-100 *nm* CMOS scaling. With mobility degradation concerns in mind, short channel effects have been suppressed using more aggressive super halo design or higher substrate doping [13, 14] to achieve high performance sub-100 *nm* devices. Figure 7 shows the *Vth, S, DIBL*, transconductance and drain current as a function of the junction depth. For a given gate length, threshold voltage *Vth*, slope *S*, *DIBL*, drain current and transconductance vary quasi-linearly with varying junction depth. For example, an increase in the drain current and transconductance of approximately 60 and 50 % was obtained with varying junction depth from 5 to 20 *nm* at 30 *nm* gate length. The increase in *S* and *DIBL* was 21 and 65 % with varying junction depth from 5 to 20 *nm* at 30 *nm* gate length. Variations in S (i.e., 9 %) and DIBL (i.e., 47 %) values were improved for 50 *nm* gate length with varying junction depth from 5 to 20 *nm*. At 10 nm junction depth, the subthreshold slope *S* (and *DIBL*) of 108 (266), 81 (156), 75 (88), 69 (55) and 66 (41) mV/dec (mV/V) was obtained for 10, 20, 30, 40 and 50 nm gate device, respectively. Similarly, *S* (and *DIBL*) values of 82 (142), 79 (83), 68 (50), 65 (36), and 63 (28) were obtained for 10, 20, 30, 40 and 50 nm gate device, respectively at 5 nm junction depth. These numbers clearly show that the shallow junctions (5 -10 *nm*) are needed to suppress/minimize the *S*, and *DIBL* in order to realize sub-50 *nm* gate strained *Si* nMOSFETs as observed in our simulation and consistent with previous theoretical [13] and experimental [14,15] findings on conventional *Si* nMOS devices.

Lateral source/drain diffusion of impurities underneath the gate edge region is another parameter which needs special attention for sub-100 nm gate realization. Depending on the doping profile and the impurity type



(a)



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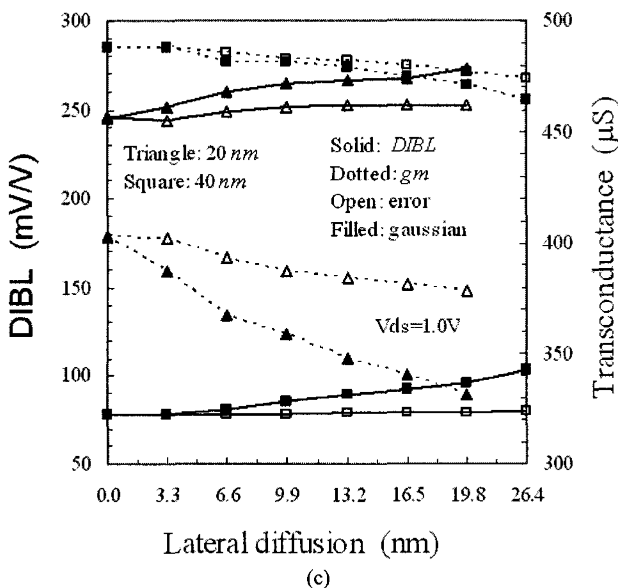

(c)

Fig. 8. Threshold voltage (a), transconductance (b), and DIBL (c) as a function of lateral diffusion using Gaussian (filled symbol) and error function (open symbol) profiles in the simulation. Squares (40 nm), triangles (20 nm), and diamonds (10 nm)

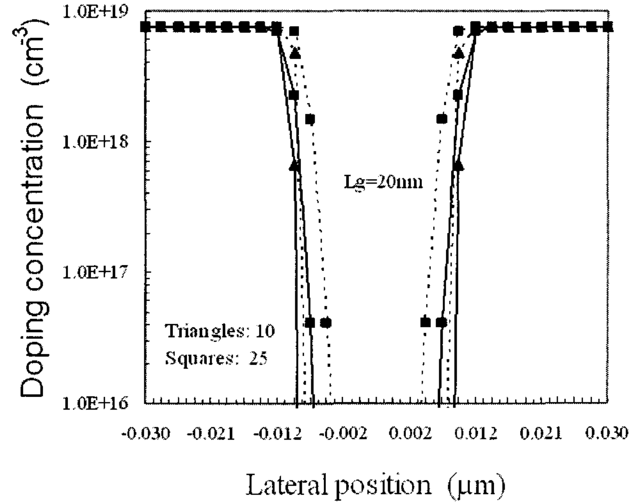

Fig. 9. Doping concentration profile for 20 nm gate length device with a lateral diffusion factor of 10 (triangles) and 25 (squares) using Gaussian (dotted) and error (solid) function profile

[11], the lateral diffusion of impurities produces the gate overlap region (L_{ov}) and hence reduces the effective gate length: an effect which becomes more critical as the channel length is scaled down to sub-50 *nm*. If the overlap of the *S/D* extension and the gate edge is too great, the device will suffer from excessive leakage due to increased short channel effects that arise due to reduced channel length. On the other hand, if the overlap is too short, the on-state saturated drain current will decrease because the end of the channel and the *S/D* extension region is not electrically coupled. Since the type of impurity used in the shallow source-drain extension region varies from device to device [7, 11], different lateral doping gradients are produced and hence difficult to control in sub-100 *nm* devices. In order to study this effect, we therefore simulated devices using Gaussian profile and error function profile for lateral diffusion of dopants since both profiles result in different doping gradient. The junction depth and doping concentration (1.0 x 10^{19} cm^{-3}) was kept constant in the shallow *S/D* extension region. The detailed description of the analytical function of both profiles and calculation of the lateral distance is found elsewhere [17]. Figure 8 shows the *Vth, S, DIBL*, and transconductance as a function of the lateral diffusion and for different gate length. A doping concentration profile for Gaussian and error function for 20 gate length device is shown in figure 9. For a given gate length, *Vth, S*, and *DIBL* increase with the lateral diffusion and enhancement is larger for the Gaussian than the error lateral profile. Similarly, the

transconductance decreases with the lateral diffusion and this decay is larger for the Gaussian than the error lateral profile. For a fixed lateral diffusion, the increase in the *Vth, S,* and *DIBL* and decrease in the transconductance is higher for shorter channel lengths. Although, these observations are in general consistent with the design work for *Si* based nMOSFETs [14], the importance of doping gradient or abruptness is extremely critical for realizing sub-50 *nm* devices. Thus, heavier dopant atoms such as *Sb* (because they have shorter diffusion length under the same annealing condition) are needed because they form more abrupt junctions than conventional light atoms (e.g., *As*) for realizing sub-50 *nm* gate devices. From the viewpoint of the process margin and lateral doping control, new atoms such as *Sb* and *In* have been proposed [11] for sub-100 *nm n* and *p-MOS* devices for the fabrication process.

IV. CONCLUSIONS

We have demonstrated that the strained *Si-SiGe* on insulator (*SSOI*) type nMOSFETs can be realized down to gate length 10nm since they retain the benefit of increased electron mobility over conventional control *Si-* devices. Although the net performance improvement is limited by the short channel effects, this simulation work shows that the sub-50 *nm* gate devices suffer from long-range Coulomb interactions and hence degrades the devices speed because the transconductance decreases with the gate length. With reasonable transconductance and current drivability, the short channel effects can be well controlled with shallow *S/D* extension junction depth of 5-10 *nm* and with thin layer combination of t_{si}/t_{sg}=5/5, 5/10 and 5/15 *nm*. Furthermore, with controlled lateral diffusion length of 5-10 *nm*, heavier dopant atoms (such as Sb) are needed since they produce abrupt doping profile: an aspect which is critical for sub-50 *nm* device realization.

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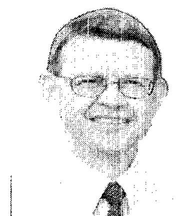
Muhammad Nawaz He received the M. Sc (Physics) degree from University of Punjab Lahore, Pakistan in 1987. He also received M.Sc (Optoelectronics) and Ph.D (Electronics) degrees from University of Oslo, Norway in 1992 and 1996, respectively. His major area of research interest deals with semiconductor device physics. Particularly, he works with design, modeling, simulation, processing and characterization of compound semiconductor devices and circuits. He spent one year as a research fellow at Nanyang Technological University, Singapore and worked on simulation and processing of GaAs and InP based HEMT devices. In 1997, he joined Chalmers University of Technology, Sweden, where he mainly worked on processing and characterization of 0.1um InP and GaAs based HEMTs and MMICs devices for microwave and millimeterwave applications. From 2000 to 2004, he had been working on design, and development of 1.55 um InP based DFB Lasers, DFB-EA (electroabsorption modulators) Lasers, 1.3 um InP based FP lasers and 1.55 um APDs (avalanche photodiodes) at Ericsson Microelectronics and Northlight Optronics AB in Sweden. In Oct-2004, he joined Infineon Technologies AG as expert technology simulation, where his main research interest deals with technology and device simulation of Si based nano MOS devices. He is author and co-author of 48 research articles published in various referred international journals and conferences. He is senior member of IEEE and review member of various IOP (Institute of Physics) journals.



Mikael Östling Received the MSc degree in engineering physics and the PhD degree from Uppsala University in 1980 and 1983 respectively. He has been with the faculty of EE of KTH, Royal Institute of Technology in Stockholm, Sweden since 1984 where he holds a position as professor in solid state electronics. Since 2001 he is head of the department of microelectronics and information technology. In December 2004 he was appointed Dean, School of Information and Communication Technology, KTH. He was a senior

visiting Fulbright Scholar 1993-94 with the center for integrated systems at Stanford University, and a visiting professor with the University of Florida, Gainesville. He initiated and was appointed program director by the Swedish Foundation for Strategic Research for a 5 year RF-CMOS national Swedish program, coordinating the 3 major universities in Sweden in this area. His research interests are silicon/silicon germanium devices and process technology for very high frequency, as well as device technology for wide bandgap semiconductors with special emphasis on silicon carbide and nitride based structures. He has supervised 20 PhD theses work, and been the author of 8 book chapters and about 300 scientific papers published in international journals and conferences. Mikael Östling is a fellow of the IEEE.