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A Control Technique for 120Hz DC Output Ripple-Voltage Suppression Using BIFRED with a Small-Sized Energy Storage Capacitor

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ABSTRACT

This paper presents a technique to reduce the low frequency ripple voltage of the dc output in a BIFRED converter with a small-sized energy storage capacitor. The proposed pulse width control method can be effectively used to suppress the low frequency ripple appeared in the dc output and still maintains generally good performance such as low THD of input line current and a high power factor. Using the small-sized energy storage capacitor, it has better merits of low cost and smaller size than a conventional BIFRED converter. The proposed technique is illustrated its validity and effectiveness through simulations.

Keywords: BIFRED, Ripple-voltage suppression, Small-sized energy storage capacitor

1. Introduction

Owing to the growing concern regarding harmonic pollution of the power distribution system, and the adoption of standards such as IEC-555-2[1], there is a need for single-phase power supplies whose AC line currents are low in harmonic content and have a power factor close to unity. The BIFRED(boost integrated flyback rectifier energy storage dc-dc converter) converter is a single stage converter that consists of a boost converter for power factor correction [2] and a flyback converter for dc output voltage regulation [3]-[5]. The BIFRED has a near sinusoidal line current, output isolation and regulated output voltage [6].

In this system, power factor correction and output voltage regulation are achieved by the pulse width control method. However there is a low frequency ripple voltage in the DC output. The DC ripple voltage produces the associated ripple current in the DC-link, which may flow through into the battery, when the battery is connected to the DC output. It is said that the low frequency ripple current flowing into a battery causes an increase in the operating temperature and reduces the life time of a battery. Also, the low frequency ripple voltage is fed back to the control loop through the voltage controller and may introduce any waveform distortion of the input line current. In order to reduce the ripple voltage, a large energy storage capacitor is

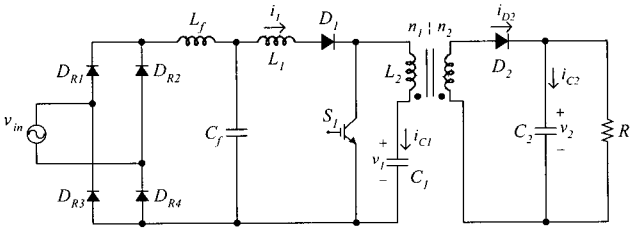

Fig. 1 The BIFRED converter

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used. At that point its voltage is essentially constant over the line period under normal operating conditions. Therefore, energy storage capacitor can absorb and supply the difference between the pulsating (single-phase AC) instantaneous input power and the constant DC output, and hence the output voltage is originally constant.

In this paper, without the extra power circuit, the practical suppression technique to reduce the low frequency ripple voltage of the DC output in the BIFRED converter with the small-sized energy storage capacitor is proposed. Simulation and experimentation are performed to illustrate validity of the control methods.

2. Conventional BIFRED converter [9]

The BIFRED converter, shown in Fig. 1, consists of a boost input circuit integrated with a flyback output stage, thus using a single switch. The particular problem of high energy storage capacitor voltage at light loads is addressed and it is shown how this may be resolved if the boost and flyback sections of the converter are allowed to operate discontinuously. Therefore the boost stages operates in a DCM (Discontinuous conduction mode) [7], [9].

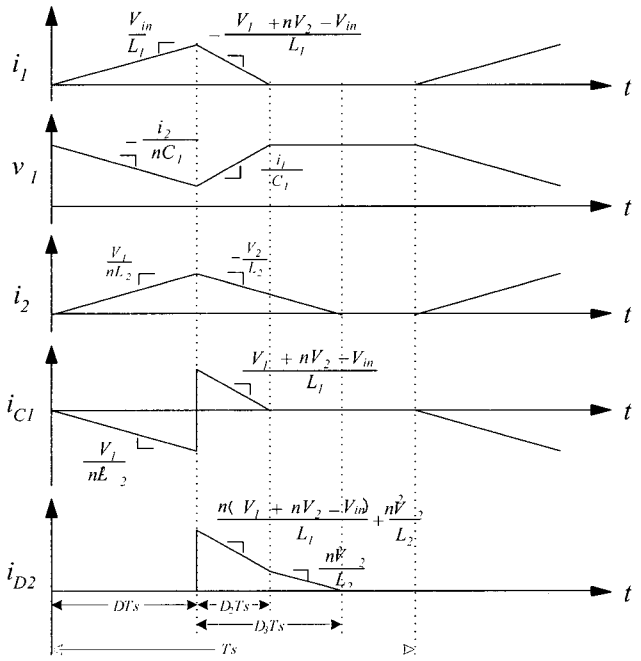


Fig. 2 Discontinuous conduction mode waveforms

Fig.2 shows the ideal waveforms of a BIFRED flyback converter in which both the boost and the flyback sections operate discontinuously. The converter should be designed such that the input inductor current (i_1) becomes discontinuous before that of the transformer magnetizing inductance (i_2). If this condition is not satisfied, i_1 becomes continuous at the peak of the input voltage, resulting in a surge of current and, hence, an increase in the input current total harmonic distortion (THD). Therefore, the BIFRED converter must be designed to operate in a mode whereby i_1 becomes discontinuous before i_2. The operation modes are classified into 4 intervals shown in Fig. 2.

2.1 Large-signal model

If the inductor and capacitor currents are averaged over a switching period, a large-signal instantaneous average model of the operation for the DCM BIFRED converter is given in Eq. (1) ~ (3).

$$(i_1)_{av} = \frac{D^2 T_s}{2L_1}\left(\frac{v_{in}(v_1 + nv_2)}{v_1 + nv_2 - v_{in}}\right) \tag{1}$$

$$\left(C_1 \frac{dv_1}{dt}\right)_{av} = \frac{D^2 T_s}{2}\left\{\frac{1}{L_1}\left(\frac{v_{in}^2}{v_1 + nv_2 - v_{in}}\right) - \frac{v_1}{L_2}\right\} \tag{2}$$

$$\left(C_2 \frac{dv_2}{dt}\right)_{av} = \frac{D^2 T_s n}{2}\left(\frac{1}{L_1}\frac{v_{in}^2}{v_1 + nv_2 - v_{in}} + \frac{1}{L_2}\frac{v_1^2}{nv_2}\right) - \frac{v_2}{R} \tag{3}$$

where v_{in} is the line voltage, v_1 is the bulk capacitor voltage, v_2 is output voltage, L_1 is the input inductance, L_2 is the flyback transformer magnetizing inductance, T_s is the switching period, D is switch duty cycle, n is the flyback transformer turns ratio, and R is the road resistance.

2.2 Steady-State Equations

In steady state, the average value of the energy storage capacitor current and the output capacitor current must be zero over a half line period. If it is assumed that the duty cycle D and switching period T_s are constant and that the ripple of voltages v_1 and v_2 can be neglected, then the averaging (2) over a half line period and equating to zero results in the steady-state equation

$$V_1 = \frac{V_{in\,Peak} L_2}{L_1}\left\{-\frac{2}{\pi} - M + \frac{2}{\pi}\frac{M^2}{\sqrt{M^2-1}}\left(\frac{\pi}{2} + \tan^{-1}\frac{1}{\sqrt{M^2-1}}\right)\right\} \quad (4)$$

where, $M = \frac{V_1 + nV_2}{V_{in\,Peak}}$, $V_{in\,peak}$ is the peak of the line voltage,

V_1 and V_2 are average voltage of v_1 and v_2 respectively. L_1 is the input inductance, T_s is the switching period and D is switch duty cycle. Substituting (4) into the half line period average of the output capacitor current yields the following equation for the steady-state duty cycle D:

$$D = \sqrt{\frac{2L_2}{RT_s}\frac{V_2^2}{V_1(V_1 + nV_2)}} \quad (5)$$

2.3 Condition for DCM

As mentioned previously, the DCM BIFRED must also be designed such that i_1 becomes discontinuous before i_2 reaches zero. The condition for ensuring the correct operation is

$$\frac{D_2}{D_2 + D_3} \le 1 \quad (6)$$

where D_2 and D_3 are as defined in Fig. 2, the condition for ensuring the correct operation is

$$\frac{V_1}{V_{in\,peak}} \ge 1 \quad (7)$$

To ensure that the flyback section of the converter remains discontinuous, the magnetizing inductance of the transformer must be limited to a value that will allow discontinuous operation for maximum output power and for the minimum energy storage capacitor voltage. When operating at the cups of the input voltage, the energy contribution from the boost input is zero and hence all the energy is supplied by the bulk capacitor. Therefore, the switch on-time is at its maximum at this point and the maximum magnetizing inductance referred to the primary is

$$L_{1\max} = \frac{\left(\frac{V_{1\min} nV_2}{V_{1\min} + nV_2}\right)^2 T_s}{2P_{out\max}} \quad (8)$$

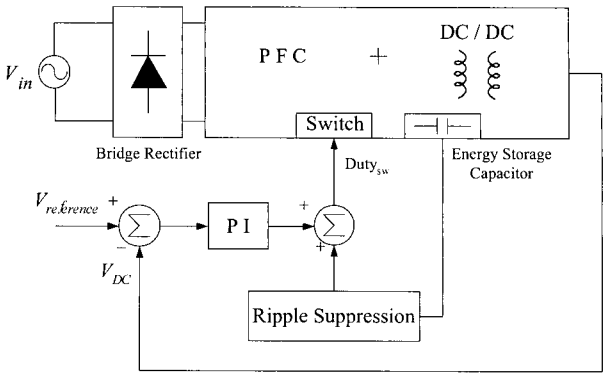


Fig. 3 Control block diagram

To ensure that the converter operates in the correct mode, the magnetizing inductance must be calculated from equation (8), and then the input inductance can be selected by setting the energy storage capacitor voltage equal to the peak of the minimum input voltage in equation (4).

3. Voltage Ripple Suppression Scheme

To reduce the voltage of the energy storage capacitor, both boost and flyback sections operate in the DCM. In the DCM mode, it is possible to reduce the energy storage capacitor voltage, however it has a problem that increases the conduction loss and low-frequency ripple of the output voltage. Therefore, big-sized electro extra power circuit elements such as big-sized energy storage capacitor are provided.

The low-frequency DC ripple voltage in the BIFRED converter with the small-sized energy storage capacitor is easily suppressed with the help of the ripple voltage supression scheme, without adding the additional power devices to the power circuit. Fig. 3 shows a control block diagram of the proposed method. The proposed control loop consists of two different loops. One control loop is for the output voltage regulation and the other control loop is for the ripple voltage suppression of the low frequency component in the DC output voltage. This ripple suppression is obtained by feedforward of the low frequency ripple voltage.

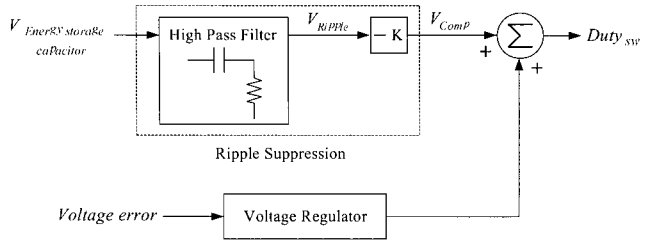


Fig. 4 determination of the duty signal

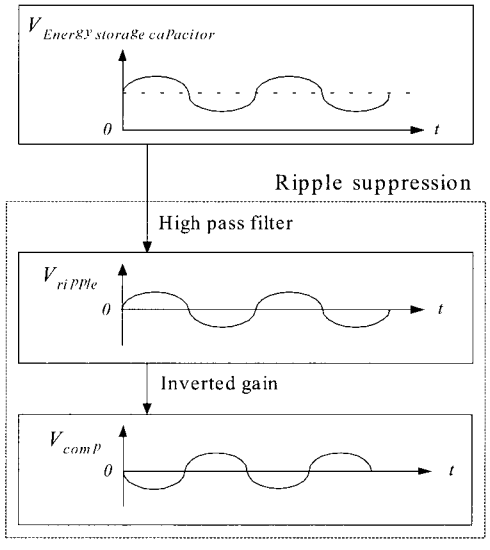


Fig. 5 Waveforms in the ripple suppression circuit

Fig. 4 shows the detailed control scheme for the ripple voltage suppression. The control signal for the ripple suppression is established through a high pass filter and an inverted gain block from a measurement of the energy storage capacitor voltage. The cutoff frequency of the filter is selected so that only the ac component of the low frequency ripple voltage around 120Hz can be shifted. It can be seen in Fig. 5 that the control signal for the ripple reduction is obtained from the waveform of the practical ripple voltage.

The proposed DC ripple voltage suppression scheme shows good performance in the DCM BIFRED converter as well as the CCM BIFRED converter.

4. Simulation

Several simulation models of the proposed control technique for the BIFRED converter are done to show validity.

Table 1. Parameters of the BIFRED Converter

BIFRED	
Parameter	Value
L_1	260μH
C_1	20μ ~ 220μF
N	2
L_2	350μH
C_2	250μF
R	8Ω
L_f	262μH
C_f	1μF
f_s	30kHz

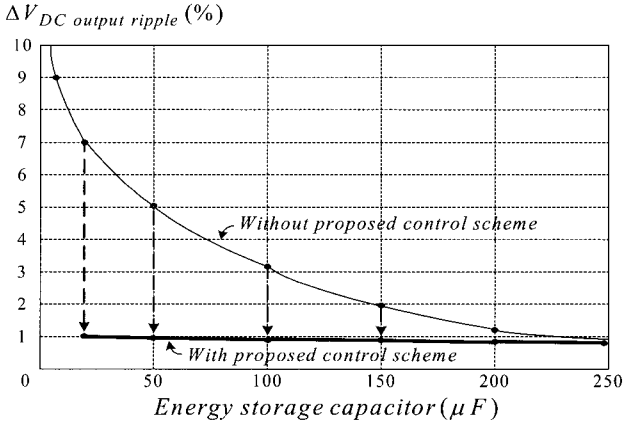


Fig. 6 Energy storage capacitor versus DC output ripple voltage in the BIFRED converter

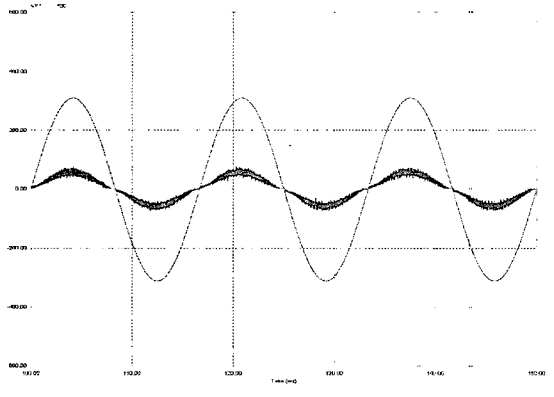
They performed under an environment of the input voltage of 220Vac, 60Hz, the output DC voltage of 48Vdc, and the output power of 300W. The component values are given in Table 1.

Fig. 6 shows the relation of the energy storage capacitor and DC output ripple voltage in the BIFRED converter. It can be seen from this figure, the ripple voltage of the DC output is increased from 1% to 7% by reducing energy storage capacitor C_1 from 220μF to 20μF. However, the DC output voltage ripple is controlled about 1% regardless of the varying energy storage capacitor when the proposed control scheme is applied.

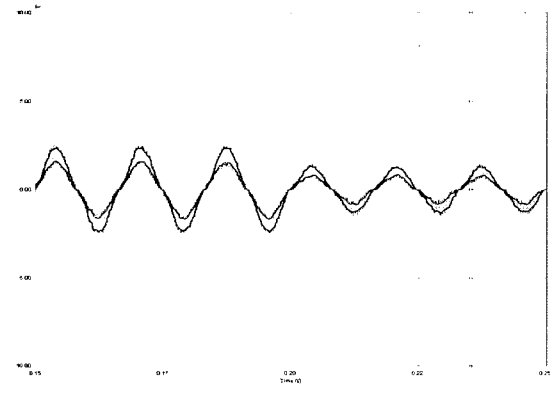
4.1. DCM BIFRED converter

Fig. 7(a) shows the simulated input voltage and input current of the DCM BIFRED converter using the proposed control method. Fig. 7(b) shows that the simulation result of the input current under the load condition is varied from full to half at t=200ms. As shown in Fig. 7, the waveform of input line current is nearly a sinusoidal waveform, maintaining the high power factor.

Fig. 8(a) shows the simulation result of the DC output voltage waveforms. It is said in this figure that the low frequency ripple component is relatively reduced when the proposed ripple suppression scheme is applied at t=250m. Fig. 8(b) shows the simulation results of the input voltage and output voltage under the input voltage is varied from 311V to 350V at t=100ms. Fig. 8(c) shows the simulation results of the output voltage and output current under the load condition is varied from full to half at t=100ms. It can be seen from these figures that the output voltage is constantly regulated.

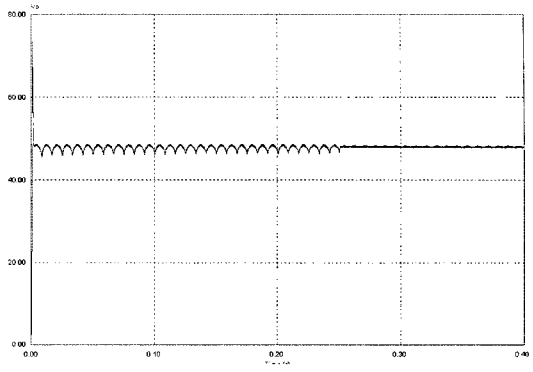


(a) Input voltage and input current(×30) waveform

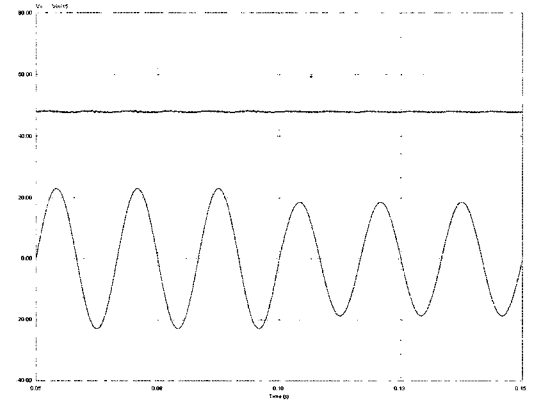


(b) Input current at the variation of the load (at 200ms)

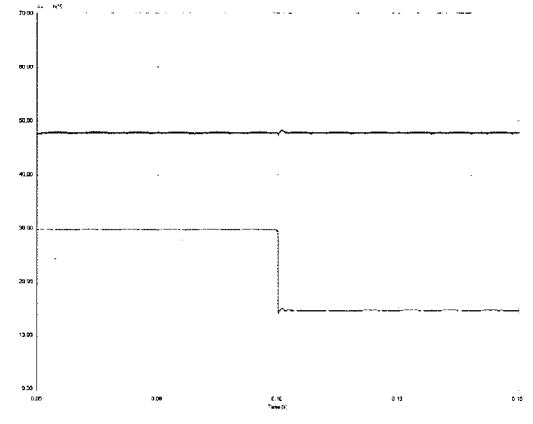
Fig. 7 Input current waveform in DCM BIFRED converter



(a) With proposed control method (at 250ms)



(b) Output voltage and input voltage(÷15) waveform at the variation of input voltage (at 100ms)



(c) Output voltage and output current(×5) waveform at the variation of load from full to half (at 100ms)

Fig. 8 Output voltage waveform in DCM BIFRED converter

4.2 CCM BIFRED converter

Fig. 9 shows the simulated input voltage and input current of the CCM BIFRED converter using the proposed control method.

Fig. 10 shows the simulated results of the DC output voltage waveforms when the proposed ripple suppression scheme is applied. It also shows that the low frequency ripple component is relatively reduced.

5. Experiment

Fig. 11 shows the experimental input voltage and input current of the DCM BIFRED converter using the proposed control method. As shown in Fig. 11, the waveform of the input line current is nearly a sinusoidal waveform, maintaining the high power factor.

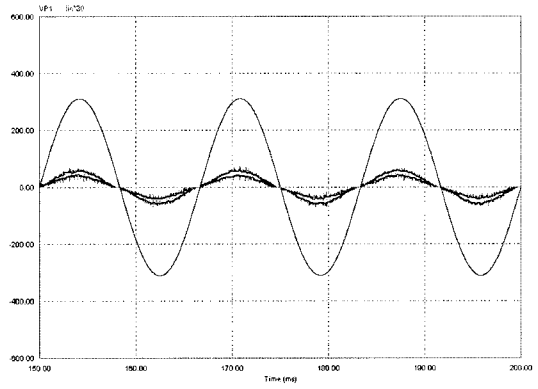
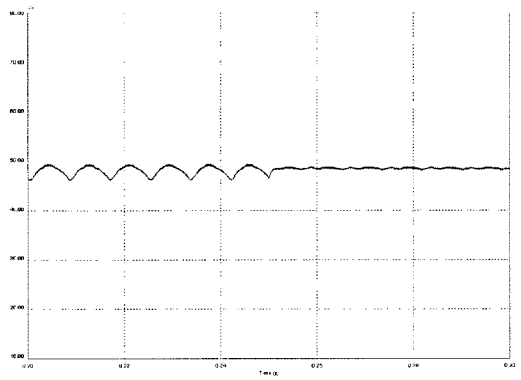
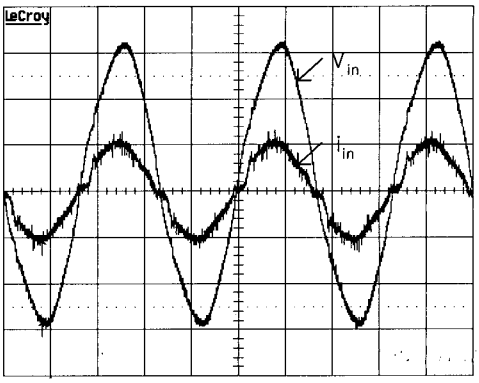


Fig. 9 Input voltage and input current(×30) waveform in CCM BIFRED converter



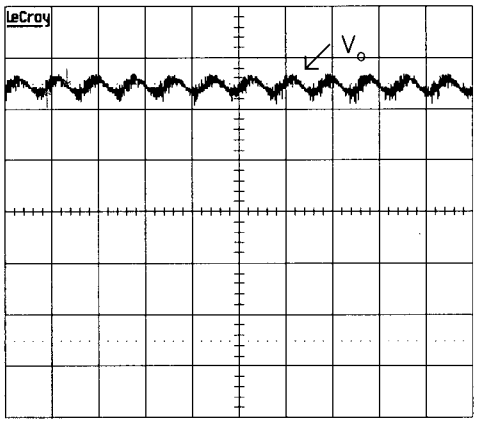
[10V/div, Time : 50ms]

Fig. 10 With proposed control method (at 250ms) in CCM BIFRED converter



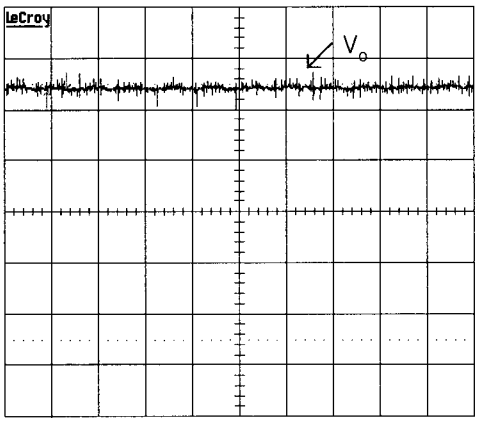
[100V/div, 2A/div, Time : 5ms]

Fig. 11 Input voltage and input current waveform BIFRED converter



[20V/div, Time : 10ms]

(a) Without proposed control method



[20V/div, Time : 10ms]

(b) With proposed control method

Fig. 12 Output voltage waveform in BIFRED converter

Fig. 12 shows the experimental result of the DC output voltage waveforms. Fig. 12(a) shows the DC output voltage waveform without the proposed control scheme. In this case the DC output voltage ripple is about 7%. Fig. 12(b) shows the DC output voltage waveform with the proposed control method. It is said in this figure that the low frequency ripple component is relatively reduced when the proposed ripple suppression scheme is applied.

As these results show, the validity of the proposed rectifier with the high power factor and the output voltage ripple suppression is verified. Table 2 shows that the BIFRED converter using the proposed control method performs better than the existing BIFRED.

Table 2 Comparison of the BIFRED Converter.

BIFRED	Power factor	Energy storage capacitor	Output ripple voltage
Conventional	high	220u	1%
With small-sized energy storage capacitor	high	20u	7%
Using proposed control method	high	20u	1%

5. Conclusions

The DC ripple voltage suppression scheme in BIFRED converter with a small-sized energy storage capacitor is presented in this paper. In addition, the validity of the proposed scheme was varified through the simulation results. The advantages of the proposed technique are as follows.

- High power factor and regulated DC output voltage.
- Small fluctuation against the step change of the load and input voltage.
- Simple control circuit for DC ripple suppression.
- Small-sized energy storage capacitor compared with the conventional BIFRED converter.
- Small size and low cost.

It has been shown that the BIFRED converter with the small-sized energy storage capacitor can be employed in applications requiring a well regulated output voltage and power factor correction.

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