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A Novel Boost-Input Full-Bridge Converter

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ABSTRACT

In order to correct the power boost topology has been used for easy control. But conventional boost topology has the following drawbacks: switching voltage surge, cross conduction current and right-half-plane zero of its control transfer function. Furthermore, in this topology the output voltage is always higher than the input voltage. As a result, a first-stage boost PFC converter needs to be connected with a second-stage DC-DC converter. A new topology which can be used as single stage PFC converter is proposed in this paper.

Keywords: Single-Stage, PFC, ZVS

1. Introduction

The conventional boost topology has the following drawbacks: high output voltage, cross conduction current, and a right-half-plane zero of the control transfer function.

This paper proposes a new topology to overcome these drawbacks. Two boost converters operating in an interleaving manner are connected in parallel, and four switches used in these boost converters with synchronous rectification derive an equivalent full- bridge converter by combining a transformer. This novel converter provides the following prominent features: small current ripple in both the input and the output sides, disappearance of right-half-plane zero under a certain parameter value, and availability of an arbitrary low voltage output. The steady-state and the dynamic characteristics are analyzed in this paper. The analysis confirms that the novel converter provides ZVS operation, small input current ripple, and high efficiency.

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2. Drawbacks of a Conventional Boost Converter

In a conventional boost converter, the output voltage is always higher than the input voltage. When the output voltage is required to be lower than the input voltage, it is necessary to use a buck, forward, half-bridge, or full-bridge converter as the second stage. As the result, the power efficiency is decreased. Furthermore, these two converters operating at different switching frequencies cause a beat-frequency phenomenon which cannot be suppressed by the output filter. To overcome these above drawbacks, this paper proposes a boost-input-type full-bridge converter topology.

3. Boost-Input Type Full-Bridge Converter

Figure 1 shows the circuit configuration of the proposed boost-full-bridge converter composed of two boost converters operating in an interleaving manner, where MOSFET switches are utilized instead of rectifying diodes and a transformer is used to build a full-bridge converter. Figure 2 illustrates the time chart of four switches S_1, S_2, S_3, and S_4. S_1 and S_3 are driven in a complimentary, interleaving manner, as are S_2 and S_4. In this topology, the ZVS operations of all switches are achieved. The steady-state and the dynamic characteristics of this converter are derived by applying the state-space-averaging method[1,2].

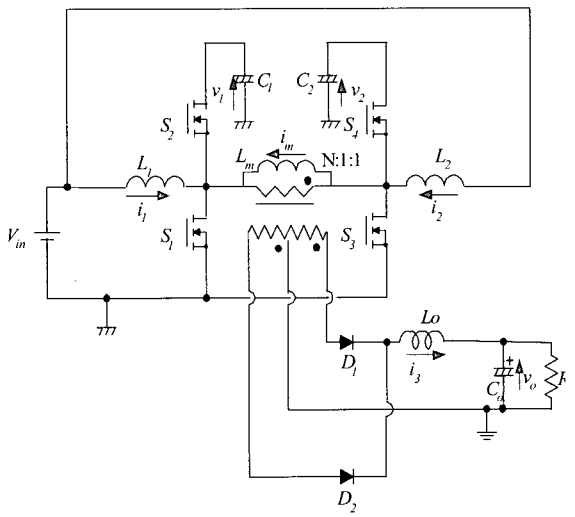

Fig. 1 Proposd Boost-Input Full-Bridge Converter

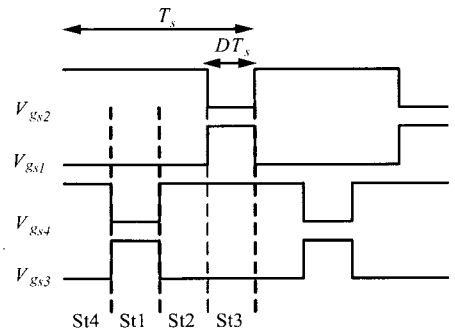

Fig. 2 Time Chart of Gate-Drive Signals for Four MOSFET Switches

4. State-Space Averaged Analysis

4.1 Basic Differential Equations

(a) In the case of $D<0.5$:

First, the division of circuit states is shown in Fig. 2. Second, the state variables are selected as shown by eq.(1). Then, a state-space differential equation and an output equation are derived correspondingly to each state as shown by eqs.(2) and (3), respectively.

$$\vec{x} = (i_1 \quad i_3 \quad v_{c1} \quad v_{co})^T \qquad \vec{y} = (i_1 \quad i_3 \quad v_1 \quad v_o)^T \tag{1}$$

$$\frac{d\vec{x}}{dt} = A_k \vec{x} + \vec{b}_k Vin \tag{2}$$

$$\vec{y} = g_k \vec{x} \tag{3}$$

$$A_1 = \begin{pmatrix} -\frac{r_s + r_1}{L} & -\frac{r_s}{NL} & 0 & 0 \\ \frac{r_c - r_s}{NL_o} & -\frac{r_\beta}{L_o} & \frac{1}{NL_o} & -\frac{R_o}{L_o r_\alpha} \\ 0 & 0 & 0 & 0 \\ 0 & \frac{R_o}{C_o r_\alpha} & 0 & -\frac{1}{C_o r_\alpha} \end{pmatrix} \tag{4}$$

$$A_2 = \begin{pmatrix} -\frac{r_c + r_1}{L} & -\frac{r_c}{NL} & -\frac{1}{L} & 0 \\ 0 & -\frac{r_\gamma}{L_o} & 0 & -\frac{R_o}{L_o r_\alpha} \\ \frac{1}{C} & \frac{1}{NC} & 0 & 0 \\ 0 & \frac{R_o}{C_o r_\alpha} & 0 & \frac{-1}{C_o r_\alpha} \end{pmatrix} \tag{5}$$

$$A_3 = \begin{pmatrix} -\frac{r_c + r_1}{L} & \frac{r_c}{NL} & -\frac{1}{L} & 0 \\ \frac{r_c - r_s}{NL_o} & -\frac{r_\beta}{L_o} & \frac{1}{NL_o} & -\frac{R_o}{L_o r_\alpha} \\ \frac{1}{C} & -\frac{1}{NC} & 0 & 0 \\ 0 & \frac{R_o}{C_o r_\alpha} & 0 & -\frac{1}{C_o r_\alpha} \end{pmatrix} \tag{6}$$

$$A_4 = \begin{pmatrix} -\frac{r_c + r_1}{L} & \frac{r_c}{NL} & -\frac{1}{L} & 0 \\ 0 & -\frac{r_\gamma}{L_o} & 0 & -\frac{R_o}{L_o r_\alpha} \\ \frac{1}{C} & -\frac{1}{NC} & 0 & 0 \\ 0 & \frac{R_o}{C_o r_\alpha} & 0 & -\frac{1}{C_o r_\alpha} \end{pmatrix} \tag{7}$$

$$b_1 = b_2 = b_3 = b_4 = \begin{pmatrix} \frac{1}{L} & 0 & 0 & 0 \end{pmatrix}^T \tag{8}$$

$$g_1 = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & \frac{R_o r_{co}}{r_\alpha} & 0 & \frac{R_o}{r_\alpha} \end{pmatrix} \tag{9}$$

$$g_2 = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ r_c & \frac{r_c}{N} & 1 & 0 \\ 0 & \frac{R_o r_{co}}{r_\alpha} & 0 & \frac{R_o}{r_\alpha} \end{pmatrix} \tag{10}$$

$$g_3 = g_4 = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ r_c & -\frac{r_c}{N} & 1 & 0 \\ 0 & \frac{R_o r_{co}}{r_\alpha} & 0 & \frac{R_o}{r_\alpha} \end{pmatrix} \tag{11}$$

$$\begin{aligned} r_\alpha &= R_o + r_{co} \\ r_\beta &= \frac{r_c + r_m + r_s}{N^2} + r_{Lo} + \frac{R_o r_{co}}{r_\alpha} \\ r_\gamma &= \frac{2r_c + r_m}{N^2} + r_{Lo} + \frac{R_o r_{co}}{r_\alpha} \end{aligned} \tag{12}$$

Applying the state-space-averaging method to the above-mentioned equations, a state-space averaged equation and an averaged output equation are obtained as shown by eqs.(13) and (14), respectively.

$$\frac{d\bar{x}}{dt} = A\bar{x} + bV_{in} \tag{13}$$

$$\bar{y} = g\bar{x} \tag{14}$$

$$A = DA_1 + (0.5 - D)A_2 + DA_3 + (0.5 - D)A_4 \tag{15}$$

$$b = Db_1 + (0.5 - D)b_2 + Db_3 + (0.5 - D)b_4 \tag{16}$$

$$g = Dg_1 + (0.5 - D)g_2 + Dg_3 + (0.5 - D)g_4 \tag{17}$$

where,

i_1, i_3, v_1, and v_o : as shown in Fig.1,

v_{c1} and v_{co} : Capacitance voltage without ESR,

k : 1, 2, 3 and 4,

r_{r1}: Parasitic resistance of primary stage inductor,

r_{Lo}: Parasitic resistance of secondary stage inductor,

r_m: Parasitic resistance of transformer,

r_c: ESR of primary stage capacitor,

r_{co}: ESR of secondary stage capacitor,

r_s: ON resistance of MOSFET

D: Duty ratio of the switches S_1 and S_3

N: Turns ratio of transformer windings.

4.2 Steady-State Characteristics

Assuming that the derivative of (13) is zero, the steady-state characteristics are obtained. As a result, the voltage conversion ratio is expressed as eq.(18), where parasitic resistances associated with switches, inductors, transformer, and capacitors are neglected for simplicity.

$$\frac{V_o}{V_{in}} = \frac{2D}{N(1-D)} \tag{18}$$

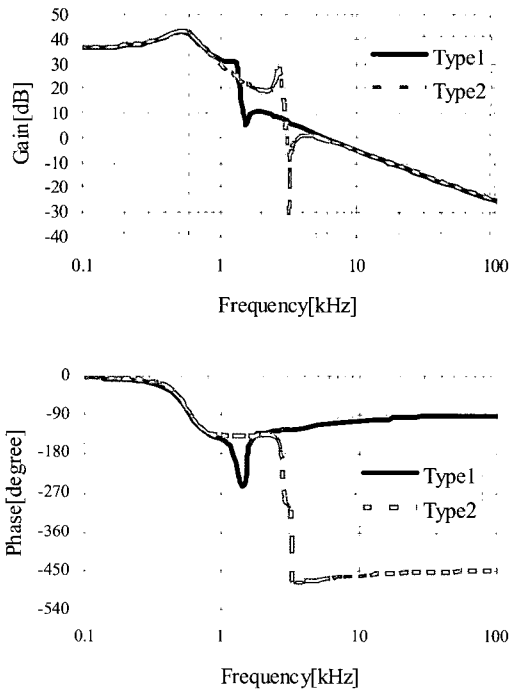

Fig.3 Bode Diagram for Two Cases of Tranfer Function with Different Parameters.

Type 1 : r_c=0.2[Ω] and C=44[μF]

Type 2 : r_c=0.01[Ω] and C=10[μF]

Common parameters for both cases: r_s=0.4[Ω], r_1=r_m=r_{Lo}=0.01[Ω], r_{co}=0.05[Ω], L=160[μH], L_o=60[μH], C_o=1200[μF], R_o=12[Ω], N=4, D=0.35 and V_{in}=140[V]

(b) In the case of D>0.5 :

The voltage conversion ratio in this case is derived by the same procedure as the previous one, and is expressed as

$$\frac{V_o}{V_{in}} = \frac{2}{N} \tag{19}$$

Hence the conversion ratio does not depend on the duty ratio when D>0.5. Therefore, the duty ratio is required to be smaller than 0.5 for the output regulation.

4.3 Dynamic Characteristics

Applying the perturbations to the variables around their steady-state values such as $\overline{x} \to X + \Delta X$, $\overline{y} \to Y + \Delta Y$, and $D \to D + \Delta D$, a linearized small-signal model for D<0.5 is obtained as follows:

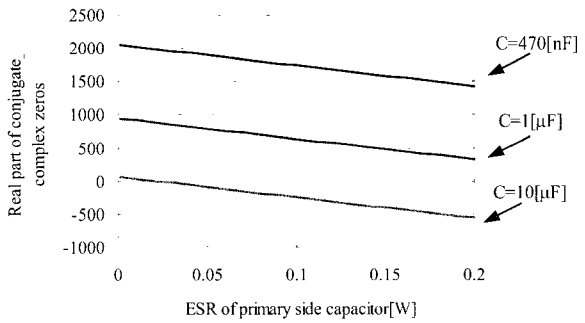

Fig. 4 Effect of ESR of Primary-side Capacitor on the Real Part of Conjugate Complex Zeros

$$\Delta X(s) = (s - A)^{-1}(\frac{\partial A}{\partial D} X + \frac{\partial b}{\partial D} V_{in})\Delta D(s) \tag{20}$$

$$\Delta Y(s) = g\Delta X(s) + \frac{\partial g}{\partial D} X \Delta D(s) \tag{21}$$

$$\frac{\partial A}{\partial D} = A_1 - A_2 + A_3 - A_4 \tag{22}$$

$$\frac{\partial b}{\partial D} = b_1 - b_2 + b_3 - b_4 \tag{23}$$

$$\frac{\partial g}{\partial D} = g_1 - g_2 + g_3 - g_4 \tag{24}$$

Furthermore, the control transfer function of this converter is derived as follows:

$$\frac{\Delta Vo(s)}{\Delta D(s)} = \frac{K(s^3 + \alpha s^2 + \beta s + \gamma)}{\{1 + 2\xi_1(\frac{s}{\omega_1}) + (\frac{s}{\omega_1})^2\}\{1 + 2\xi_2(\frac{s}{\omega_2}) + (\frac{s}{\omega_2})^2\}} \tag{25}$$

where

ω_1 : First peak frequency,

ω_2 : Second peak frequency,

ξ_1 : Damping factor of first peak,

ξ_2 : Damping factor of second peak,

K, α, β, γ : Constant value.

The converter stability can be estimated by examining whether one of three zeros represented by this control transfer function is located in the right-half plane or not. Figure 3 compares two cases of the frequency characteristics: Type 1 is the transfer function without any right-half-plane zeros, and Type 2 is with a right-half-plane zero. The location of these zeros strongly depends on parasitic resistances. The effect of ESR of the primary-side capacitors on the location of zeros is shown in Fig.4, where the real part of the conjugate complex zeros of the transfer function is examined. It shows that the decrease of the ESR of the primary-side capacitors causes converter instability, and that a larger capacitance is needed to assure converter stability.

5. Experiment

In order to evaluate the performance of this converter experimentally, a breadboard was implemented using the following specifications and parameters:

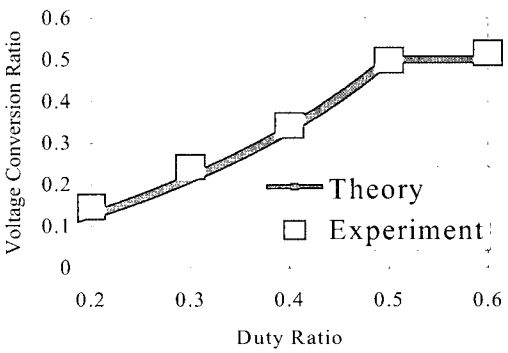

Fig. 5 Voltage Conversion Ratio vs. Duty Ratio

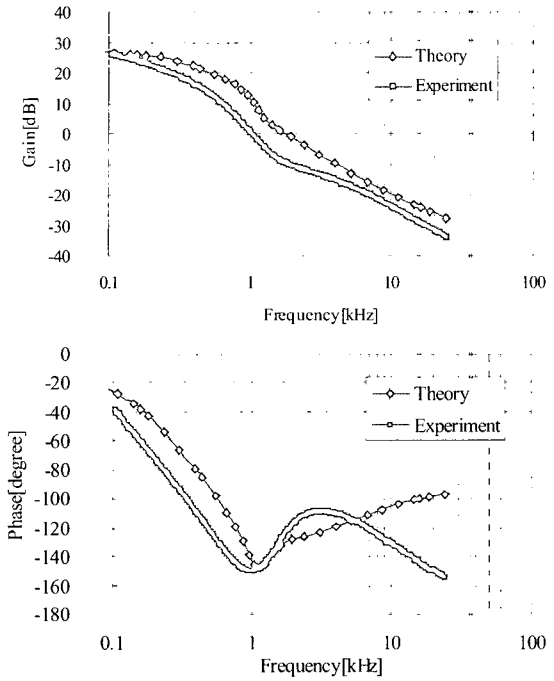

Fig. 6 Bode Diagrams of the Control Transfer Function

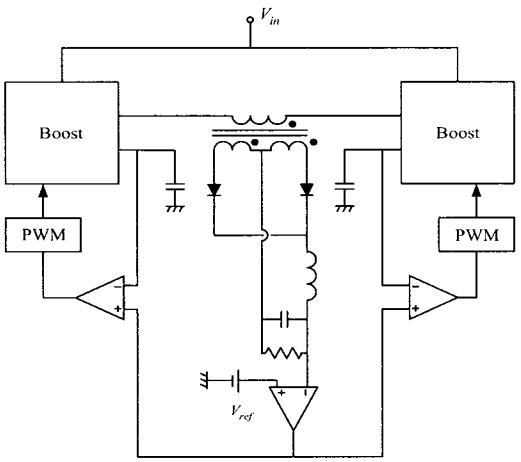

Fig. 7 Block Diagram of Double Feedback loops

V_{in}=140[V], f_s=200[kHz], L_1=L_2=160[μH], C_1=C_2=44[μF], L_o=60[μH], C_o=1200[μF], N=4.

Figure 5 shows the relation of the voltage conversion ratio and the duty ratio, and Figure 6 illustrates Bode plots of the control transfer function. The analytical and experimental results are compared, respectively, and a good agreement is obtained.

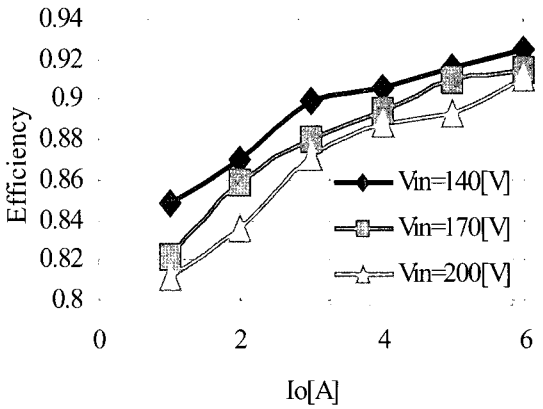

Fig. 8 Power Efficiency (Vo=48[V])

In practical applications, a transformer should be protected from the asymmetrical magnetization, so the voltage across the primary-side capacitor is regulated to be equal to each other as shown in Fig.7, where double feedback loops are used for the output voltage and the voltage across the primary-side capacitors. The experimental results measuring power efficiency are shown in Fig.8, where Vin =140 to 200V, Vout=48V, and Io= 1 to 6A. A high efficiency of over 90% was obtained for the output power of 300W.

6. Conclusion

A novel topology of boost-input full-bridge converters has been proposed. The steady-state and dynamic characteristics were analyzed by using the state-space averaging method and were experimentally confirmed. It is predicted that the application of this converter to a power-factor-correction converter derives some prominent features. This work will be pursued in the future.

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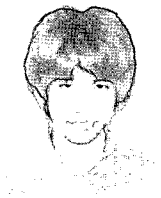

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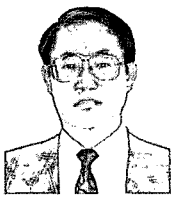

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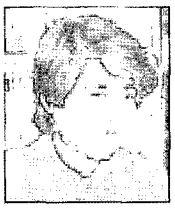

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