# A Wideband Down-Converter for the Ultra-Wideband System

# 초광대역 무선통신시스템을 위한 광대역 하향 주파수 변환기 개발에 관한 연구

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## Abstract

In this paper, we propose a direct conversion double-balanced down-converter for MB-OFDM UWB system, which is implemented using 0.18 $\mu$m CMOS technology and its measurement results are shown. The proposed down-converter adopts a resistive current-source instead of general transconductance stage using MOS transistor to achieve wideband characteristics over RF input frequency band 3~5 GHz with good gain flatness. The measured conversion gain is more than +3 dB, and gain flatness is less than 3 dB for three UWB channels. The dc consumption of this work is only 0.89 mA from 1.8 V power supply, leading to the low-power UWB application.

## 요 약

본 논문은 MB-OFDM UWB 시스템에 적용할 수 있는 직접 변환 방식용 하향 주파수 변환기 구조를 제안한다. 제안하는 주파수 변환기 구조는 3~5 GHz 광대역 입력 매칭을 하기 위해 일반적으로 CMOS로 구성된 트랜스컨덕턴스 회로를 사용하지 않고, 저항을 사용하였다. 하향 주파수 변환기는 0.18 $\mu$m CMOS 공정으로 구현하였으며, 측정 결과 3개의 UWB 채널에 대하여 최소 +3 dB의 주파수 변환 이득과 각각 3 dB 이하의 게인 평탄도를 보이며, 1.8 V dc Power supply에서 0.89 mA를 소비한다.

Key words : Ultra-Wideband, UWB, CMOS, Down-Converter, Mixer

## Ⅰ. Introduction

The ultra-wideband(UWB) system has emerged a new high data-rate communication system for high multimedia service. Recently, The Federal Communications Commission(FCC) has newly defined UWB devices as one that have a fractional bandwidth more than 20 % of its carrier frequency or an absolute bandwidth of more than 500 MHz[1]. The whole bandwidth of UWB system is 3.1~10.6 GHz, and the spectrum shape of transmitted power and maximum transmitted power level are limited(-41.3 dBm/MHz). Recently, two UWB system approaches for the wireless personal area network(WPAN) use the carrier frequency like conventional wireless systems[2]: MB-OFDM(Multi-Band Orthogonal Frequency Division Multiplexing) and DS-CDMA(Direct-Sequence Code Division Multiple Access) approach. MB-OFDM approach has inherent robustness against narrowband interferers and multi-path environments, compared to DS-CDMA approach. In addition, the MB-OFDM approach divides the full 7 GHz UWB frequency band(3.1~10.6 GHz) into several

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528 MHz sub-band channels to enable multiple modes of operations, and adopts frequency/time-hopping methods for multiplexing. Therefore, the MB-OFDM approach can use its frequency band more flexibly so that hardware implementations can be flexibly developed as technology advances. The lowest frequency band(3.1～4.9 GHz) among full UWB band in MB-OFDM approach, which also can provide up to 480 Mbps, has been allocated for the development of the first generation device. The CMOS technology can be an adequate choice for the implementation of this lowest band UWB system, when considering time to market, hardware cost, degree of difficulty, etc. In this paper, we propose a direct-conversion CMOS down-converter, which can cover the lowest band(3～5 GHz) in MB-OFDM UWB system, and its measurement results are shown. Measurement results show good gain flatness over three channels with bandwidth of 528 MHz and very low dc power consumption.

## Ⅱ. Design and Measurement

The transceiver for MB-OFDM UWB system can be implemented by using heterodyne or direct conversion architecture. The direct conversion architecture has advantages of high integration, low power, low cost, and so on, despite of its some inherent drawbacks(*I*/*Q* mismatch, dc-offset, 1/*f* and so on), compared to the heterodyne architecture.

Fig. 1 shows direct-conversion receiver architecture for MB-OFDM UWB system. Incoming RF signals, which have three channels(3,432, 3,960, and 4,488 MHz) with their channel bandwidth of 528 MHz, are amplified by low noise amplifier(LNA), and then down-converted to the baseband by *I*/*Q* down-converter (mixer). Unlike conventional wireless system, in MB-OFDM system, three *I*/*Q*-LO signals are provided from off-chip sub-band generator(SBG) with the switching time less than 9.5 nsec. The power level of the down-converted baseband signal is required to have good flatness over channel bandwidth. In this work, the *I*/*Q* down-converter is designed and implemented based on 0.18 $\mu$m CMOS technology.

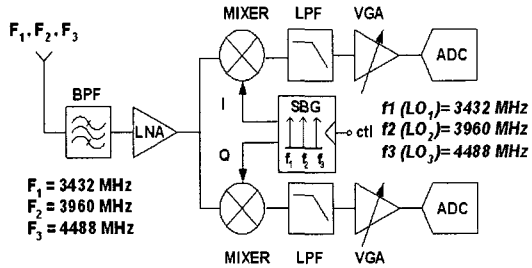



Fig. 1. Direct conversion receiver for MB-OFDM.

Fig. 2 shows the proposed CMOS down-converter for the direct conversion UWB receiver, where the topology of down-converter in *I*-path is only shown. The detailed bias circuit is omitted in Fig. 2. The down-converter adopts the double-balanced topology to have high immunity for common-mode noises at high frequency range and even-order distortion for high IP2 performance in direct conversion receiver. In Fig. 2, the incoming RF signals(3～5 GHz) are applied to the common-source node of switching transistors($M_1$, $M_2$, $M_3$, and $M_4$) and then down-converted by the switching operation of switching transistors for three LO frequencies(3,432, 3,960, and 4,488 MHz).

For UWB applications, the down-converter is required to have wideband characteristics and gain flatness for each three channel. In a general CMOS down-converter, the transconductance stage consists of MOS

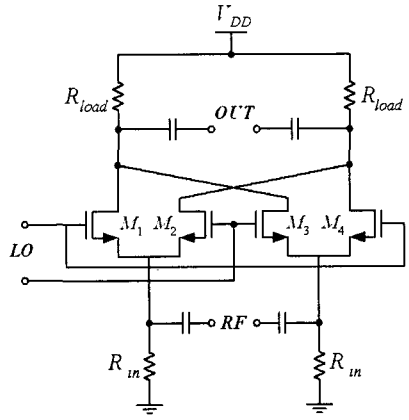



Fig. 2. Schematic of proposed down-converter.

transistors, so that input impedance of the transconductance stage is very capacitive at high frequency range, leading to the requirement of a complicated input wideband matching circuit. To overcome this problem, in this work, the incoming RF signals, after being amplified by LNA, are directly applied to the source node of switching transistors($M_1$, $M_2$, $M_3$, and $M_4$), without using the transconductance stage. Two resistors $R_{in}$ in Fig. 2 work as a current source. for the double-balanced down-converter. The differential input impedance in Fig. 2 can be expressed $1/g_m$, leading to wideband input matching without any additional matching circuit, where $g_m$ is the transconductance of switching transistors $M_1$, $M_2$, $M_3$, and $M_4$, This connection also can considerably reduce low frequency even-order nonlinearity from transconductance stage, leading to high IP2 performance. In Fig. 2, P-type poly resistor $R_{load}$ is used for output load of the double-balanced mixer to reduce $1/f$ noise at base-band frequency range and to provide wideband frequency response characteristics for the down-converted signal. From gain-bandwidth theory, the value of resistor $R_{load}$ is limited[3].

Fig. 3 shows the test board for $I/Q$ down-converter. All measurements are performed for the down-converter in $I$-path. The fabricated CMOS chip is packaged(MLF RF package) and mounted on the FR-4 PCB for measurements. RF, LO and IF ports are matched to 50 ohm with resistor on the PCB and a passive hybrid balun is used to convert the single-ended RF and LO signal provided from a signal generator into differential signals. Fig. 4 shows the measured conversion gain of the proposed down-converter for each channel.

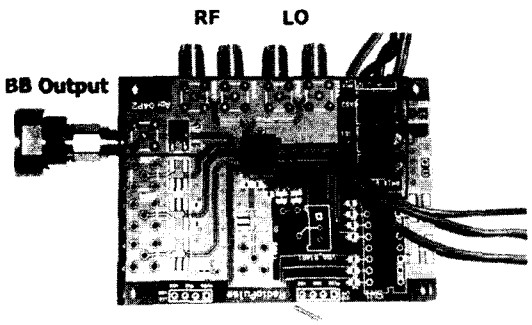
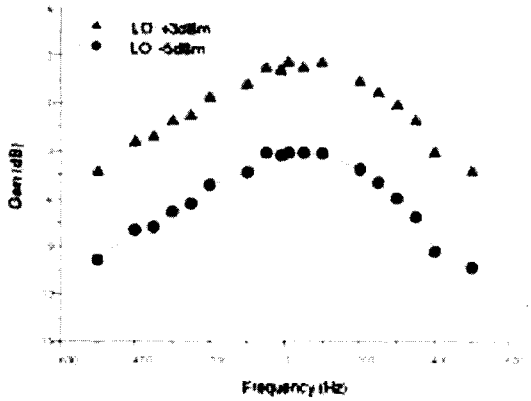
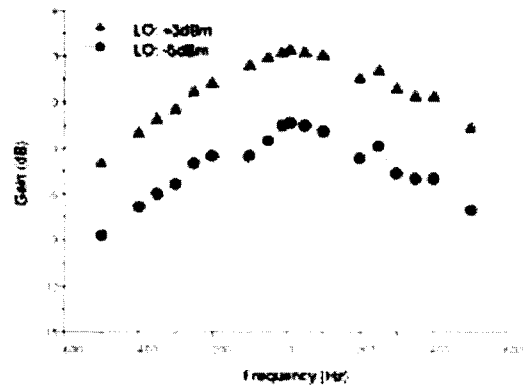



Fig. 3. Photograph of test board.

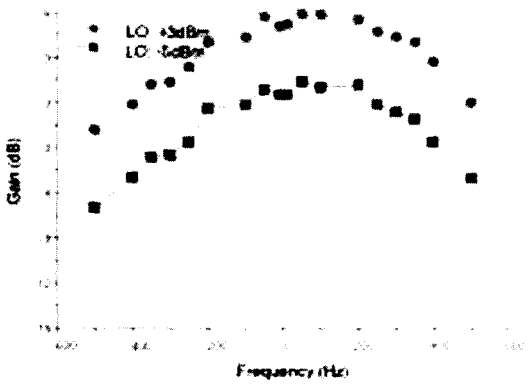
The measured peak conversion gain of down-converter is about +3 dB for channel 1 and 2, and +6 dB




(a) Channel 1




(b) Channel 2




(C) Channel 3

Fig. 4. Conversion gains for three channels.

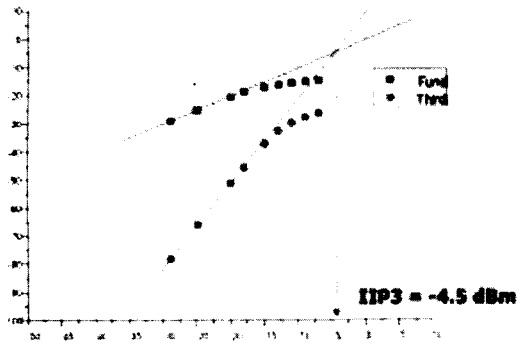



Fig. 5. $P_{1dB}$ and IP3 for channel 2.

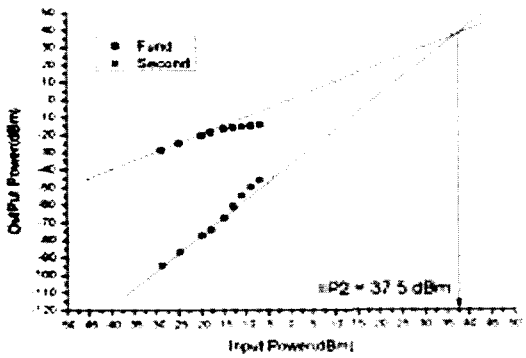



Fig. 6. IP2 for channel 2.

for channel 3, respectively, when the LO power level is +3 dBm.

The gain flatness is less than 3 dB over channel bandwidth of 528 MHz for all three channels. Fig. 5 shows the measured input referred 1 dB compression point and IP3 for channel 2 at RF1 = 3,955 MHz and RF2 = 3,965 MHz. The input 1 dB compression point is −14 dBm and IP3 is −4 dBm. Fig. 6 shows the measured IP2 of +37.5 dBm for channel 2. The measured IP2 value degrades compared to simulation results due to devices mismatch of layout and non-ideal RF/LO differential signal generated from an off-chip balun for the measurement. Table 1 shows the summary of measurement results of the proposed down-converter in Fig. 2.

## Ⅲ. Conclusion

Table 1. Summary of measurement results.

| | | |
|---|---|---|
| Conversion gain / Flatness | 3 dB / < 3 dB | Channel 1 |
| | 3 dB / < 3 dB | Channel 2 |
| | 6 dB / < 3 dB | Channel 3 |
| Input $P_{1dB}$/ IP3 /IP2 (dBm) | −14.7/ −8.8/ +27.0 | Channel 1 |
| | −14.0/ −4.5/ +37.5 | Channel 2 |
| | −16.0/ −8.9/ +17.5 | Channel 3 |
| Input return loss | > 13 dB | For all channels |
| Noise figure | 17~21 dB | For all channels |
| LO-IF isolation | > 43.5 dB | Fo rall channels |
| LO-RF isolation | > 56 dB | For all channels |
| RF-IF isolation | > 46.3 dB | For all channels |
| DC power | 0.89 mA @1.8 V | |

A CMOS direct conversion down-converter for UWB system is proposed and its measurement results are shown. The implemented down-converter can achieve wideband input matching without any passive matching network over 3~5 GHz frequency range. The measurement results show conversion gain of +3 dB for channel 1, 2 and +6 dB for channel 3. For three channels, gain flatness is less than 3 dB. This work consumes only 0.89 mA from a 1.8 V power supply. Finally, the proposed double-balanced down-converter is suitable for low power UWB application.

## References

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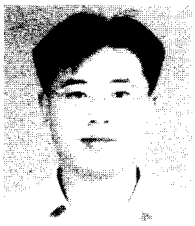

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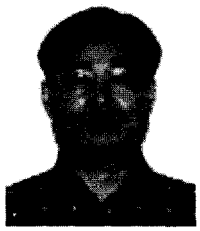

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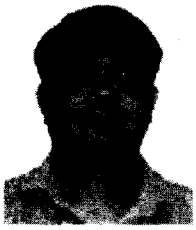

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