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a-Si TFT Integrated Gate Driver Using Multi-thread Driving

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Abstract

A novel a-Si TFT integrated gate driver circuit using multi-thread driving has been developed. The circuit consists of two independent shift registers alternating between the two modes, "wake" and "sleep". The degradation of the circuit is retarded because the bias stress is removed during the sleep mode. It has been successfully integrated in 14.1-in. XGA LCD Panel, showing enhanced stability.

Keywords : a-Si TFT, integrated gate driver, instability, multi-thread, clamping voltage, TFT-LCD

1. Introduction

Integrating driver circuits using a-Si TFTs on glass is drawing increased attention in LCD technology since fabrication cost can be reduced by eliminating driver ICs and related processes. Attempts have been made to fabricate the integrated circuits with a-Si TFTs at early stages of a-Si TFT development [1,2]. It has become possible to apply gate driver circuitry on glass with a-Si TFTs with recent efforts though it is not mature enough for main stream products [3-6].

Instability of a-Si is a major difficulty that makes difficult to obtain stable circuits using a-Si TFTs. The degradation of a-Si TFT is inevitable when they deviate from as-deposited equilibrium because of applied bias voltage [7]. Usually, bias-stressed a-Si TFTs show an increase in threshold voltage with time. Thus, the circuits using a-Si TFT have limited life time because of the degradation of constituent TFTs. The insufficient life time of circuits was the critical barrier to prevent a-Si TFT driver integration from being practical technology.

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It has been reported that the degradation of a-Si circuits can be slowed down by relieving bias stress through AC driving [4,8]. The gate driver circuits with AC-driven pull-down transistor show markedly slow degradation. The circuits have relatively complicated structure for controlling the node voltages. In this study, a recent advancement in the design of a-Si gate driver circuit using multi-thread driving is introduced, in which simple conventional DC-type circuits are used.

2. Instability of a-Si Gate Driver Circuits

Fig. 1 is the block diagram of a unit of a conventional

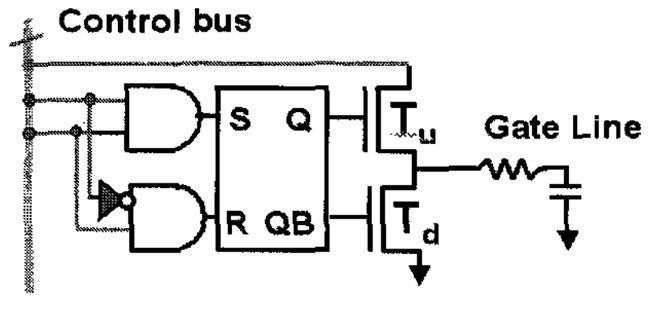

Fig. 1. (a) Schematic block diagram of a conventional gate driver unit and (b) voltage of QB node in the circuit. Nearly DC gate bias is applied to QB node

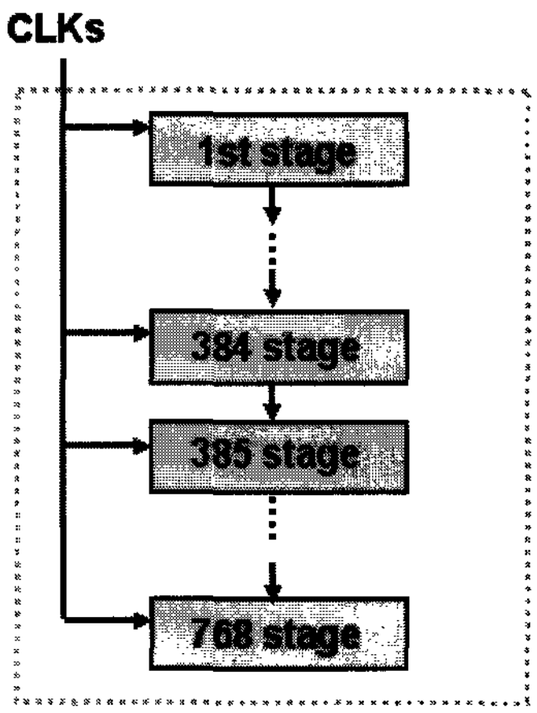

Fig. 2. Block diagram of a conventional gate driver comprising 768 stages for XGA.

gate driver using a-Si TFTs. The a-Si:H gate driver is functionally a shift register consisting of unit stages having their own output terminals (Fig. 2). Each stage gives high voltage output during one horizontal time in one frame time, maintaining the gate line connected to it at high voltage state while pixels controlled by the gate line are charged to certain data levels. After the pixels are charged, the gate line must have low voltage to keep the stored charges in the pixels until the next scan time. Thus, for TFT-LCDs, the gate lines are maintained at low voltage almost all the time during operation.

The pull-up transistor (Tu) is presumed to be in the off-state. When a clock pulse is applied to the pull-up transistor, the fluctuations of the low voltage in the nodes of an inactive stage occur. Current can flow through the pull-up transistor owing to the voltage fluctuation at the Q node by capacitive coupling with the clock pulse. To stabilize the low voltage of gate lines, the pull-down transistor is maintained in a conducting state. It is required that the QB node in the gate driver is biased high.

The voltage disturbance at the output terminal of the generic shift register was investigated by a continuum shift register model with traveling clock pulses [9]. The clamping voltage is a measure of the onset of an abrupt increase of output voltages given by the sum of the retarded voltage fluctuations from each stages propagating with damping. The degradation of the pull-down transistor weakens the damping and accelerates the abnormal behavior of the circuit.

To reduce the stress to the pull-down transistors in the circuit, AC-driving the pull-down transistors has been suggested. The a-Si:H driver circuits with AC- driven dual pull-down structure (DAC) and AC-driven single pull-down structure (SAC) have been reported to have enhanced stability [4,8]. It is desirable that the bias stress to the QB node is reduced in gate drivers using a-Si:H TFTs.

3. Multi-thread Driving

The gate driver in this study consists of two independent shift registers. Each shift register is a conventional DC circuit having separate controls and clocks. We call the independent shift register in the gate driver a "thread". The main idea of the circuit is that multiple threads form a gate driver and a thread that need not operate is exempt from any bias stress. The clocks and controls are maintained in low voltage state when the thread is in the "sleep mode". The threads in the gate driver are switched between the "wake" mode and "sleep" mode.

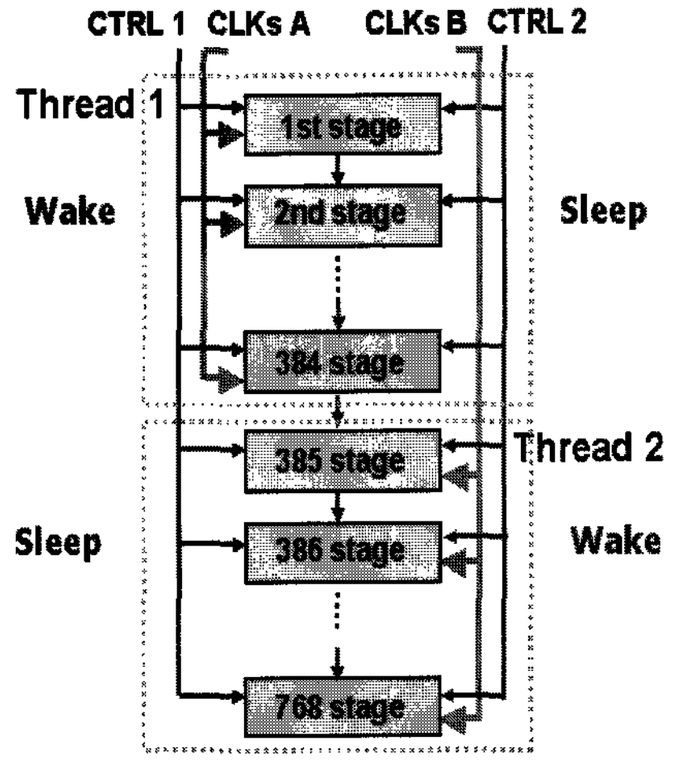

Fig. 3. Block diagram of a gate driver comprising two independent shift registers.

Fig. 3 is a block diagram of a gate driver for XGA panel, comprising two independent shift registers (thread 1 and 2). The first shift register (thread 1) has 384 unit stages for driving the upper half panel. The second shift register (thread 2) also has 384 unit stages for driving the lower half panel. Each shift register has independent clocks and controls.

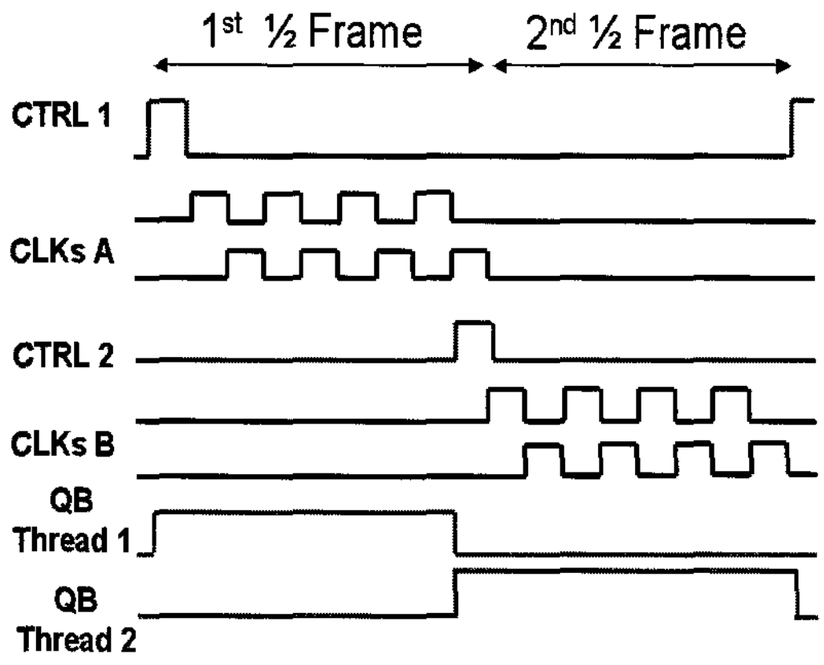

Fig. 4. Timing diagram for the gate driver using multi thread driving.

Fig. 4 shows the timing diagram of the controls and clock signals. When thread 1 is working, thread 2 is sleeping with the controls and clocks in the low voltage state. The inner nodes of thread 2 are also in the low voltage state. Thus, the bias stress is stopped in this sleep mode. After the 384-th stage of thread 1 gives an output, thread 1 sleeps and thread 2 wakes up and starts operating. When thread 1 is in sleep mode, the nodes are cleared and have low voltage. The two threads wake up and sleep alternately, accomplishing multi-thread driving.

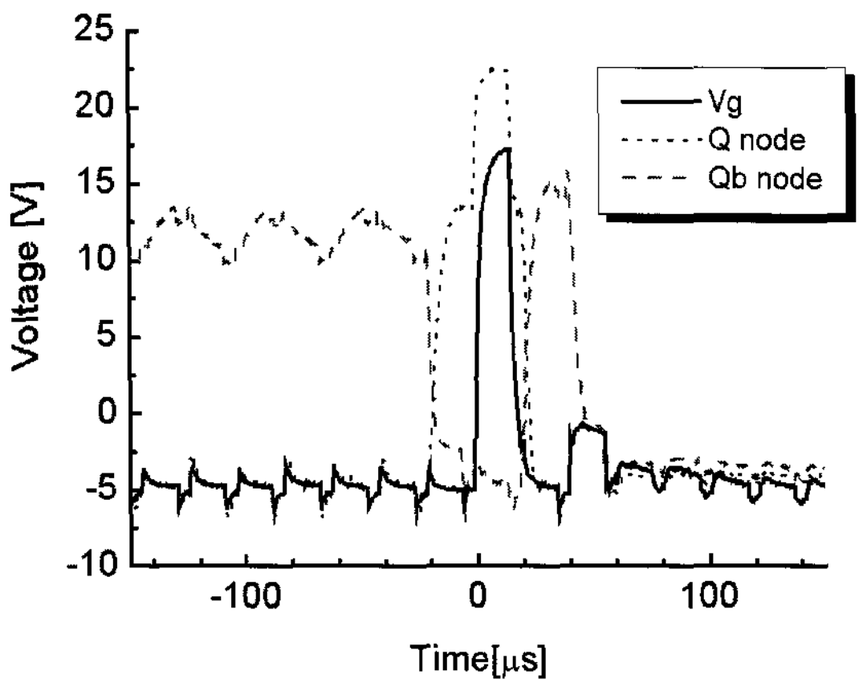

Fig. 5. Voltage at the nodes of 382-th shift register unit while thread 1 is scanning upper half panel.

Fig. 5 shows the measured voltage of the nodes of 382-th stage in the upper shift register (thread 1) of a 768-stage gate driver. The Q node and QB node are the gate electrode of the pull-up transistor and pull-down transistor of the shift register unit, respectively (Fig. 1)

The QB node is maintained at the low voltage stage when the thread 2 is operating. All TFTs in the thread 1 are under low voltage condition. This helps release the bias stress to the circuit.

In the design of the circuits for multi-thread driving, the timing of independent signal is taken into consideration. For example, clock lines for each thread may have different loads because of the physical difference of the position. Thread 2 has longer clock lines than thread 1. A clock line is depicted as the equivalent circuit in Fig. 6. It has the resistance R_O+R_L and capacitance C_L. The resistance R_O is different between the clock lines for the two threads because of different length, thus the clock signals applied to the treads may vary.

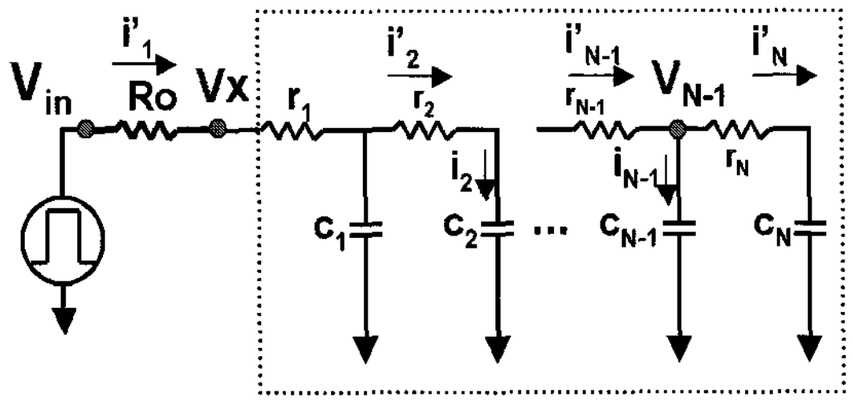

Fig. 6. Equivalent circuit diagram for the clock line.

Let us consider a characteristic time for transmission of the input signal. Applying Kirchhoff's rule to each node of the circuit gives

$$V_{N-1}-V_N = ri'_N = r(i_N)$$
$$V_{N-2}-V_{N-1} = ri'_{N-1} = r(i_N + i_{N-1})$$
$$\cdots$$
$$V_{in}-V_1 = (R_o + r_1)i'_1 = R_o(i_1+\ldots+i_N)+r(i_1+\ldots+i_N)$$
$$\Downarrow$$
$$V_{in}-V_N = R_o(i_1+\ldots+i_N)+r(i_1+\ldots(N-1)i_{N-1}+Ni_N)$$

By integration for the time interval, we obtain

$$\int V_{in}-V_N dt = \int V_{in}dt - \delta_1'(N) = V_{in}T - \delta_1$$
$$= R_0 C_L V_{in} + \frac{N(N+1)R_L C_L V_{in}}{2}$$
$$T = R_0 C_L + \frac{R_L C_L}{2} + \delta_1 \qquad (1)$$

The input clock signal Vx has a characteristic time as

$$\int V_{in} - V_x dt = R_o \int (i_1 + i_2 + ... + i_n) dt$$

$$\int V_{in} dt - \delta'_2 = R_0 c \sum_n V_n$$

$$T = R_0 C_L + \delta_2 \qquad (2)$$

The clocks to the last stage of thread 1 and those to the first stage of thread 2 should have the same characteristics. Neglecting Ro for thread 1 in eq. (1), Ro in eq. (2) should be equal to $R_L/2$.

Although the shift register unit of multi-threaded gate driver has a structure similar to that of the DC gate driver, the degradation is markedly slow because of the stress relieving driving.

Fig. 7 shows that the clamping voltage increases with time when the circuits operate at 60 °C. The conventional DC circuit fails approximately within 200 h. The circuit using multi-thread driving has a much longer life time of over 1000 h.

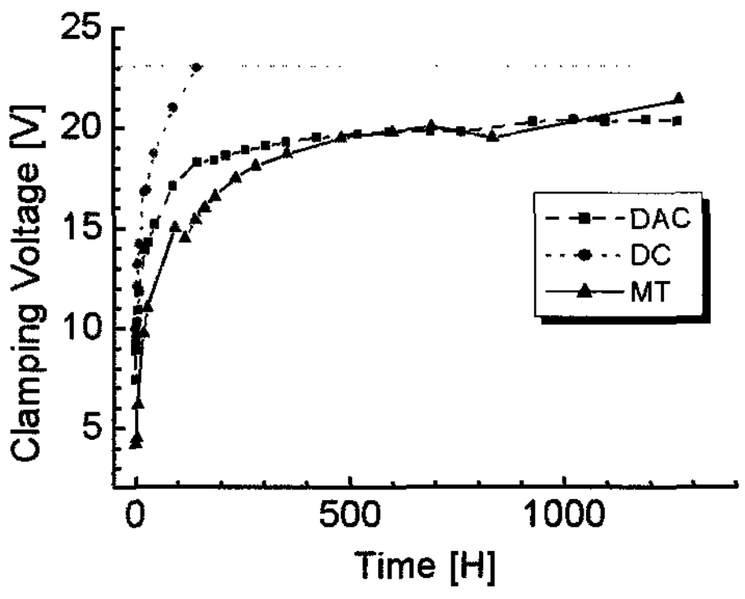

Fig. 7. Clamping voltage of a-Si gate driver using multi- thread driving (MT) vs. time.

Fig. 8 is the photograph of 14.1" XGA panel with the integrated gate driver using multi-thread driving.

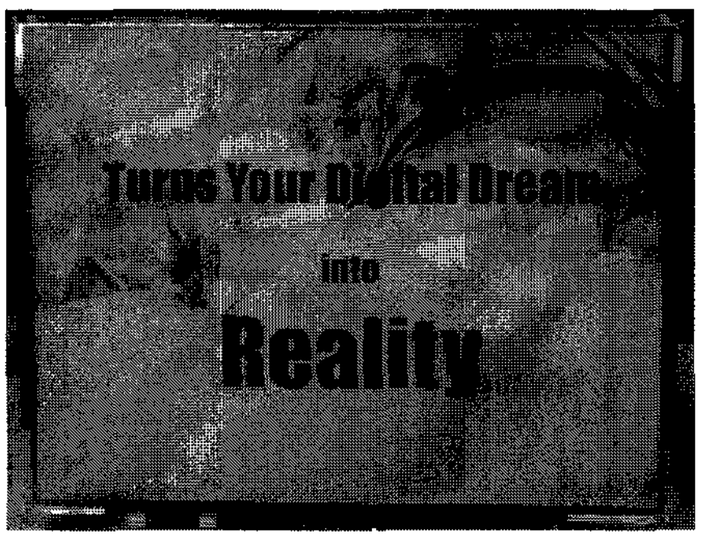

Fig. 8. 14.1" TFT-LCD with integrated a-Si TFT gate driver using multi-thread driving.

4. Conclusion

A novel gate driver using multi-thread driving has been developed to enhance the stability of a-Si circuits caused by the radical threshold voltage shift under bias stress. Each thread, which is independently driven shift register, wakes up and sleeps alternately during panel operation. The thread consists of a simple DC shift register units and needs smaller areas than DAC circuits. The circuit shows enhanced stability. It is also expected to contribute to saving power consumption by making the clocks change to sleep mode.

5. References

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