Hydrogen Ion Implantation Mechanism in GaAs-on-insulator Wafer Formation by Ion-cut Process

Hyung-Joo Woo, Han-Woo Choi, and Joon-Kon Kim

***Abstract*—The GaAs-on-insulator (GOI) wafer fabrication technique has been developed by using ion-cut process, based on hydrogen ion implantation and wafer direct bonding techniques. The hydrogen ion implantation condition for the ion-cut process in GaAs and the associated implantation mechanism have been investigated in this paper. Depth distribution of hydrogen atoms and the corresponding lattice disorder in (100) GaAs wafers produced by 40 keV hydrogen ion implantation were studied by SIMS and RBS/channeling analysis, respectively. In addition, the formation of platelets in the as-implanted GaAs and their microscopic evolution with annealing in the damaged layer was also studied by cross-sectional TEM analysis. The influence of the ion fluence, the implantation temperature and subsequent annealing on blistering and/or flaking was studied, and the optimum conditions for achieving blistering/splitting only after post-implantation annealing were determined. It was found that the new optimum implant temperature window for the GaAs ion-cut lie in 120~160°C, which is markedly lower than the previously reported window probably due to the inaccuracy in temperature measurement in most of the other implanters.**

***Index Terms*—GaAs-on-insulator, ion-cut, hydrogen implantation**

I. INTRODUCTION

Much scientific interest has been focused on the combination of III-V semiconductors with mature silicon technology for many years. Especially, monolithic integration of GaAs into silicon technology presents a huge potential of interest as it combines the superior electrical and optical properties of GaAs with the mechanical and economical advantages, and density of integration of silicon. To obtain this structure, heteroepitaxial growth has been investigated extensively, but due to the notable lattice mismatch of about 4%, an unacceptable high density (typically > $10^7/cm^2$) of threading dislocations could not be avoided [1, 2].

From technical and economical points of view, one of the most promising techniques for joining thin GaAs single crystal layer with various substrates is an ion-cut technology proposed by Bruel in 1995 [3,4] in the name of 'smart-cut' as a method for the fabrication of high-quality silicon-on-insulator (SOI) wafers. SOI describes a sandwich structure in which a monocrystalline silicon layer (device layer) is electrically isolated from the silicon substrate by an oxide layer. SOI benefits include high speed, low power consumption, low leakage current, the ability to withstand higher temperatures and radiation fields, and the integration of electrical and optical signals. So, SOI encompasses a wide array of applications, including MEMS, smart power, solar cells, and high-speed microprocessors and memories [5, 6].

The ion-cut technology consists in hydrogen ion implantation into the semiconductor wafer, bonding implanted wafer with an unimplanted one, and final exfoliation by thermal treatment leading to the transfer of the surface layer of hydrogen-implanted wafer. However, layer splitting can be achieved only if appropriate implantation conditions (fluence, flux and actual implantation temperature due to beam heating), specific to each material, are employed. As opposed to Si, the

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optimum implantation temperature range for GaAs (160~250°C) is known to be rather narrow, and such condition is somewhat difficult to control when standard ion implanters are used [7,8]. Several attempts to transfer GaAs layers onto Si by layer splitting have been reported [9-11]. However, until now, there is no consensus as to the implantation temperatures required to split GaAs [12] most probably due to the inaccuracy in the measurement of wafer surface temperature.

Recently, Radu et al. proposed He+H co-implantation technique which enables room temperature implantation, and in addition, the minimum fluence necessary to induce blistering and exfoliation of silicon can be decreased by a factor of 2~3 by this technique [13]. Originally, it was proposed as a low-temperature (<250°C) splitting and layer transfer of GaAs. When dissimilar materials are used, it is desirable that the splitting temperature is low enough to allow bonded wafer pairs to withstand stresses associated with a difference in thermal expansion coefficients.

We have tried to develop ion-cut process to allow a large dimension GaAs thin film to be transferred onto a full silicon wafer as shown in Fig. 1, based on the already developed ion-cut technology for the formation of SOI wafers with various SOI thicknesses [14]. The aim of this paper is to investigate the role of implantation temperature and ion fluence on blistering of the surface after a subsequent annealing, which is a prerequisite of ion-cut splitting, in detail and to further investigate hydrogen implantation mechanism.

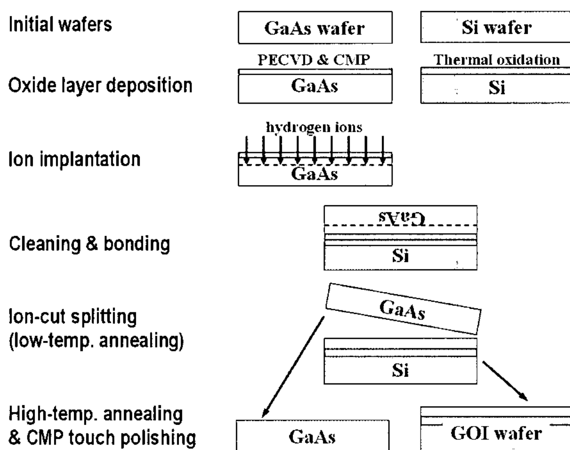


Fig. 1. Schematic of the ion-cut process for GaAs-on-insulator wafers formation.

II. EXPERIMENTS

In order to determine the optimum conditions (implantation temperature and fluence, and annealing parameters) for the layer transfer of GaAs thin film, hydrogen ions were implanted into semi-insulating (100) oriented, 2" GaAs wafers at the temperature ranging from 40°C to 300°C. ion implantation has been performed by using a low energy ion implantation system at KIGAM as shown in Fig. 2. The actual surface temperature of the implanted wafer was directly measured to increase the accuracy in temperature measurement during implantation. Implantation energy of hydrogen ions was 40 keV, and fluences were varied from $4x10^{16}$ H^+/cm^2 to $2x10^{17}$ H^+/cm^2. To minimize channeling effects, implantation was performed under 7° sample tilt. In order to ignore the dependence of hydrogen flux on the ion-cut process [12], it was kept almost constant at about $1x10^{13}$ $H^+/cm^2/s$.

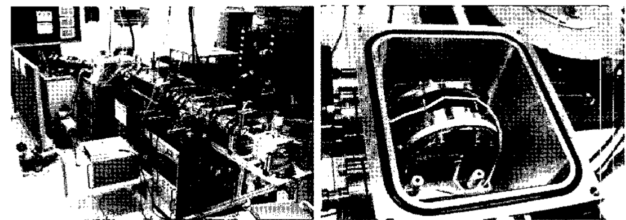


Fig. 2. Overview of the KIGAM low energy implantation system and inside view of the target chamber.

The implantation profile of hydrogen ions in GaAs was simulated by SRIM2003 (The Stopping and Range

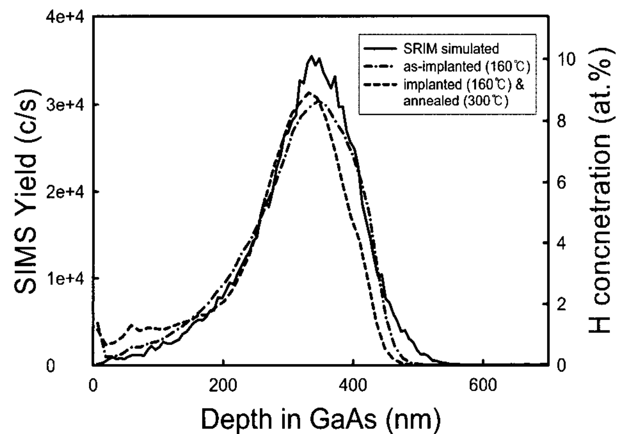


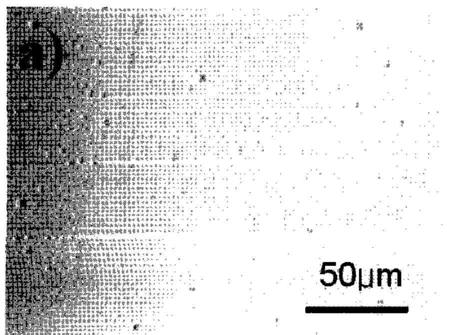
Fig. 3. Hydrogen concentration profiles in GaAs implanted with $8x10^{16}$ H^+/cm^2 at 160°C and annealed at 300°C as determined by the SIMS analysis.

of ions in Matter) code. A normal hydrogen depth distribution with a single peak at 320 nm depth corresponding to the projection range of 40 keV hydrogen ion beam was confirmed by secondary ion mass spectrometry (SIMS) measurements as shown in Fig. 3, and the profile of hydrogen atoms didn't alter remarkably either upon hot implantation and or upon annealing. It means that only short-range rearrangement of hydrogen atoms in the matrix can occur at the temperature less than 350°C [15].

Surface morphology after hydrogen bombardment and thermal treatment finally leading to the surface layer exfoliation was studied by means of optical microscopy and field emission scanning electron microscopy (FE-SEM). Structural defect formations were studied by means of Rutherford backscattering spectrometry (RBS)/channeling, and formation of platelets in the as-implanted GaAs and their evolution with annealing were analyzed by cross section transmission electron microscopy (XTEM).

III. Results And Discussion

Blistering is directly representative of the formation of hydrogen-induced microcracks, a condition required to obtain layer splitting, and blistering in GaAs is strongly dependent on both the substrate temperature and implantation fluence. For limited implantation fluences, no morphological change effect is observed on the surface of as-implanted wafers, and a bonding step with other wafer is possible. In the samples implanted at an optimum temperature and fluence, the mean size of the microcavities increases during annealing at an elevated temperature (>200°C) inducing deformations of the surface as blistering and flaking as shown in Fig. 4.



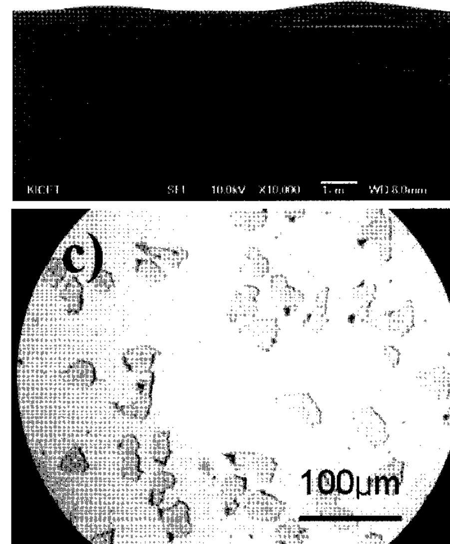


Fig. 4. Microscopic images on GaAs surfaces after implanttation (40 keV, $1.6x10^{17}$ H^{+}/cm^{2}) and annealing for 30 min at 300°C (a: optical, b: FE-SEM) and at 400°C (c: optical).

For the samples implanted at 120°C~160°C with a fluence in the range $1x10^{17}$ to $2.0x10^{17}/cm^{2}$, denoted with gray color in Fig. 5, the surface blistering phenomenon was observed after annealing at 200~300°C for about 30 min. The surface blisters have about 2~3 µm lateral size as shown in Fig. 4(a), and the areal density of generated blisters (~10^{6} blisters/cm^{2}) is found to be sufficient for ion-cut splitting. The minimum implantation temperature for obtaining blisters is a direct function of the hydrogen implanted fluence.

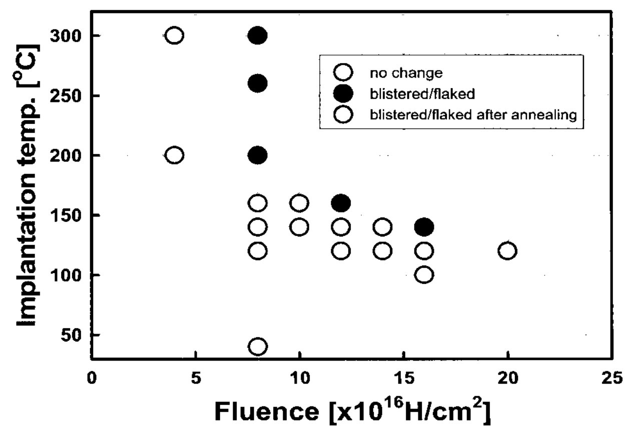


Fig. 5. Fluence and temperature boundaries of blister formation in hydrogen-implanted GaAs.

Actually the optimum temperature window for GaAs ion-cut process is not yet clearly known probably because the actual temperature on a wafer surface in implantation is not directly measured for most of the implanters. Tong et al. [7] reported that the appropriate window for the implantation temperature for GaAs ion-cut process is 160~250°C. However, this range is markedly different from our new result which indicate that the temperature window should be in the range between 120°C and 160°C for fluences ranging from 1.0 to $2.0x10^{17}$ H^+/cm^2.

As shown in Fig. 6, it is clear from the RBS/ channeling measurement that the lattice disorder substantially increases with increasing temperature due to rearrangement of hydrogen into the microcavities that are known to be responsible for blistering. The common crystal damage curing effect at elevated temperatures doesn't appear in this case against expectation. It is worth to point out that at this temperature only defects in the Ga sublattice are mobile, as defect mobility threshold for As sublattice lies above 300°C [11]. If the implant temperature is too low, the hydrogen does not appear to be mobile enough in the lattice to rearrange into the micro-defect structures. This is in agreement with the observation that no detectable surface deformation were observed after low temperature hydrogen implantation up to the fluence of $2.0x10^{17}/cm^2$. At temperatures above 200°C, RBS/channeling data has not been measured because blistering begins to appear at the high temperature. However, it is reported that at the high temperature the lattice disorder is lower, suggesting that the evolution of these defects is less prolific because of a

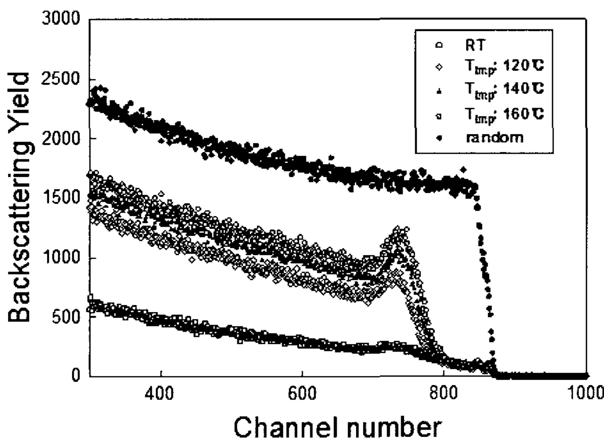


Fig. 6. Random and aligned RBS spectra for GaAs single crystals implanted with $8x10^{16}$ H^+/cm^2 at different temperatures.

pronounced out-diffusion of hydrogen [12]. These phenomena are responsible for the existence of a implantation temperature window for the layer splitting of GaAs wafer by an ion-cut process.

Fig. 7(a) shows a XTEM image of the damaged layer in a GaAs wafer implanted at a fluence of $1.2x10^{17}$ H^+/cm^2 at 140°C. It revealed that the microcavities are preferentially oriented along {111} and {100} planes and are localized at a depth of 320 nm from the surface close to the maximum concentration of hydrogen implanted into GaAs at 40 keV calculated by SRIM2003. These microcracks are hydrogen-filled platelets responsible for blistering and/or exfoliation, and have a relatively large (100~300 nm) lateral size in comparison to those in case of silicon. Those microcavities are also found in Si, SiC and Ge, and these results show that hydrogen-related splitting mechanism in GaAs is similar to that observed in other semiconductors.

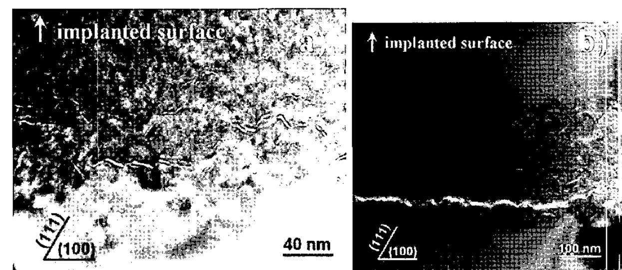


Fig. 7. Cross section TEM images of GaAs wafer after a) hydrogen ion implantation (40 keV, $1.2x10^{17}$ cm^{-2}) at 140°C and b) annealing at 300°C.

During annealing, hydrogen is released from the trapping sites and accumulates on the platelets formed during implantation. Due to an increase of the inner pressure, platelets grow and overlap, eventually leading to formation of large cracks following a zigzag path but parallel to the wafer surface on the whole as shown in Fig. 7(b). It is known that during thermal treatment a vertical rearrangement of the platelets occurs, following an Ostwald ripening mechanism, leading to formation of microcracks in a narrow layer, where cracking would occur.

When a handle wafer is bonded to the surface of implanted donor wafer as a stiffener, the blistering and/or flaking phenomena do not take place and a propagation of the cavities is observed. During annealing, gas-containing microcavities gradually grow and an interaction between neighboring microcavities results in

the propagation of a crack along the cavity plane and the complete separation parallel to the bonded surface. This experimental result is in agreement with theoretical consideration indicating that large area exfoliation and blistering are competing processes each other [16]. The originality of the ion-cut process is to use this pro pagation of cavities as a way to induce in-depth splitting over the whole wafer. Transferred film thickness can be correlated to projected range of implanted hydrogen ions, and as cavities are located in a layer with thickness corresponding to the simulated projected range straggling, a somewhat rough surface is obtained after splitting.

IV. CONCLUSIONS

Our results suggest that the ion-cut process for the GaAs layer transfer is sensitive to both the implant temperature and the hydrogen ion fluence. At implant temperatures below 100°C, hydrogen is unable to rearrange into the defect structure which is responsible for blistering, and if the implant temperature is too high, the platelets are not able to evolve and blistering is less prolific because of a pronounced out-diffusion of hydrogen atoms due to increased mobility. It was found that the optimum implant temperature window lie in 120~160°C for fluences ranging from 1.0 to 2.0×10^{17} H^+/cm^2, which is relatively lower than the previously reported implant temperature window probably due to the inaccuracy in temperature measurement in other laboratories.

Optimum post-implantation annealing temperature for the ion-cut layer splitting was found to be less than 250°C, and the low temperature splitting is of importance for layer transfer between dissimilar materials with very different thermal expansion coefficients as well as for processed wafers containing temperature-sensitive devices.

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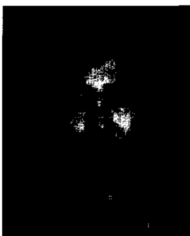

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