

DC Characteristics of P-Channel Metal-Oxide-Semiconductor Field Effect Transistors with $\text{Si}_{0.88}\text{Ge}_{0.12}(\text{C})$ Heterostructure Channel

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Abstract—Electrical properties of $\text{Si}_{0.88}\text{Ge}_{0.12}(\text{C})$ p-MOSFETs have been exploited in an effort to investigate $\text{Si}_{0.88}\text{Ge}_{0.12}(\text{C})$ channel structures designed especially to suppress diffusion of dopants during epitaxial growth and subsequent fabrication processes. The incorporation of 0.1 percent of carbon in $\text{Si}_{0.88}\text{Ge}_{0.12}$ channel layer could accommodate stress due to lattice mismatch and adjust bandgap energy slightly, but resulted in deteriorated current-voltage properties in a broad range of operation conditions with depressed gain, high subthreshold current level and many weak breakdown electric field in gate-oxide. $\text{Si}_{0.88}\text{Ge}_{0.12}(\text{C})$ channel structures with boron delta-doping represented increased conductance and feasible use of modulation doped device of $\text{Si}_{0.88}\text{Ge}_{0.12}(\text{C})$ heterostructures.

Index Terms—SiGeC Epitaxy, MOSFET, RPCVD, DC characteristics

I. INTRODUCTION

High level integration density, high speed operation, and low level energy consumption have been accomplished via primarily scaling technology based on the reduction of device dimensions, in accordance with specific ways of circuit design and software controlled optimization [1-4]. SiGe heterostructures, after valuable

success in high performance semiconductors by virtue of advanced BiCMOS technology, expand their applications to CMOS regime focusing on radio frequency integrated circuits as well as sub-100 nm processors [5-9]. Coming years will render interest even more in SiGe heterostructures to CMOS embedded SoC for subsequent evolution of mobile communications.

In SiGe heterostructures, using different energy bandgap of Si (1.12 eV) and Ge (0.66 eV), quantum well channels can be fabricated with two-to-eight folds high in carrier mobility compared to conventional silicon bulk channels. Moreover, many researchers reported SiGe devices could achieve much less noise level and expanded linearity in addition to fundamental merit of high speed operation. That is, high density integration and low cost for fabrication, and extremely stable reliability of electrical and thermal treatments provokes uncountable value of SiGe devices. Many previous works on SiGe MOSFETs suggested very promising advantages in terms of extreme enhancement in performance and 1/f noise level [10].

In case of admitting carbon in SiGe layer, the stress developed at the interface of SiGe and Si can be relaxed, and bandgap energy in SiGe(C)/Si heterostructures is to be precisely controlled by the amount of carbon incorporation. Since carbon is known to suppress the diffusion of boron in SiGe, a sharp delta doping of boron in SiGe channel may supply carriers and high performance devices [11, 12]. It is necessary to optimize epi structures for the development of new high performance SiGe MOSFETs [13]. Aggressive trial to adopt carbon in silicon-based devices must surpass technical barrier consisting of unknown problems with defects or segregation related interface states.

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In this study, we have exploited Si_{0.88}Ge_{0.12}(C) MOSFET with 0.1 % of carbon and boron delta doping underneath Si_{0.88}Ge_{0.12}(C) channel as a first step to expand horizon of silicon-based heterostructure devices targeting high performance and progressive approach toward nano-scale generation. As observed from the first trial to employ carbon and boron doping in SiGe heterostructures, possible considerations and difficult issues regarding fabrication process could have been understood in the practical aspect.

II. EXPERIMENTS

In this experiments, Si_{0.88}Ge_{0.12}(C) p-MOSFET with 0.6 μm gate has been fabricated in a conventional CMOS process. Device isolation was formed by LOCOS and Si/Si_{0.88}Ge_{0.12}(C)/Si quantum-well channels were grown on Si(100) substrate using RPCVD (Reduced Pressure Chemical Vapor Deposition) using SiH₄, GeH₄, SiH₃CH₃ as Si, Ge, and C source gases. The wafers were chemically ex situ cleaned and inserted into the N₂

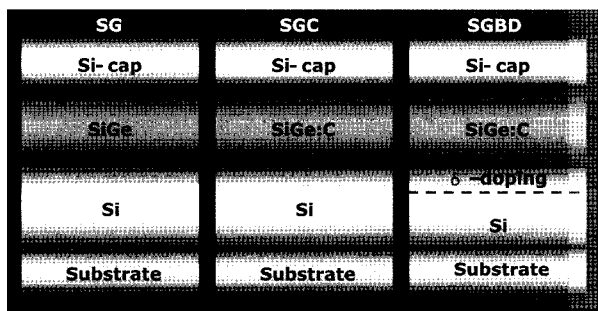


Fig. 1. Epitaxial structures of samples of SG (SiGe), SGC (SiGe:C) and SGBD (SiGe:C with δ-doping).

Table 1. Typical process conditions for device fabrication.

Process	Process Condition
N-well	P, 2.2x10 ¹³ cm ⁻² @120keV, 1150°C, 8 hr anneal
LOCOS	5500 Å
Gate Oxide	70 Å
Gate Poly	In-situ P-doped Poly-Si (IDP), 3000 Å
LDD	BF ₂ , 2.0x10 ¹³ cm ⁻² @65keV
Sidewall spacer	1000 Å
p+ S/D	BF ₂ , 3.0x10 ¹⁵ /cm ² @60keV, RTA @800°C, 30"
Polycide	TiSi ₂ salicide on the gate, source and drain
Dielectric	UDO and BPSG, 7500 Å
Metallization	Al-1%Si

Table 2. Summary of DC properties (L_g=0.6μm W_g=25μm).

	V _{th} (V)	SS (mV/dec.)	I _{off} (A)	G _{m,max} (mS)	
				L(@ V _{DS} =0.1V)	S(@ V _{DS} =3V)
SG	-1.1	80	2.1x10 ⁻⁹	0.26	2.28
SGC	-1.8	125	6.4x10 ⁻⁷	0.11	1.66
SGBD	-1.5	165	1.3x10 ⁻⁷	0.14	1.81

purged CVD load-lock chamber. Right after placed on the substrate susceptor, an in situ cleaning was performed by baking the substrate at 100 °C for 1 to 5 min in hydrogen environment. SiGe(C) layers were grown with three typical structures described in the Table 1 at 650 °C and 30 torr.

Major process steps are summarized in the Table 2. For pMOS device, after forming n-well, Si/Si_{0.88}Ge_{0.12}(C) channel epi layer was grown. The thickness of gate oxide was 7 nm, where the in-situ doped poly silicon holds heavy amount of phosphorous above 2x10²⁰ cm⁻³ in concentration. Source-drain area implanted with BF₂ was annealed at 800 °C using a rapid thermal anneal (RTA) system in nitrogen gas environment. Self-aligned Ti/TiN was deposited to the thickness of 30/30 nm for each layers and silicidation of low sheet resistance of 3-5 ohm/sqr. could be performed via sequential process of annealing and etching in NH₄OH chemicals. The Fig. 2(a) shows SEM photograph of a SiGe device taken after the metal layer defined, where the body contact could be identified along with other contact pads for source, drain and gate current flow schematic in Fig. 2(a) is discussed below.

Using secondary ion mass spectroscopy (SIMS) the atomic profile was analyzed in various epi structures of Si_{0.88}Ge_{0.12}, Si_{0.88}Ge_{0.12}(C), and delta-doped Si_{0.88}Ge_{0.12}(C). The electrical properties including I-V and C-V were measured using a parameter analyzer of HP4155 assembled with a probe station of Cascade's SUMMIT11741B-6.

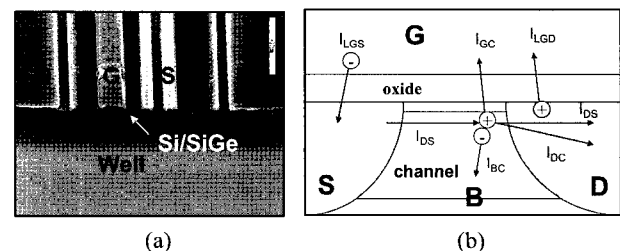


Fig. 2. (a) SEM pictures taken from SiGe:C p-MOSFETs, and (b) schematic view of current flow under MOS gate, where G, S, D, and B denote gate, source, drain and drain contacts.

III. RESULTS AND DISCUSSION

Fig. 3 shows depth profile of Ge, C, B atoms measured from the surface of samples of (a) SG, (b) SGC and (c) SGBD. Fig. 3(a) shows depth profile of Ge and detection limit of carbon concentration of SIMS system that we used for analysis. Figs. 3(b) and 3(c) represent quite normal distribution of Si, Ge, C concentrations as designed structure, but the boron profile reveals significant broadening. In fact, much of the broadening corresponds to artifacts of SIMS measurement with no additional calibration works.

It is necessary to note the sharp profile toward upside for boron concentration inside $\text{Si}_{0.88}\text{Ge}_{0.12}(\text{C})$ epi layer. Thermal process could have caused the dispersion of boron atoms in large part, and this problem needs further controlled thermal management in the future. In order to obtain more sharp delta-doped profile, dispersion phenomena will be prohibited through additional experiments to lower substrate temperature during epitaxial growth as well as subsequent process steps.

To evaluate gate oxides grown on Si/SiGe heterostructure, we have measured capacitance (C-V) and current flow as a function of gate voltage as shown in Figs. 4 and 5. Capacitance-voltage curve of MOS gate was measured at the frequency of 10 kHz with $10\ \mu\text{m} \times 25\ \mu\text{m}$ gate-oxide MOS structure. The capacitance characteristics changing from accumulation to inversion implies that the SiGe MOS structure formed well for device applications. In Fig. 5, when bias is applied

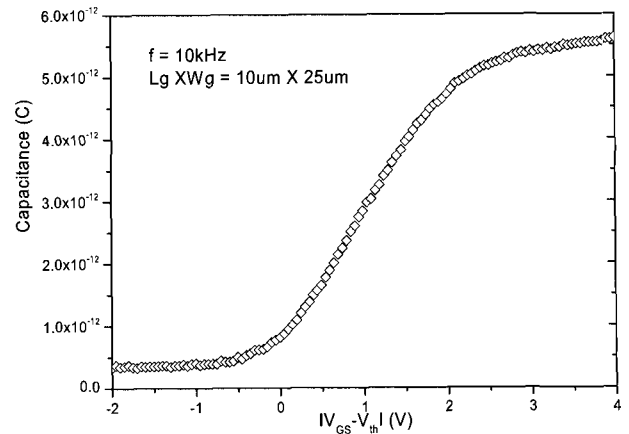


Fig. 4. Capacitance-voltage curve of MOS gate measured at the frequency of 10 kHz ($10\ \mu\text{m} \times 25\ \mu\text{m}$).

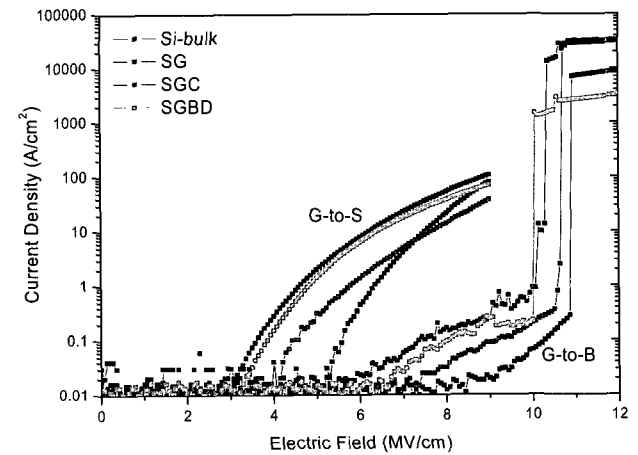


Fig. 5. Current-voltage curves of gate-to-source&drain (G-S) and gate-to-body (G-B) from the samples with gate dioxide of 7 nm grown on SG, SGC, and SGBD devices. The gate oxide on silicon bulk is inserted for comparison and oxidation was performed at $700\ ^\circ\text{C}$ in dry oxidation condition.

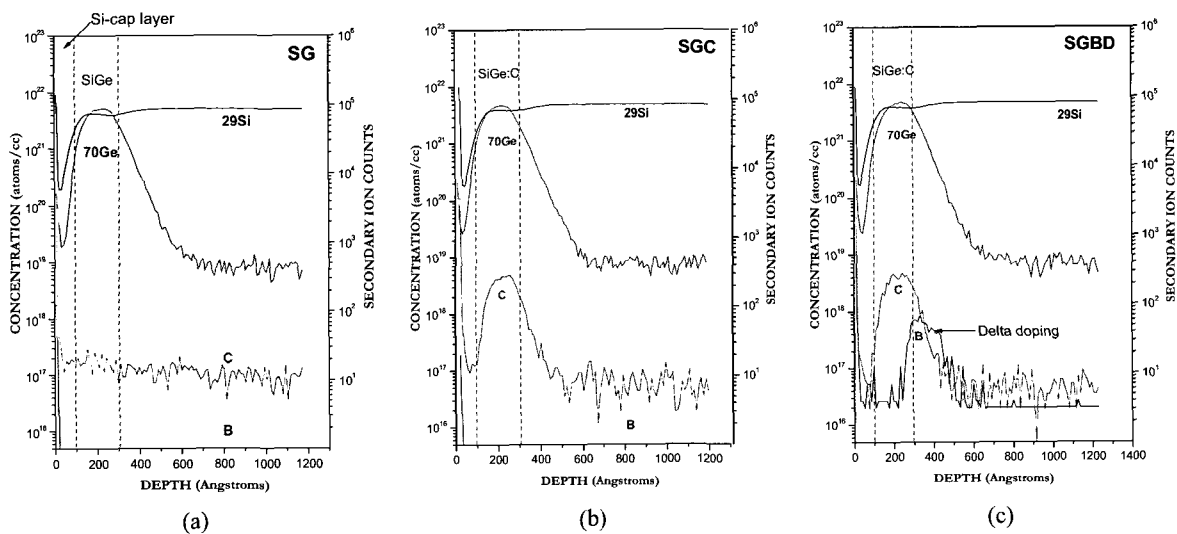


Fig. 3. SIMS depth profiles in SiGe channels structures measured from SG, SGC, and SGBD.

between gate and body contact, the electric field causing Fowler-Nordheim tunnel current begins at 6~8.5 MV/cm for SGBD, SGC, SG, and bulk-Si samples, and their corresponding breakdown fields are 10~10.9 MV/cm. When bias is applied between gate and source contact, the electric field causing tunnel current begins at 3~5.2 MV/cm for those and bulk-Si samples. The tunnel current of 7 nm SiO₂ on bulk-silicon implies that normal silicon dioxide films were grown, and their shifts in SiGe channel samples also exist in an appropriate regime.

Fig. 6 represents I_D vs. V_D curves measured while varying gate bias |V_{GS}-V_{TH}| from 0 V to 2 V with intervals of 500 mV. In SG sample, the maximum drain current of 3.4 mA was obtained at V_{DS}= 3 V and |V_{GS}-V_{TH}| = 2 V. As seen in transconductance, SGC resulted in the

smallest current level of 2.29 mA. On the contrary, SGBD sample shows 2.56 mA, which corresponds to 11 % increase in current level in comparison with SG sample. The degradation measured from SGC sample looks due to the presence of carbon atoms which would deteriorate gate-oxide interface or lower carrier transportation efficiency in channels correspondingly due to impurity scattering. According to current-voltage curves, the severe depression in the transconductance in the samples of SGC and SGBD were associated with the increased external resistance of source and drain. This degradation could be partially amended by the local-doping that supplies carriers in channel layers.

Figs. 7(a) and (b) represent transfer characteristics measured respectively in the linear (V_{DS}= -0.1 V) and saturation (V_{DS}= -3.0 V) regimes, and their corresponding electrical properties are summarized in Table 2. Subthreshold slope (SS) measured from samples of SG, SGC, SGBD represents progressive increase as given 80, 125, 165 mV/dec. in those samples. The maximum transconductance, G_{m,max}, was 0.23 mS in SG sample, which was higher than the other two samples. Meanwhile carbon doped SGC sample resulted in the lowest value of 0.17 mS. Small increase in transconductance of SGBD sample as given 0.18 mS compared to that of SGC. Nevertheless these imply that carbons not placed in appropriate sites of Si_{0.88}Ge_{0.12} channel might cause catastrophic degradation in several ways, as discussed below along with leakage, breakdown, and microscopic crystalline changes.

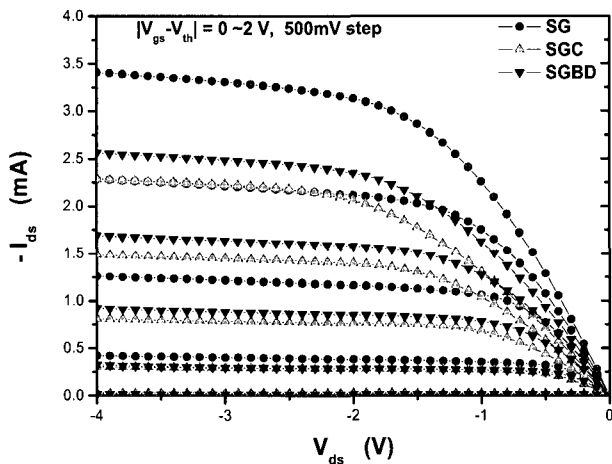


Fig. 6. I_{DS}-V_{DS} curves of SG, SGC, and SGBD devices.

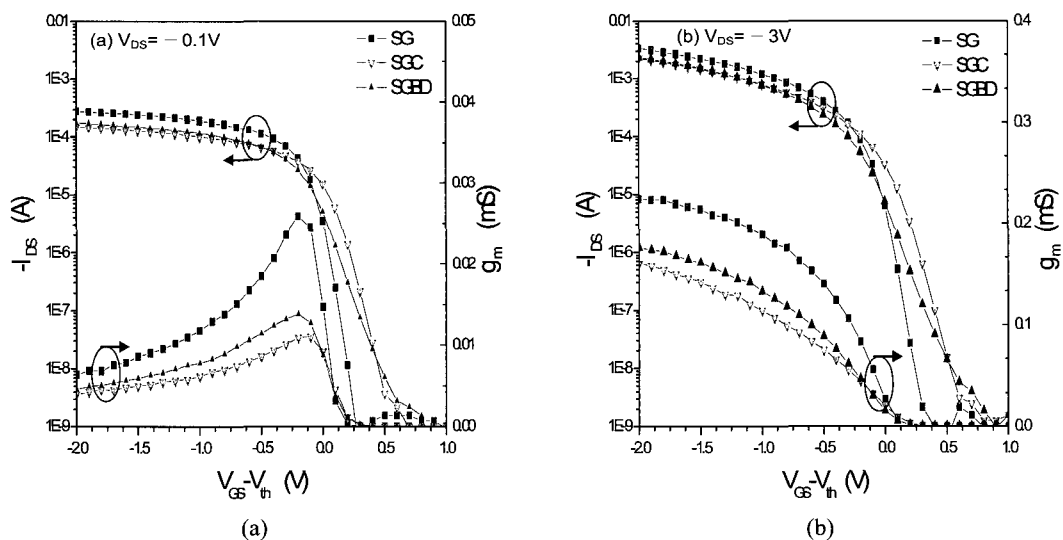


Fig. 7. Drain current and transconductance curves of SG, SGC and SGBD devices measured at (a) linear (V_{DS} = -0.1 V) and (b) saturation (V_{DS} = -3 V) conditions

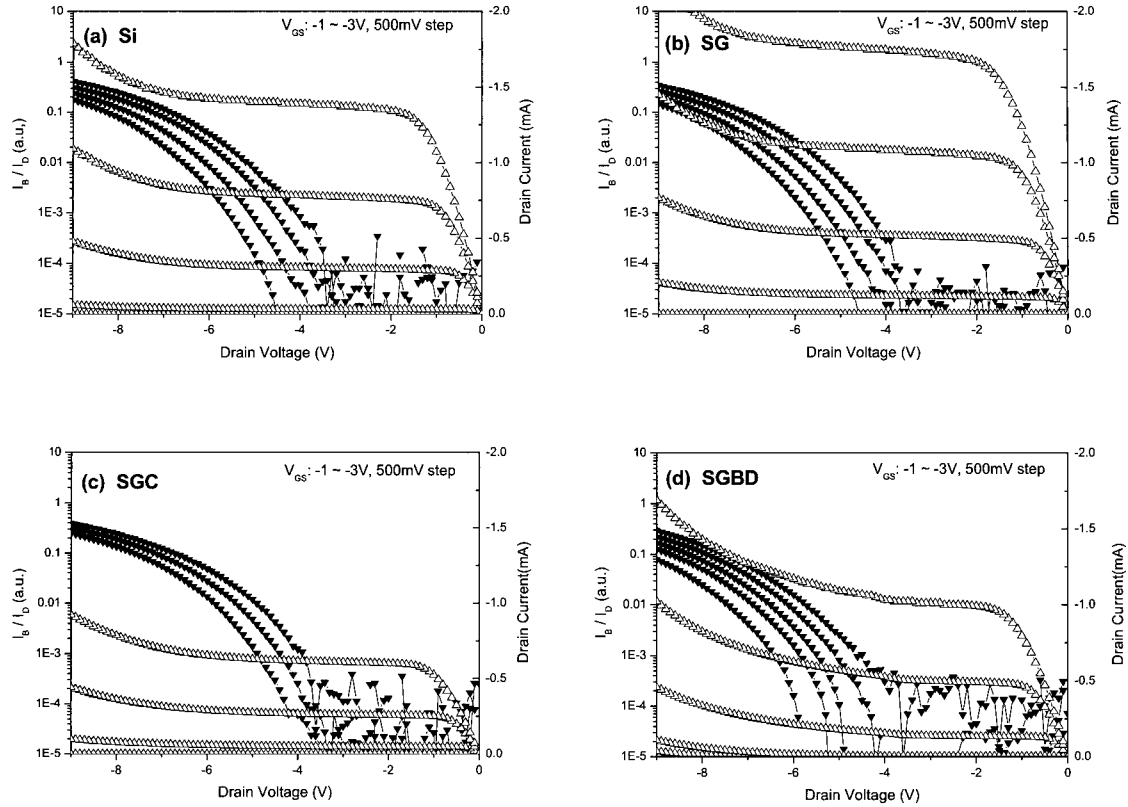


Fig. 8. Body current of (a) SG, (b) SGC, and (c) SGBD devices, measured in operation conditions of $V_{GS} = -1 \sim -3$ V with intervals of 500 mV, and the drain bias was scanned from 0 V to -9 V.

Meanwhile, the gate capacitance of MOS structure (C_G) measured as a function of gate voltage (V_{GS}) is expressed as $1/C_G(V_{GS}) = 1/C_{ox} + 1/C_D(V_{GS})$, where C_{ox} is the effective gate oxide capacitance, and C_D is assumed to be an ideal junction capacitance for simple calculation. Using this relationship and transconductance $g_m = dI_{DS}/dV_{GS}$, the drift mobility of carriers in Si/SiGe channel can be obtained as $\mu(V_{GS}) = \frac{g_m(V_{GS}) \cdot L_g}{C_D(V_{GS}) \cdot V_{DS}}$, where L_g and V_{DS} are the gate length and the drain voltage [14].

The depressed conductance in SGC and SGBD samples is likely due to carbon scattering impurities. although the highest carbon concentration is known to fully substitute lattice sites as high as ~ 1 at. % for the growth using CVD at 550 °C. We can adopt an appropriate expression between mobility and scattering centers, as found empirically found similarly scattering at interface states, $\mu/\mu_o = 1/(1+k \cdot N_s)$, where N_s (cm^{-3}) is the concentration of scattering centers, and k is a constant [15]. Additional precise work will be required to find k constant and the amount of scattering centers for various carbon embedded SiGe:C films.

Fig. 8 displays current-voltage curves of gate dioxide

grown on the samples of SG, SGC, and SGBD samples with 70 Å thickness, where gate oxide on silicon bulk is inserted for comparison and oxidation was performed at 700 °C in dry oxidation condition. Figure 8 shows body current for (a) SG, (b) SGC, and (c) SGBD samples, which were measured under various bias conditions: $V_{GS} = -1 \sim -3$ V with 500 mV step, and $V_{DS} = 0 \sim -9$ V. As the drain current increases, the body current becomes prominent through the impact ionization generating electron-hole-pairs (EHPs). The ratio of current, I_B/I_{DS} implies that the carriers in the channel of SGC sample generates large amount of electron-hole pairs (EHPs) through significant scattering of charged carriers. This degraded performance is believed primarily due to the presence of carbons placed improper positions in channel. The current flow of gate-to-body in Si and SG sample is observed almost same level, but substantial increase is recognized in both SGC and SGBD due to the carbon incorporation.

Fig. 9 shows gate current for the samples of (a) SG, (b) SGC, and (c) SGBD, which were measured in various bias operation conditions of $V_{GS} = -1 \sim -3$ V with 500mV step, and $V_{DS} = 0 \sim -9$ V. Unlike the body current,

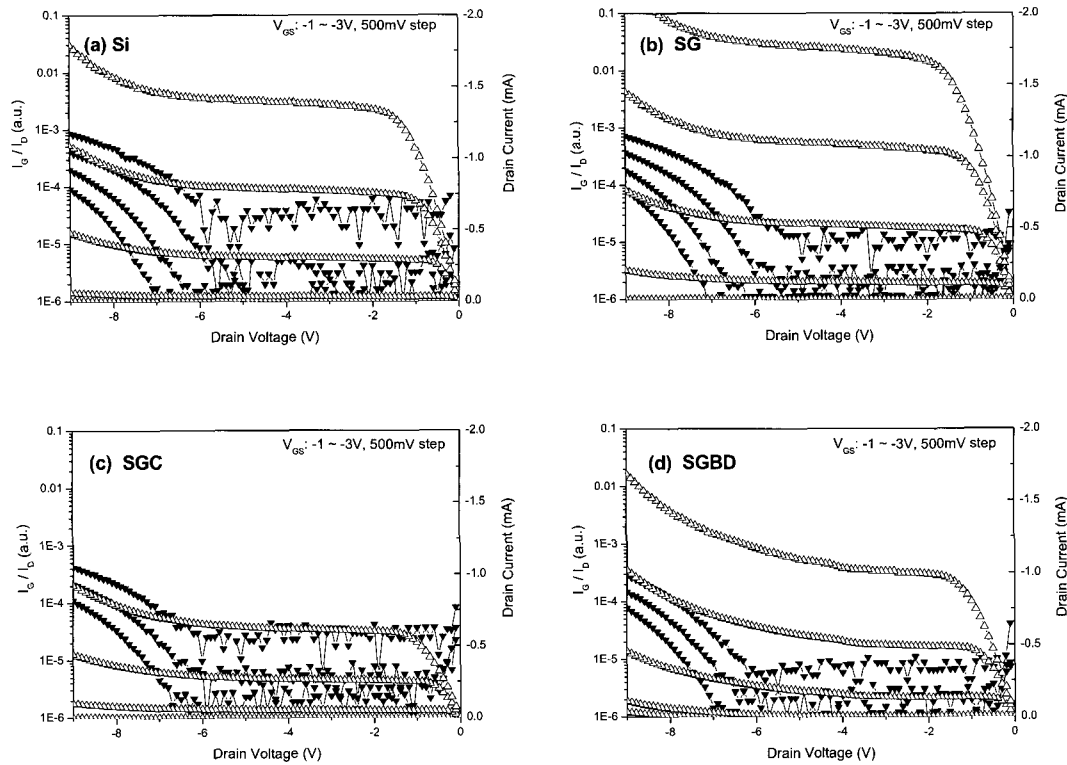


Fig. 9. Gate current of (a) SG, (b) SGC, and (c) SGBD devices, measured in operation conditions of $V_{GS} = -1 \sim -3$ V with intervals of 500mV, and the drain bias was scanned from 0 V to -9 V.

the gate leakage current looks more dependent on electrical properties of gate oxide than any contribution from EPHs generated in channels. Among gate leakage components as described in the Fig. 2(b), two possible contributions may come from electron tunneling: one is from gate to channel (I_{LGS}), and the other is the hole conduction from channel to gate I_{GC} and I_{LGD} . According to Fig. 7 and Fig. 8, and as notified in Fig. 5, most of excess carriers dissipate through body contact and the degree of current flow by excess carrier became dominant in carbon doped channel.

As discussed above, it is clear that the delta doping of boron could increase transconductance, however we also need to mention that carbon doping must be separated from carrier conduction and the spacer between channel and delta-doped layer should be adjusted properly. Also it is suggested that the delta-doping needs to be more sharp and narrow to reduce subthreshold current.

As explained above, three different shape of samples were fabricated to analyze the influence of carbon and boron playing a role of diffusion barrier and carrier supply in channels. Electrical properties obtained from SG presented the best properties with high transconductance

and straight forward device parameters. $Si_{0.88}Ge_{0.12}(C)$ layers were known to be stable for remarkably high annealing temperature due to the presence of carbon retarding phase transformation and stress compensation [16]. Therefore controlled process is necessary to utilize feasible merits of additional considerations using carbon and boron in $Si_{0.88}Ge_{0.12}$ channels. Carbon looks predominantly related to the depressed transport properties in $Si_{0.88}Ge_{0.12}$ channel and the increase in transconductance by boron were limited in this experiment.

From experimental results, it is concluded that $Si_{0.88}Ge_{0.12}(C)$ layer must be separated from channels being made of either silicon or SiGe is desirable, so a certain shape of silicon cap layer can be placed between channel and the delta-doped layer. In addition, it is likely that scales or three dimensional CMOS will try to adopt SiGe, SiGeC in dca-nao technology generations. Problems associated with auto-doping and out-diffusion, additional process steps are necessary during epitaxial growth and subsequent fabrication process.

IV. CONCLUSIONS

$\text{Si}_{0.88}\text{Ge}_{0.12}(\text{C})/\text{Si}$ heterostructure channels grown by RPCVD were employed to p-type MOSFETs, and their electrical properties were analyzed using I-V and C-V measurements. In a wide range of scope, samples with carbon and boron presented favorable breakdown voltage and leakage levels as compared to conventional Si device. The incorporation of carbon resulted in a shift of threshold voltage -0.7 V, and even significantly decreased transconductance. The delta doping of boron could have increased the transconductance by 11 % in the device using $\text{Si}_{0.88}\text{Ge}_{0.12}(\text{C})$ channel but not sufficient to recover up to that of $\text{Si}_{0.88}\text{Ge}_{0.12}$ channel device. It is suggested that low temperature epitaxial growth and subsequent thermal process need to eliminate unfavorable phenomena associated with dispersed profile of carbon and boron in channels.

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