Molecular Beam Epitaxy of InAs/AlSb HFET's on Si and GaAs Substrates

Jae-Eung Oh* and Mun Deok Kim**

***Abstract*—High electron mobility transistors with InAs channels and antimonide barriers were grown on Si and GaAs substrates by means of molecular beam epitaxy. While direct growth of Sb materials on Si substrate generates disordered and coalescences 3-D growth, smooth and mirror-like 2D growth can be repeatedly obtained by inserting AlSb QD layers between them. Room-temperature electron mobilities of over 10,000 cm^2/V-s and 20,000 cm^2/v-s can be routinely obtained on Si and GaAs substrates, respectively, after optimizing the buffer structure as well as maintaining InSb-like interface.**

***Index Terms*—InAs/AlSb HFET, Molecular Beam Epitaxy, Nano-CMOS, Quantum Dot**

I. INTRODUCTION

With Si MOSFET scaling down to its fundamental physical limit, new materials and structures must be developed in order to keep the continuous improvement on device performance. The saturation drain current of MOSFET I_{DS} upon dimension shrinkage may limit the prospect of future scaling:

$$I_{DS} = W \times Q_{inv} \times v_{inj} \quad (1),$$

where Q_{inv} is the charge density of inversion layer and v_{inj} is a source injection velocity, which translates into higher drive current and smaller gate delay. To obtain high gate capacitance with lower gate leakage, many materials with high dielectric constant (κ) such as HfO_2 and ZrO_2 have been studied in Si MOS devices to replace SiO_2. As for channel material, several different materials including Ge and III-V compound semiconductors have been considered to replace Si for future high-speed CMOS technology due to their much higher carrier mobility than Si. Therefore, the most important innovation in the future device technology will be "Non-Si-OI (on Insulator) Channel CMOS".

Fig. 1 illustrates the schematic of "Non-Si-OI Channel CMOS", where p-MOS consists of GOI (Ge on Insulator) or SGSOI (SGS on Insulator) while n-MOS can be III-V-OI (III-V on Insulator) [1]. Due to its highest hole mobility and higher electron mobility, Ge is one of the most promising candidates as a channel material for "Non-Si-OI Channel CMOS". On the other hand, III-V materials such as InGaAs, InAs, and InSb look promising due to their extremely high electron mobility as well as high saturation velocity. A few groups began to explore new channel FETs over a decade ago. To date, most research has focused on demonstrating the feasibility as well as on solving the fundamental problem existing in the complicated material system, especially hetero-epitaxial growth on Si substrate as a final destination [2, 3].

In this work, we have explored the hetero-epitaxial growth of InAs/AlSb HFETs on both GaAs and Si substrates by optimizing the initial stage of hetero-epitaxy. Advantages of this material system include the high electron mobility (>20,000 cm^2/V-s at 300K) and velocity (4x10^7 cm/sec) of InAs, and a large conduction band offset between InAs and AlSb (1.35 eV), offering a great possibility as a new n-channel material in the concept of "Non-Si-OI Channel

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CMOS". Due to large lattice mismatch with GaAs and Si (7% and 12%, respectively) and its polar nature compared to non-polar Si, however, high density threading dislocation over 10^7 cm^{-2} through the active device region and complicated defect network prohibits it from further evolving to the digital application.

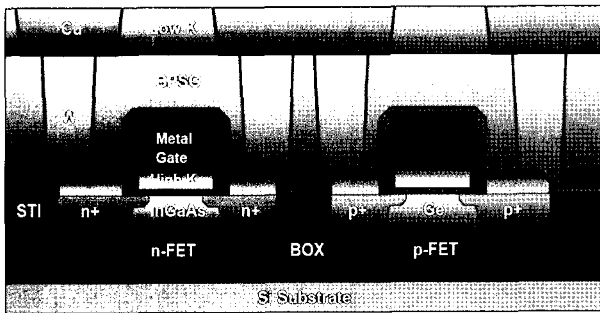

Fig. 1. Schematic of "Non-Si-OI Channel CMOS" proposed by Ref. 1.

II. EXPERIMENTAL TECHNIQUES

Samples were grown by solid-state molecular beam epitaxy (MBE) on Riber-32P system. The native oxide of GaAs is removed by heating the sample to 600°C under an As_4 flux. A 200 nm thick buffer layer of GaAs is then grown at 580°C prior to proceed to the InAs/AlSb system growth. Piranha solution, consisting of four parts of H_2SO_4 (2M) per one part of H_2O_2 (30 wt.%) by volume, used to remove carbon contamination and to chemically oxidize the exposed Si, after the usual HF treatment. In-situ thermal processing until a clear (2x1) superstructure was observed by reflection high-energy electron diffraction (RHEED).

At relatively low temperature, a few mono-layer of Sb was deposited, followed by the formation of AlSb quantum dots on both substrates, which intends to, in a controlled manner, transfer to the lattice constant from the hosting material to that of the active material in the initial stage of growth. Some samples were grown without AlSb QD layer for the comparison purpose. The substrate temperature was set to 500°C to grown 0.5 m thick GaSb and subsequent 1.5 m thick AlSb buffer layers. Then, additional 20 period of AlSb and GaSb superlattice was grown to block the remaining threading dislocations. The Sb-soaking while lowering the substrate temperature to 460°C was used to form InSb-like interface, followed by the growth of 15 nm thick InAs channel layer. The channel was followed by a 10 nm AlSb barrier, a 10 nm $Al_{0.8}Ga_{0.2}Sb$ layer, and a 5 nm InAs capping layer. Transmission electron microscopy (TEM) micrographs and selected area electron diffraction (SAED) patterns for the study of a growth mode and structural properties were taken with a JEOL-2000EX and JEOL-3010. Standard Hall/van der Pauw measurements were performed at 0.37 T on 5x5 mm^2 squares, usually taken from the center of the wafer. Low-temperature photoluminescence at 10K and high-resolution x-ray diffraction measurements were performed to characterize the grown materials.

III. RESULTS AND DISCUSSION

Fig. 2 shows the HRTEM micrograph of the GaSb directly grown on Si substrate, which is the three-dimensional (3D) GaSb islands and their coalescences with the height of approximately 250 nm, with the relative orientation of GaSb <110> // Si <110> and GaSb {111} // Si {220}. Fig. 2 (b) and 2 (c) are the fast Fourier transformation (FFT) and the inverse-fast Fourier transformation (IFFT) results carried out for an extended structural study. The zone axis is indexed as $[1\bar{1}0]$ and the GaSb (111) plane is parallel to the Si (220) plane in both the FFT image and Fig. 2 (b). In this case, the misfit δ between the GaSb layer and Si substrate is defined by

$$\delta = (2 \times d_{Si220} - d_{GaSb111}) / d_{GaSb111} = 0.091$$

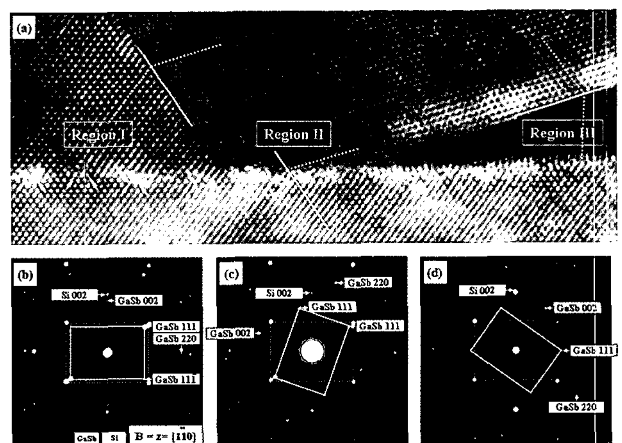

Fig. 2. HRTEM micrograph and FFT structural analysis of GaSb directly grown on Si substrate, showing three regions with different crytal structure.

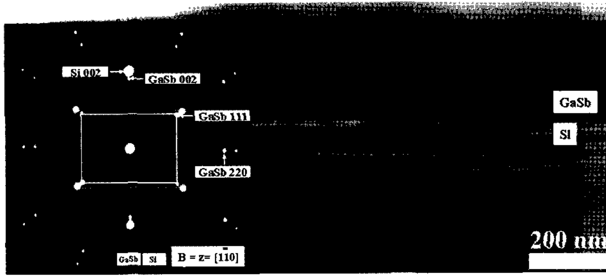

Fig. 3. FFT crystal analysis and cross sectional TEM of GaSb grown on Si substrate with AlSb QD insertion.

this value is quite s maller than the misfit δ′ of the system with the relative orientation of GaSb <110> // Si <110> and GaSb {002} // Si {002} (δ′ = ~ 0.122). If extra half planes are introduced into the structure for strain relaxation, the average spacing S of misfit dislocations depends on the misfit δ and is of the order of $(2 \times d_{Si220})/\delta$. Therefore the S is determined in Fig. 3 (c) following as:

$$= (2 \times 1.92) / 0.091 = 42.2 \text{ Å}$$

because the inter-planar spacings of (220) planes of the Si substrate and that of (111) planes of the GaSb are about 1.92 Å and 3.52 Å, the (220) plane of Si and the (111) plane of the GaSb have to be accordant with each other every about twelve planes for GaSb and twenty-two planes for Si, respectively.

From the above results, the crystallographic orientation relation was changed through twin boundaries with (111) plane as mirror plane to reduce the lattice misfit between GaSb and Si substrate when the GaSb was directly grown on Si substrate.

It is found that the AlSb QD buffer layer plays a critical role for improving the crystallinity of GaSb layer in the growth process of GaSb on Si substrate. Fig. 3 shows the cross-sectional TEM micrograph and SAED pattern for the GaSb grown on the AlSb QD buffer layers deposited after antimony (Sb) soaking. The introduction of the AlSb QD buffer layer clearly improved the quality of the GaSb crystals. The GaSb layer has a very flat surfaces and interface. The dislocations are mostly generated near the interface between GaSb layer and Si substrate and the dislocation density decreases with the increase of the thickness of GaSb layer. The SAED pattern shows the relative orientation of the GaSb <110> // Si <110> and GaSb {002} // Si {002}. Fig. 5 is the HRTEM micrographs taken from the GaSb layer grown on the AlSb QD buffer layer. Just eight 90° misfit dislocations are shown in Fig. 5. The driving force for the generation of 90° dislocations is the lattice mismatch between GaSb layer and Si substrate. 90° dislocations are the most efficient misfit dislocations for strain relaxation because the length of the Burgers vector edge component projected into the interface b_e is $a/\sqrt{2}$ (The Burgers vector b_{90° of 90° dislocations is 1/2a $[\bar{1}\bar{1}0]$). The theoretical average spacing S of 90° misfit dislocations is 49.8 Å because the misfit δ is about 0.123. However, the 90° misfit dislocations are actually arranged with a periodicity between 3.07 nm to 3.84 nm along the [110] direction in Fig. 4, and there eventually are more 90° dislocations than the theoretical value on the interface between the GaSb layer and Si substrate.

Fig. 5 shows the series of RHEED patterns during the formation of AlSb QD, GaSb buffer, and subsequent AlSb buffer layers. Spotty RHEED pattern of AlSb QD is immediately transferred to the streaky pattern of GaSb layer, implying that 2D layer-by-layer growth is actually occurred in the early stage of GaSb growth. This is

Fig. 4. HRTEM of AlSb inserted between Si substrate and GaSb layer, clearly showing a lattice constant transition.

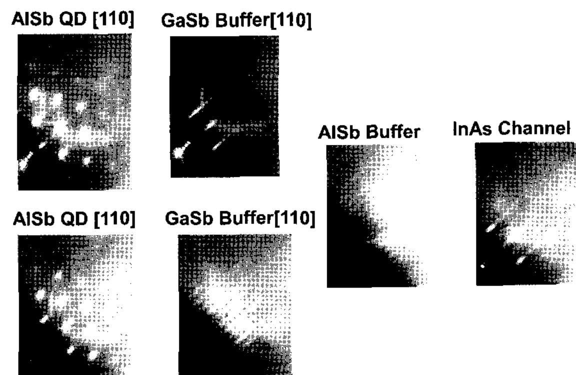

Fig. 5. RHEED pattern taken during the growth of AlSb QD, GaSb buffer, AlSb buffer, and InAs channel. Streaky pattern of GaSb reveals the 2D growth occurring during the buffer growth.

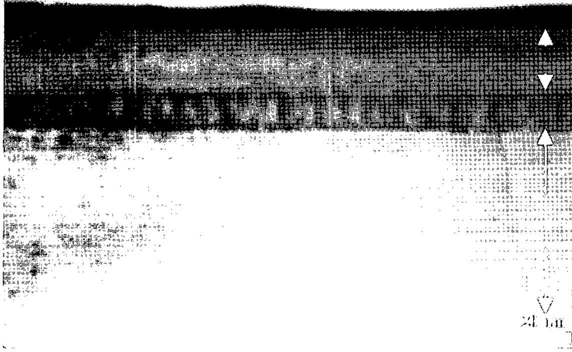

Fig. 6. Cross sectional view of InAs/AlSb HFET grown on Si substrate.

contradicted to the 3D growth of GaSb layer directly grown on Si substrates, as shown in Fig. 2 (a). Streaky and bright RHEED pattern is kept during the growth of AlSb buffer layer as well as underneath GaSb buffer layer. The surface roughness of the buffer layer consisting of AlSb, GaSb, and AlSb QD on Si substrate, measured by AFM, is below 1 nm, confirming the very smooth surface obtained by this growth technique.

Fig. 6 shows the cross sectional TEM picture of the active region of AlSb/InAs HFET grown on Si substrates. As shown in the picture, very abrupt interfaces of the channel as well as low threading dislocations demonstrates that the growth condition including the initial buffer formation is indeed quite well optimized. As reported in the previous works, the smoothness of the interface as well as InSb-like interface formation is a key growth parameter to determine the carrier transport properties.

IV. CONCLUSIONS

We have successfully demonstrated the hetero-epitaxial growth of InAs/AlSb HFET's on both Si and GaAs substrates. AlSb QD layer inserted between the substrate and GaSb buffer layer enhances the 2-D growth and subsequent good transport properties of InAs HFET. In addition to optimizing the buffer growth condition, InSb-like interface between InAs and AlSb plays an important role in the channel transport characteristics.

ACKNOWLEDGMENTS

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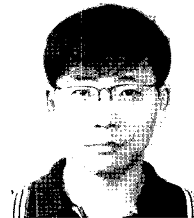

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