Beyond-CMOS: Impact of Side-Recess Spacing on the Logic Performance of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs

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Abstract—**We have been investigating InGaAs HEMTs as a future high-speed and low-power logic technology for beyond CMOS applications. In this work, we have experimentally studied the role of the side-recess spacing (L_{side}) on the logic performance of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs. We have found that L_{side} has a large influence on the electrostatic integrity (or short channel effects), gate leakage current, gate-drain capacitance, and source and drain resistance of the device. For our device design, an optimum value of L_{side} of 150 nm is found. 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs with this value of L_{side} exhibit I_{ON}/I_{OFF} ratios in excess of 10^4, subthreshold slopes smaller than 90 mV/dec, and logic gate delays of about 1.3 ps at a V_{CC} of 0.5 V. In spite of the fact that these devices are not optimized for logic, these values are comparable to state-of-the-art MOSFETs with similar gate lengths. Our work confirms that in the landscape of alternatives for beyond CMOS technologies, InAs-rich InGaAs FETs hold considerable promise.**

Index Terms—**HEMT, $In_{0.7}Ga_{0.3}As$, side-recess spacing, subthreshold-slope, DIBL, I_{ON}/I_{OFF}, gate delay.**

I. INTRODUCTION

For the last 30 years, Moore's law has been a guiding principle for the semiconductor industry [1]. Sustaining Moore's law requires a continuous scaling of Si MOSFETs. The physical gate length of Si-transistors that are utilized in the current 65 nm technology-node is about 30 nm [2]. It is expected that this critical dimension will reach about 10 nm around 2011. While a matter of considerable debate, it is widely believed that this is the ultimate limit of CMOS-scaling [2]. With this prospect, identifying a new semiconductor logic device technology that can sustain Moore's law is becoming increasingly urgent. Candidates, which have been often mentioned, are Carbon-nanotube transistors, semiconductor nano-wires and, further out, spintronics [3-5]. However, at this time, many of these device concepts are hardly beyond the prototyping stage.

In contrast with these alternatives, III-V HFETs and, in particular, InAlAs/InGaAs High-Electron-Mobility-Transistors (HEMTs), constitute a very "real" device technology. For most of the last nearly 20 years, it has demonstrated the best high frequency performance of any transistor technology as measured by cut-off frequency (f_T) [6]. The current record is 562 GHz [6]. Besides, InGaAs HEMT manufacturing technology is relatively mature. Until now, several ultra-high-speed integrated circuits (ICs) have already been successfully demonstrated, such as above 100 Gb/s opto-electronic ICs [7] and above 200 GHz MMICs [8]. Finally, this device technology is also space qualified [9].

These devices, however, suffer from poor electrostatic integrity and inadequate scaling behavior, and as a result are of questionable usefulness for logic. For example, in [10], the maximum transconductance ($G_{m,max}$) no longer improved below an L_g of about 80 nm. In fact, improvements in f_T with gate length scaling were shown to arise from a decrease of the gate capacitance alone. In order for InGaAs HEMT technology to play an important role in future logic systems, well behaved scaling has to be demonstrated down to about 20 nm gate lengths. Therefore, it is imperative to identify ways

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to improve the electrostatic integrity and the scaling behavior of sub-100 nm InGaAs HEMTs.

In optimizing InAlAs/InGaAs device performance for millimeter-wave and fiber optic applications, it has been reported that the side-recess spacing (L_{side}) plays a key role in balancing out short-channel effects and frequency response [11]. However, the impact of L_{side} on the logic characteristics of sub-100 nm InGaAs HEMTs has not been explored. In this paper, we have experimentally investigated the impact of L_{side} on the logic figures of merit of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs. We demonstrate that insufficient L_{side} seriously degrades the electrostatic integrity of the device and the logic figures of merit. Too long an L_{side} increases the source and drain access resistance, which also degrades logic characteristics. For our device design, an optimum L_{side} of around 150 nm results in I_{ON}/I_{OFF} ratio, subthreshold slope, DIBL and CV/I comparable to those of state-of-the-art Si MOSFETs. This paper presents an updated and expanded version of a recent conference presentation [12].

II. Process Technology

Fig. 1 shows a schematic diagram of the fabricated 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs. Device fabrication began with mesa isolation through wet chemical etching. Ni/Ge/Au was evaporated and lifted off to form the source and drain ohmic contacts. Source to drain spacing is 2 μm.

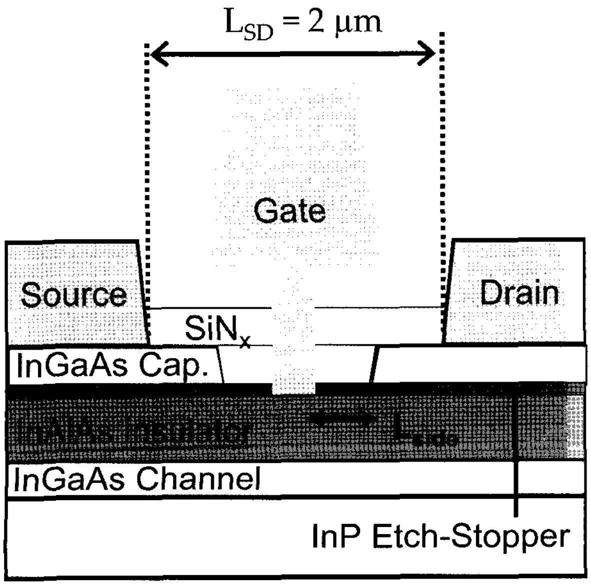

Fig. 1. Schematic of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs.

the contacts were alloyed at 320 °C in H_2 ambient. On top of a Remote-PECVD (R-PECVD) grown 60 nm SiN_x dielectric layer, a new Electron-Beam-Lithography (EBL) process was applied to fabricate 50 to 150 nm gate length T-shaped gates. A conventional T-gate process was inappropriate to fabricate 50 nm gates, because of the relatively large beam diameter (~ 50 nm) of the EBMF-10.5 e-beam machine that was available to us. In the devices studied here, a T-shaped Schottky gate with a Ti/Pt/Au metal stack was directly deposited onto the $In_{0.52}Al_{0.48}As$ insulator layer. For this purpose, the gate recess was carried out by means of a two-step recess technology [13]. The $In_{0.53}Ga_{0.47}As$ cap was etched using a mixture of citric acid ($C_6H_8O_7$) and H_2O_2 with volume ratio of 7 to 1. This has an etching selectivity of about 470 over the InP etch stop layer. Following this, the 6 nm InP etch stop layer was anisotropically etched by Ar-based RIE [13].

In [11], it was reported that the lateral extension of the gate recessing, called as side-recess spacing (L_{side}), has a significant impact on the device characteristics. Increasing L_{side} was found to enhance the cutoff frequency, and to minimize the output conductance and gate leakage current. In order to explore the impact of the side recess spacing on the logic figures of merit of our devices, in our experiment L_{side} was varied in different samples from 30 to 250 nm by changing the etching time of the InGaAs cap wet recess. After gate recess etching, L_{side} was measured by SEM, as shown in Fig. 2. Fig. 3 shows the dependency of L_{side} on the recess etching time. From these experiments, we extracted a lateral etch rate for the $In_{0.53}Ga_{0.47}As$ layer of about 127 nm/min, which is slightly slower than a vertical etch rate of about 140 nm/min.

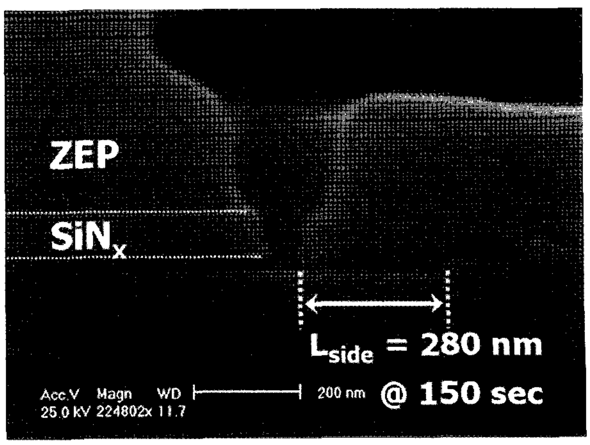

Fig. 2. SEM image of gate structure after recess etching.

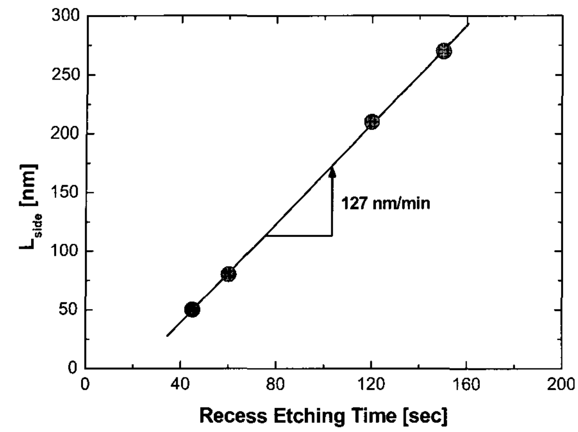

Fig. 3. Measured L_{side} as a function of recess etching time.

III. DC AND RF CHARACTERISTICS OF $In_{0.7}Ga_{0.3}As$ HEMTS

Fig. 4 shows the output characteristics of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs with four different side-recess spacings. The maximum drain current density decreases as L_{side} increases, due to the increase in a source and drain access resistance. The drop in current is the most prominent for the L_{side}=250 nm sample which is the longest. Fig. 5 shows the transconductance (G_M) characteristics for the same four devices at a drain bias of 0.5 V. As L_{side} increases, the threshold voltage (V_T) shifts positive, and the peak transconductance initially increases and then decreases.

Fig. 6 shows a semi-log plot of the drain and gate current characteristics as a function of V_{GS} for the same four devices, at a drain bias of 0.5 V. Increasing L_{side} leads to a remarkable improvement in the subthreshold characteristics. The device with L_{side} of 30 nm exhibits a poor subthreshold slope (S) of 178 mV/decade, while the device with L_{side} of 150 nm exhibits much better value of S of 86 mV/decade. S is extracted at a gate bias corresponding to I_D = 1 mA/mm. These improved subthreshold characteristics partially arise from a dramatic reduction in the gate leakage current (also shown in Fig. 6) and a mitigation of the short channel effects, consistent with [11]. The amelioration of the short channel effects also manifests itself in a positive shift in V_T as L_{side} increases.

An important Figure of merit for logic operation is the I_{ON}/I_{OFF} ratio. For non-optimized devices such as those discussed here, we have applied the methodology of [14] to extract this Figure of merit. Selecting a value of V_T that corresponds to a drain current of 1 mA/mm, the on-state current (I_{ON}) is defined as 2/3 V_{DS} swing above V_T, and the off-state current as 1/3 V_{DS} swing below V_T, as

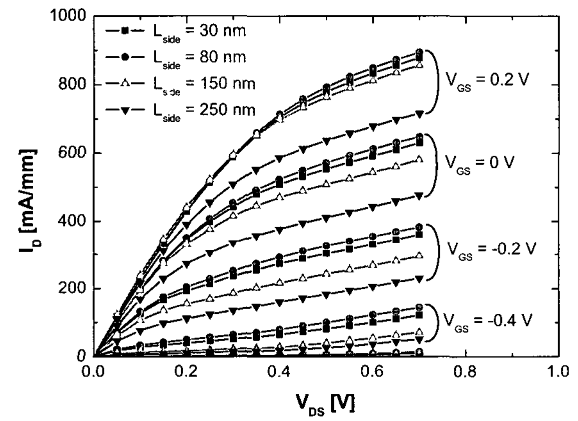

Fig. 4. Output characteristics of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs with different values of side recess spacing (L_{side}).

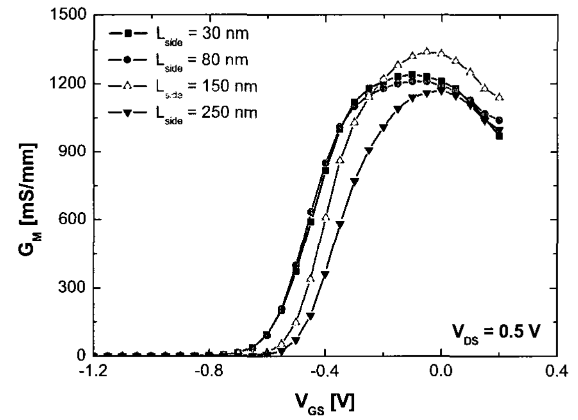

Fig. 5. Transconductance (G_m) characteristics of all 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs with four different values of L_{side} at V_{DS} = 0.5 V.

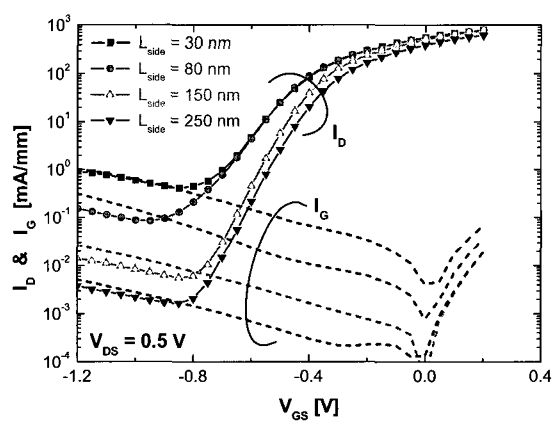

Fig. 6. Semi-log plot of I_D and I_G of all 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs with four different values of L_{side} at V_{DS} = 0.5 V.

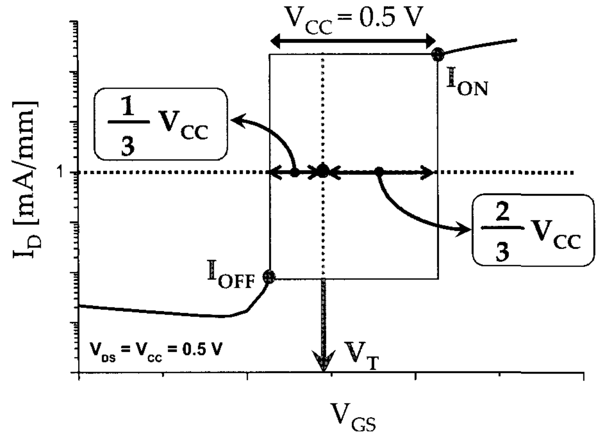

Fig. 7. Evaluation methodology for the logic performance analysis of our InGaAs HEMTs. V_T is defined at a drain current of 1 mA/mm when $V_{DS} = V_{CC}$.

Table 1. Extracted logic parameters of four 50 nm InGaAs HEMTs with different values of L_{side} at V_{DS} of 0.5 V. For reference, state-of-the-art results for 90 nm technology-node Si MOSFETs, which yield physical gate length of around 50 nm, are included at V_{DS} of 1.2 V [15].

L_{side} [nm]	$G_{M,max}$ [S /mm]	S [mV /dec]	DIBL [mV/V]	I_{ON}/I_{OFF}	CV/I [ps]	R_S+R_D [Ω-mm]	C_{GD} [fF/mm]
30	1.24	178	302	2.82×10^2	-	0.39	-
80	1.21	127	220	1.05×10^3	1.34	0.38	260
150	1.34	86	178	1.42×10^4	1.28	0.41	139
250	1.17	89	173	1.09×10^4	1.27	0.46	120
90 nm MOSFET	-	85	120	3.1×10^4	1.1	-	-

shown in Fig. 7. Based on these definitions, we extracted I_{ON}/I_{OFF} ratios for our devices at V_{DS} = 0.5 V.

Detailed results, along with other figures of merit of logic, are summarized in Table 1. As L_{side} increases, the I_{ON}/I_{OFF} ratio initially improves rapidly. This is due to the overall sharpening of the subthreshold characteristics and the reduction in the gate leakage current that are seen in Fig. 6. For L_{side} = 150 nm, an I_{ON}/I_{OFF} of 1.4×10^4 is obtained. When L_{side} increases beyond 150 nm, the I_{ON}/I_{OFF} ratio degrades. This is consistent with the drop in maximum current that is observed in Fig. 4 and which arises from increased parasitic resistances. Table 1 also lists the value of the sum of the source and drain access resistance, as measured by gate current injection technique [16]. The increase in $R_S + R_D$ that is observed beyond an L_{side} of 150 nm degrades the current driving capability and the transconductance of the device. This

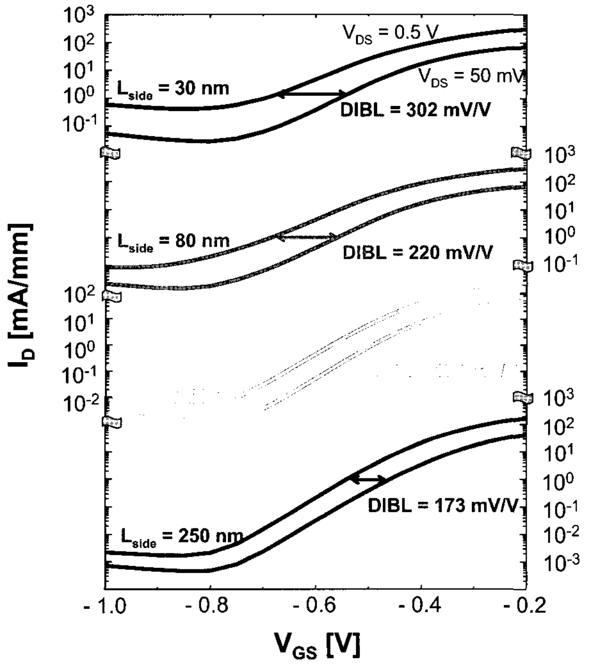

Fig. 8. Subthreshold characteristics of all 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs with four different values of L_{side} at the V_{CC} of 0.05 and 0.5 V.

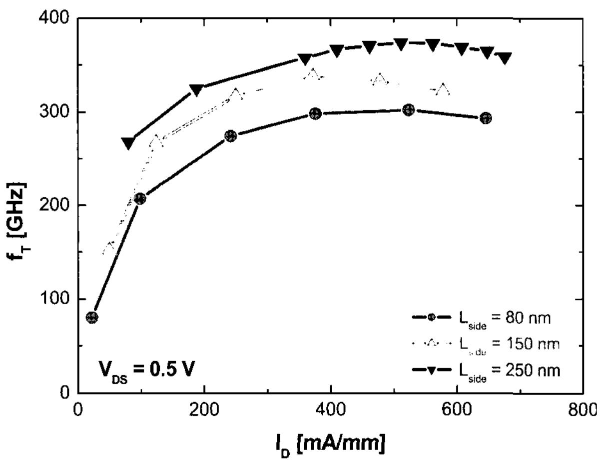

Fig. 9. Cut-off frequency (f_T) as a function of I_D at V_{DS} of 0.5 V.

brings down the I_{ON}/I_{OFF} ratio in our device design.

Fig. 8 compares subthreshold characteristics for the same four devices at the V_{DS} of 50 mV and 0.5 V. Another Figure of merit of logic, called Drain-Induced-Barrier Lowering (DIBL), quantifies the shift of V_T as V_{DS} changes. This has important consequences to CMOS logic circuit design and operation. The device with L_{side} of 150 nm has a much lower DIBL value of 178 mV/V than that with L_{side} of 30 nm (302 mV/V). These are both extracted at I_D = 1 mA/mm. This significant reduction in DIBL as L_{side} increases is another manifestation of an overall improvement in the electrostatic integrity of the device.

In order to characterize the dynamic behavior of our InGaAs HEMTs, we have measured S parameters at high frequencies. Fig. 9 shows f_T as a function of I_D with L_{side} between 80 nm and 250 nm, at a V_{DS} of 0.5 V. The peak f_T improves with increasing L_{side} up to 250 nm. This is consistent with the findings reported in [11], and is primarily attributed to the reduction of the parastic capacitance between the gate and the n+ $In_{0.53}Ga_{0.47}As$ cap on the source and drain. In fact, this can be seen in C_{GD}, also summarized in Table 1, which is extracted at a gate bias with the highest f_T and drain bias of 0.5 V. As L_{side} increases, C_{GD} decreases.

A more important speed-related Figure of merit for logic applications is the gate delay, or CV/I [14]. Here, I is I_{ON} which is defined above, V is the supply voltage (V_{CC}), and C is the total gate capacitance ($C_G = C_{GS} + C_{GD}$) at the same gate bias as I_{ON}., C_G is extracted from S-parameter measurement. Since C_G and I_{ON} are dependent upon the choice of V_T, an appropriate selection of V_T is of some importance, especially for our non-optimized devices [14]. In this work, we have selected a value of V_T that corresponds to I_D = 1 mA/mm. Based on this, we extracted values of CV/I for our devices. The result is also shown in Table 1. It can be seen that increasing L_{side} leads to an improvement in CV/I mostly as a result of the decrease of the parasitic capacitance.

The logic figures of a HEMT are very sensitive to the choice of V_T. The selection of 1 mA/mm made in this

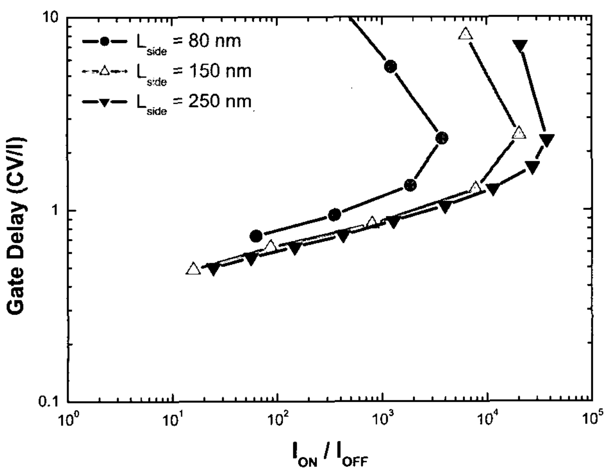

Fig. 10. Gate delay (CV/I) as a function of I_{ON}/I_{OFF} ratio for 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs with three different values of L_{side}.

paper is a common one but it need not be the optimum one for logic circuit operation. It is then of interest to examine the evolution of some of the key figures of merit of the device as the definition of V_T is changed to different current levels. Fig. 10 shows dependency of CV/I on I_{ON}/I_{OFF} ratio for different V_T definitions. Significantly smaller values of gate delay can be obtained if V_T is defined at a higher current level. This is because I_{ON} is also higher. The drawback of this is the degradation of I_{ON}/I_{OFF} ratio owing to the limited gate swing available to shut off the device.

IV. Discussion and Comparison with Si MOSFETs

The findings obtained in this work are broadly consistent with those reported in [11] and suggest a simple picture for the impact of L_{side} on device characteristics. In effect, the n+ InGaAs cap "pins" the potential at the surface of the device to the source voltage on the source side and the drain voltage on the drain side. Side etching of the cap exposes the InP etch stop layer which is undoped. As a result, on the drain side, where the fields are typically much higher, the higher L_{side} is, the lower the electric field at the drain end of the channel becomes. This implies that all things being equal, short-channel effects are mitigated the longer L_{side} is. That is precisely what is observed in the reduction of subthreshold slope and DIBL, and the positive shift in V_T as L_{side} increases.

In addition, it has been reported that the evaporated gate metal is not entirely confined to the second recess but it spreads laterally to some distance over the InP etch stop layer [11]. Thus, in addition to a Schottky contact onto the $In_{0.52}Al_{0.48}As$ barrier layer, there is also a Schottky contact onto the InP etch stop layer. Unfortunately, this is characterized by a low Schottky barrier height and hence provides a relatively high leakage path for the gate current. Increasing L_{side} is also effective in mitigating this peripheral gate leakage current component since the resistance of the InP cap is rather high. Indeed, the reduction in gate leakage current, combined with the improved electrostatic integrity as L_{side} increases, results in a remarkable improvement in the subthreshold characteristics of the device. A third

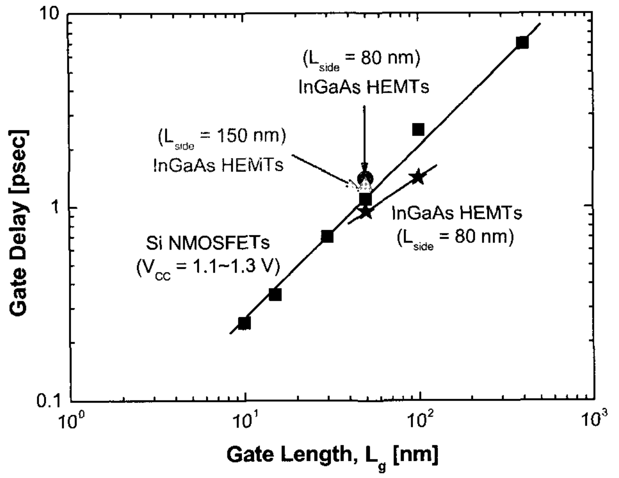

Fig. 11. Gate delay (CV/I) of our 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs as a function of gate length, as well as advanced Si MOSFETs.

advantage of increasing L_{side} is the reduction of parasitic capacitance to the gate. This occurs because as L_{side} increases, so does the distance between the gate and the n+ cap.

The most significant drawback of increasing L_{side} is an increase of the parasitic source and drain access resistance. This makes sense since the resistance of the channel underneath the exposed InP surface is higher than underneath the cap. An increase in source and drain resistance degrades the current driving capability and G_M of the device, as shown in Table 1 and Fig. 5.

Fig. 11 compares the CV/I of our 50 nm InGaAs HEMTs with L_{side} of 80 nm and 150 nm to that of advanced Si-MOSFETs [14] as a function of the gate length (L_g). In this plot, the gate delay of our devices is extracted for a value of V_T corresponding to an I_D of 1 mA/mm. As this Figure shows, the gate delay in our 50 nm InGaAs HEMTs is about the same as that of state-of-the art MOSFETs of similar gate length, even with much lower supply voltage of 0.5 V.

Solid stars in Fig. 11 refer to the best results of our previous study [17], where L_{side} was 80 nm and the gate stem was composed of Pt/Ti/Mo/Au on an $In_{0.52}Al_{0.48}As$ insulator. For consistency, these are for a V_T defined at I_D = 1 mA/mm. In [17], we showed that the use of Pt as the metal at the bottom of the gate stack yields a higher Schottky barrier height. This was found to translate in improvements in the gate leakage current, electrostatic integrity and performance. We bring these data here because it suggests that the combination of an optimized Schottky barrier height, as in [17] and an optimized side recess spacing, as shown in this work, should yield a gate delay markedly below that of comparable Si MOSFETs.

V. CONCLUSIONS

In summary, we have studied the impact of the side-recess spacing (L_{side}) on the logic figures of merit of 50 nm $In_{0.7}Ga_{0.3}As$ HEMTs. We have found that increasing L_{side} has a large impact on the subthreshold characteristics of the device due to a significant reduction of the gate leakage current and an improvement in its electrostatic integrity. In particular, 50 nm $In_{0.7}Ga_{0.3}As$ HEMT with L_{side} of 150 nm exhibited I_{ON}/I_{OFF} ratios in excess of 10^4 with S of 85.5 mV/dec, DIBL of 178 mV/V and a gate delay of 1.28 psec. Our research strongly suggests that the optimization of the L_{side}, combined with the optimization of Schottky barrier height, is essential to improving the overall logic figures of merit of sub-100 nm InGaAs HEMTs.

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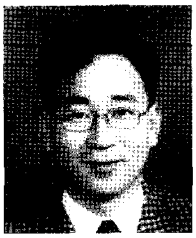

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