High-Speed Digital/Analog NDR ICs Based on InP RTD/HBT Technology

Cheol Ho Kim, Yongsik Jeong, Taeho Kim, Sunkyu Choi, and Kyounghoon Yang

Abstract—**This paper describes the new types of ngative differential resistance (NDR) IC applications which use a monolithic quantum-effect device technology based on the RTD/HBT heterostructure design. As a digital IC, a low-power/high-speed MOBILE (MOnostable-BIstable transition Logic Element)-based D-flip flop IC operating in a non-return-to-zero (NRZ) mode is proposed and developed. The fabricated NRZ MOBILE D-flip flop shows high speed operation up to 34 Gb/s which is the highest speed to our knowledge as a MOBILE NRZ D-flip flop, implemented by the RTD/HBT technology. As an analog IC, a 14.75 GHz RTD/HBT differential-mode voltage-controlled oscillator (VCO) with extremely low power consumption and good phase noise characteristics is designed and fabricated. The VCO shows the low dc power consumption of 0.62 mW and good F.O.M of -185 dBc/Hz. Moreover, a high-speed CML-type multi-functional logic, which operates different logic function such as inverter, NAND, NOR, AND and OR in a circuit, is proposed and designed. The operation of the proposed CML-type multi-functional logic gate is simulated up to 30 Gb/s. These results indicate the potential of the RTD based ICs for high speed digital/analog applications.**

Index Terms—**MOBILE, CML, D-flip flop, Mutifuc tional, VCO, RTD, HBT, InP**

I. INTRODUCTION

Recently, many novel devices using quantum transport phenomena in a nano scale dimension have been introduced, such as a resonant tunneling diode (RTD), a single electron transistor (SET), a resonant interband tunneling diode (RITD), and a heterojunction interband tunnel diode (HITD). These devices have attracted a great deal of interests for high-frequency/low-power applications due to their properties of intrinsic negative differential resistance (NDR) characteristic and high cutoff frequencies [1]. Among these devices, the RTD shows the unique NDR characteristic at a room temperature, hence it is considered as a very promising device in nano–electronics for high-speed/low-power digital and microwave applications. As a digital IC, RTD based NDR ICs such as a 35 Gb/s D-flip flop [2], a 80 Gb/s optoelectronic delayed flip flop [3] and various logic circuits [4, 5] have been reported. As an analog IC, several tunneling diode MMIC VCOs have been reported especially for their advantages of low power consumption [6, 7].

In this work, in order to further investigate the potential performance characteristics of the RTD based IC, we have integrated the RTD and HBT monolithically on an InP substrate. As a result, a low-power/high-speed MOBILE-based NRZ D-flip flop IC is proposed and implemted using an InP-based monolithic RTD/HBT IC technology. And a differential RTD/HBT VCO with the wide frequency tuning range and a low phase noise was successfully implemented. Moreover, a CML-type multi-functional logic gate with different logic operation is proposed and the operation of the circuit is simulated.

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II. InP-Based RTD/HBT MMIC Technology

The proposed MOBILE-based NRZ D-flip flop and the differential RTD/HBT VCO were fabricated by using an InP-based monolithic RTD/HBT IC technology with a minimum feature size of 2 μm. Fig. 1 shows a schematic cross-sectional view of the monolithically integrated RTD and HBT IC. The RTD and HBT were integrated on an InP substrate. First, InP/InGaAs single HBT layers were grown, then InP-based pseudomorphic AlAs/InGaAs/InAs/InGaAs/AlAs RTD layers were grown on the top of the HBT layers by MBE. The devices were fabricated by optical lithography and the wet etching technique. The detailed layer structure and fabrication sequence are described elsewhere [9]. As shown in Fig. 2(a), the fabricated RTD exhibits a peak current density (J_P) of 100 kA/cm^2 with a good peak-to-valley current ratio (PVCR) of 13 at room temperature. The peak voltage of the device was 0.28 V. Fig. 2(b) shows the measured common-emitter output characteristics of a 2 × 5 μm^2-emitter-area HBT. The HBT showed a current gain of 50 with a turn-on voltage of 0.75 V. The maximum f_T and f_{max} of the fabricated HBT were 99 GHz and 104 GHz, respectively.

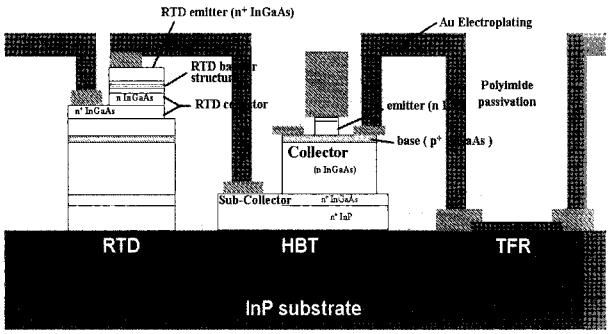

Fig. 1. Schematic cross-sectional view of monolithically integrated RTD and HBT.

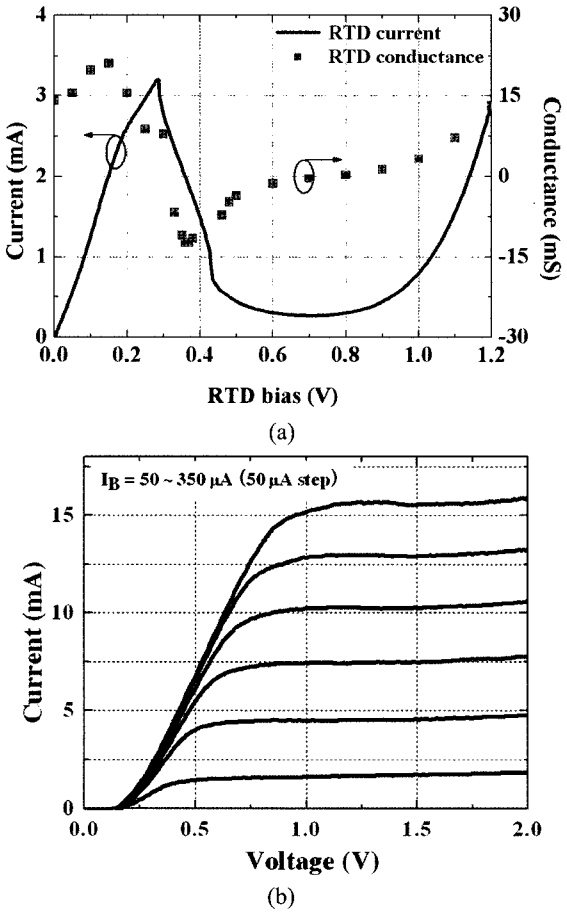

Fig. 2. Measured current-voltage characteristics of RTD and HBT. (a) RTD (b) HBT.

III. MOBILE-Based NRZ D-Flip Flop

As a digital application, a high-speed D-flip flop is a key component for applications such as multi-gigabit data communication systems and microwave/millimeter-wave wireless communication systems. To realize high-speed/low-power digital circuits, the NDR digital ICs using RTDs such as a 35 Gb/s D-flip flop [2] and a 80 Gb/s optoelectronic delayed flip flop [3] in a return-to-zero (RZ) mode have been also intensively studied demonstrating their advantages of intrinsic high-speed operation and low-power consumption. However, in order to enable the RTD-based NDR ICs to be compatible with the conventional SCFL or ECL architecture, the RTD-based NDR IC operating in a non-return-to-zero (NRZ) mode is needed. We proposed and implemented a low-power/high-speed MOBILE (MOnostable-BIstable transition Logic Element)-based NRZ D-flip flop IC using an InP-based monolithic RTD/HBT IC technology. The proposed IC provides the differential outputs as well as the compatibility with the conventional emitter-coupled logic (ECL) architecture.

The circuit configuration of the proposed MOBILE D-flip flop is shown in Fig. 3. The circuit is composed of a CML-type MOBILE core (Q_1, Q_2, RTD_1~RTD_4) generating the complementary RZ-mode outputs [9] and a CML-type SET/RESET latch (Q_3, Q_4, RTD_5, RTD_6)

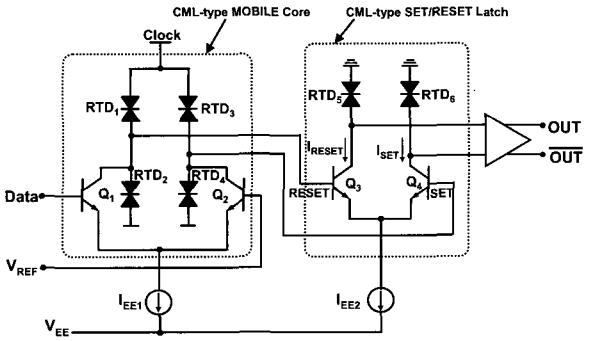

Fig. 3. Circuit configuration of non-return-to-zero (NRZ) D-flip flop using a CML-type MOBILE IC with complementary outputs and a SR latch.

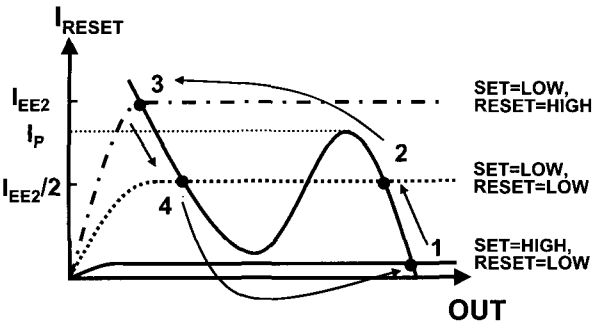

Fig. 4. The non-inverted (OUT) output voltage characteristics with respect to the SET and RESET voltages.

[10]. As shown in the figure, the device count in the proposed circuit is about 1/2 of that of the conventional master/slave D-flip flop configuration. The proposed MOBILE D-flip flop is designed to function as an NRZ-mode edge-triggered D-flip flop based on the MOBILE scheme. At the rising edge of clock signal, the RZ-mode SET and RESET signals generated from the CML-type MOBILE core are determined by the input data and maintain their state as long as the clock stays HIGH [9]. When the clock signal is LOW, both the SET and RESET signals are at the LOW logic level. In order to sense and store the SET and RESET signals, the CML-type SET/RESET latch (SR-latch) has been designed and integrated into the MOBILE D-flip flop. Fig. 4 shows the non-inverted ($\overline{OUT}$) and inverted ($\overline{OUT}$) output voltage characteristics with respect to the SET and RESET voltages. For the case that the SET voltage is higher than the RESET voltage, where I_{SET} becomes I_{EE2} with I_{RESET}=0 due to the emitter-coupled CML configuration, the voltage levels of $\overline{OUT}$ and $\overline{OUT}$ become HIGH and LOW, respectively. When both the SET and RESET voltages are LOW, the outputs of the SR-latch maintain the previous logic states with both

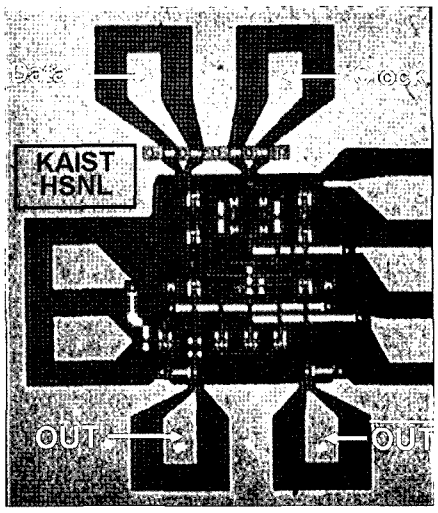

Fig. 5. Microphotograph of the fabricated RTD/HBT MOBILE D-flip flop.

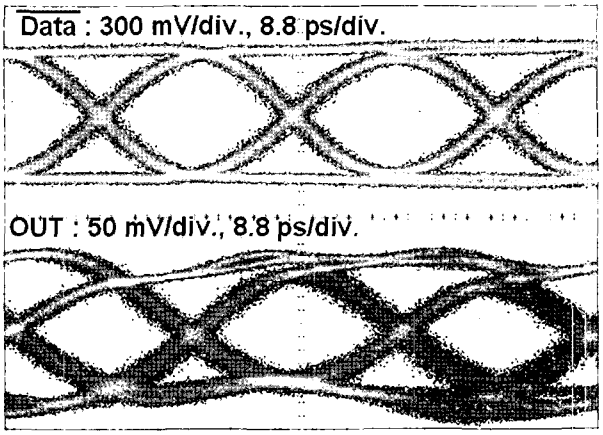

Fig. 6. Measured eye diagram for input, and non-inverted output of the fabricated RTD/HBT MOBILE D-flip flop at 34 Gb/s operation.

I_{SET} and I_{RESET} at a value of $I_{EE2}/2$. Consequently, this circuit operates as an edge-triggered NRZ D-flip flop with the differential outputs.

A chip micrograph of the fabricated MOBILE D-flip flop is shown in Fig. 5. The layout symmetry necessary for high-speed operation of the D-flip flop has been considered in the IC layout design. Fig. 6 shows the measured eye diagram of data (upper) and output (lower) of the MOBILE-based NRZ D-flip flop integrated with a common-emitter buffer at 34 Gb/s. As shown in this figure, the output eye pattern with a peak-to-peak amplitude of 100 mV has been obtained at this bit rate. The peak-to-peak jitter of the output was 9.0 ps, and the rms jitter was 1.4 ps. So, the operation of the fabricated MOBILE-based NRZ D-flip flop has been demonstrated up to 34 Gb/s. The measured DC power consumption of

the proposed D-flip flop was 35 mW, which is about 1/5 of the conventional ECL D-flip flops [11]. The low power consumption and reduced device count of the MOBILE-based NRZ D-flip flop have been successfully achieved by using the CML-type MOBILE core and the CML-type SET/RESET latch. Since the proposed D-flip flop has been implemented by using an InP-based monolithic RTD/HBT IC technology with a minimum feature size of 2 μm, improved high-speed performance of the IC can be feasible by using a further scaled-down device technology.

IV. RTD/HBT VCO

As an analog application of the RTD based IC, the low power differential VCO based on RTD/HBT technology is developed. In microwave and millimeter-wave wireless communication systems, a voltage controlled oscillator (VCO) is a crucial circuit block, which is used as a local oscillator or up and down converters. For the VCOs, one of the important performance requirements is low power consumption. As an anlog IC, we have designed and fabricated the differential-mode VCO based on RTD/HBT MMIC technology in order to reduce the power consumption. The differential-mode VCO is known to be immune to the common mode noise, such as supply and substrate noise.

Fig. 7 shows a circuit schematic of the proposed differential RTD/HBT MMIC VCO. The topology and principle of the differential RTD/HBT VCO is similar to that of the conventional balanced differential-mode VCO [12]. The ac virtual ground forms at the node between the varactors and at the node between the inductors. The overall VCO produces the differential outputs, and this topology can also reduce the phase noise due to its immunity to the common-mode noise generated from the power supply and substrate. The core VCO circuit comprises 1 × 1 μm^2 RTDs and parallel L-C resonators, and the HBT emitter-follower buffers are connected to the core VCO. The VCO is designed based on the one-port negative resistance oscillator topology. The RTD which has the negative differential resistance is used as the negative resistance cell in the one-port oscillator. To initiate the oscillation, the magnitude of the effective negative resistance ($|R_N|$) generated by the RTD has to be smaller than the overall resistance consisting of the effective input shunt resistance of the buffer (R_{Buffer}) and the equivalent resistance of the resonator (R_{RES}), such as $|R_N| < R_{Buffer}// R_{RES}$. The emitter follower buffer is integrated to isolate the VCO core from the output 50 Ω load for measurement. In this topology, the required supply voltage is determined by the NDR voltage range of the RTD. The NDR voltage range of the InP based RTD is about from 0.3 V to 0.7 V. Hence, a very low supply voltage can be used in the VCO core circuit, which reduces the DC power consumption significantly compared to the conventional-type VCO. The good phase noise performance is also expected by using the low noise active/passive devices based on the InP technology [13]. In addition, the frequency tuning range of the VCO can be increased by using the base-collector p-n junction of the HBT as a varactor in the integrated L-C resonators.

Fig. 8 shows the microphotograph of the fabricated 14.75 GHz differential RTD/HBT MMIC VCO. The area of the VCO circuit excluding pads is about 540 × 340 μm^2. As shown in Fig. 9, the output spectrum of the

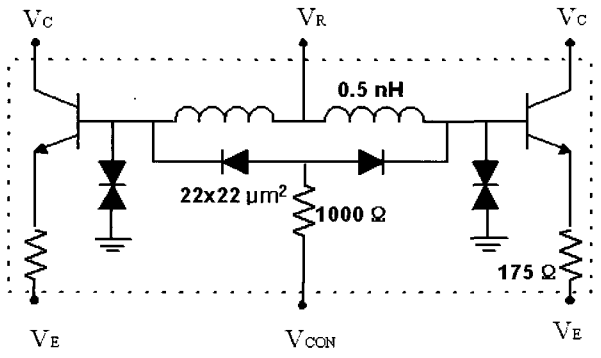

Fig. 7. Circuit schematic of the differential RTD/HBT MMIC VCO.

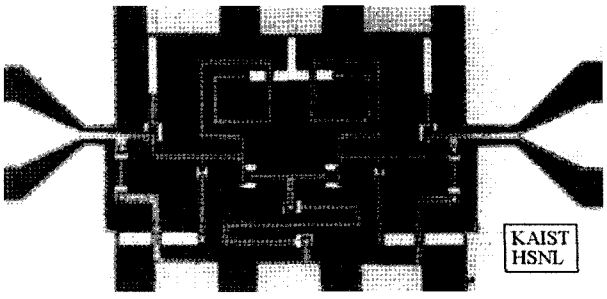

Fig. 8. Microphotograph of the differential RTD/HBT MMIC VCO.

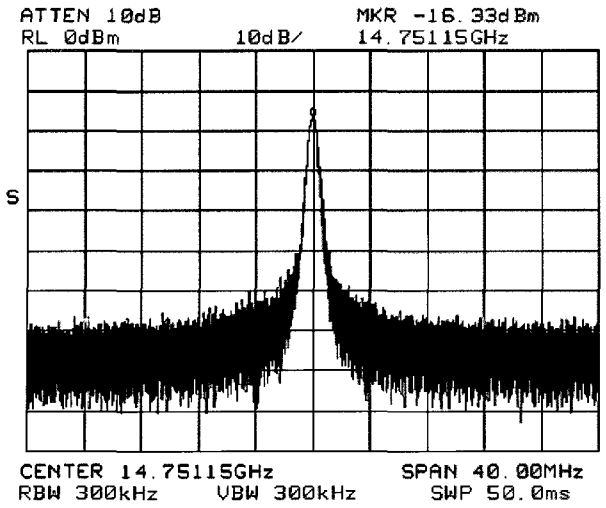

Fig. 9. Measured output spectrum of the differential RTD/HBT MMIC VCO at a bias current of 3.7 mA and a bias voltage of 0.34 V.

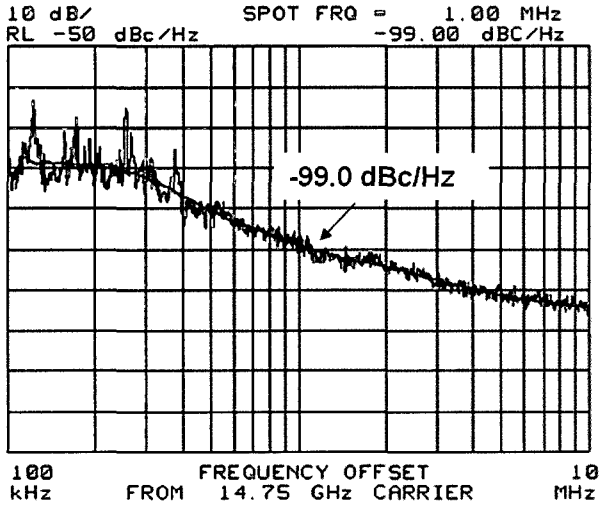

Fig. 10. Measured phase noise versus the offset frequency for the differential RTD/HBT MMIC VCO.

VCO shows an oscillation frequency of 14.75 GHz. An output power of -16.33 dBm was obtained at a bias current of 1.56 mA and a supply voltage of 0.4 V from the VCO core. The corresponding DC power consumption is 0.62 mW. The DC power of 0.62 mW is the lowest value reported among Ku-band differential VCOs to the authors' knowledge. The measured phase noise of the VCO was obtained to be -99 dBc/Hz at 1 MHz as shown in Fig. 10. The frequency tuning range of 1.65 GHz was obtained from 13.1 GHz to 14.75 GHz, which is about 11.1 % of the center frequency of oscillation. The widely used figure of merit (FOM) [14] is defined as:

$$FOM = L\{\Delta f\} - 20 \cdot \log\left(\frac{f_0}{\Delta f}\right) + 10 \cdot \log\left(\frac{P_{DC}}{1mW}\right) \quad (1)$$

with L{Δf}, which is the phase noise measured at an offset frequency (Δf) from the center frequency (f) for the measured DC-power consumption (P) of the VCO core. The obtained figure-of-merit from the differential MMIC RTD VCO in this work is -185 dBc/Hz. These results demonstrate the potential of the RTD based MMIC VCOs with low DC power consumption for wireless sensor applications.

V. Multi-functional Logic Gate

As a binary logic gate of the RTD based IC, a multi-functional logic gate based on RTD/HBT technology is developed. The binary logic gates such as AND, OR, NOR and NAND are key building logic in high-speed digital applications. The logic gates based on RTDs have generated substantial research interests owing to their unique negative differential resistance (NDR). By using the NDR feature of RTD, circuit complexity can be greatly reduced and new circuit applications have also emerged. Recently, the programmable logic gates based on controlled quenching of series-connected NDR devices have been reported demonstrating the logic functions (AND, OR, NAND, NOR, XNOR) by the control gate voltages of V_{CON1} and V_{CON2} [15].

In this work, a new CML-type multi-functional logic gate using InP-based RTD/HBT technology is proposed. The proposed circuit can operate logic functions such as inverter, NAND, NOR, AND and NOR by the control biases. The operation of the circuit is simulated up to 30 Gb/s.

Fig. 11 shows a circuit configuration of the proposed CML-type multi-functional logic gate. The circuit is composed of the two basic MOBILE pairs (RTD_1, RTD_2, RTD_3 and RTD_4) and the two CML-type input gates (V_A and V_B). The current I_A and I_B of the current sources are controlled by V_{CONA} and V_{CONB}, respectively. And the currents I_1 and I_2 flowing in parallel with RTD_1 and RTD_3 are determined by the following equations.

$$I_1 = A \cdot I_A + B \cdot I_B \text{ and } I_2 = \overline{A} \cdot I_A + \overline{B} \cdot I_B. \quad (2)$$

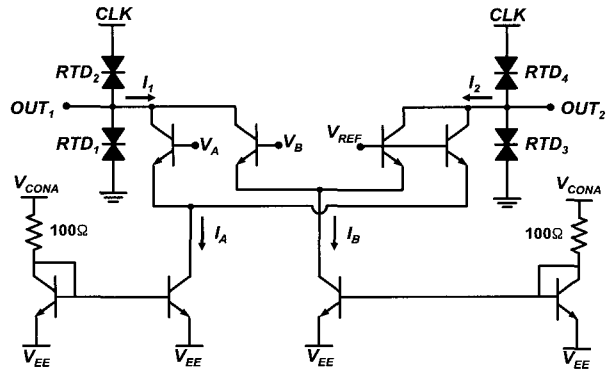

Fig. 11. Circuit configuration of CML-type MOBILE-based multi-functional logic.

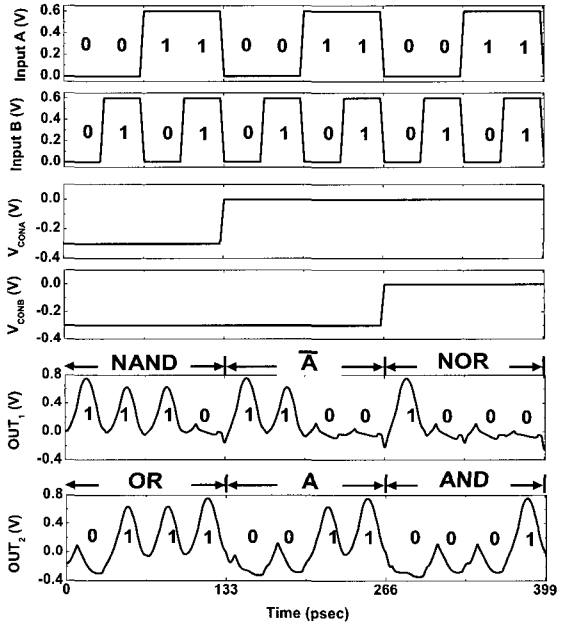

Fig. 12. Simulated results of the proposed CML-type multi-functional logic with respect to various control bias voltages at 30 Gb/s operation.

Where I_A and I_B are currents of the current sources controlled by V_{CONA} and V_{CONB}, respectively. At the rising edge of a clock bias, the OUT_1 (or OUT_2) is determined by the difference between $I_{P1} + I_1$ (or $I_{P3} + I_2$) and I_{P2} (or I_{P4}), where I_{P1} and I_{P2} are peak currents of RTD_1 and RTD_2. As an example, to realize NAND logic function, control bias voltages V_{CONA} and V_{CONB} are adjusted such that $I_{P1} < I_{P2}$ (OUT_1 high) when both V_A and V_B are logic "0", $I_{P1} + I_A < I_{P2}$ or $I_{P1} + I_B < I_{P2}$ (OUT_1 high) when either V_A or V_B is logic "1", and $I_{P1} + I_A + I_B > I_{P2}$ (OUT_1 low) when both V_A and V_B are logic "1". Table 1 shows the combination of the control bias voltages for each logic function of the CML-type multi-functional logic gate. Fig. 12 shows the simulated

Table 1. Combination of the control bias voltages for each logic function.

Control bias		Logic function	
V_{CONA}	V_{CONB}	OUT_1	OUT_2
-0.3 V	-0.3 V	NAND	OR
0.0 V	-0.3 V	$\overline{A}$	A
-0.3 V	0.0 V	$\overline{B}$	B
0.0 V	0.0 V	NOR	AND

results of the circuit with respect to various control bias conditions at 30 Gb/s operation. The logic function of OUT_1 are changed to NAND, $\overline{A}$, and NOR, while the logic function of OUT_2 are changed to AND, A and OR with respect to the control bias voltages. As shown in the figure, the logic functions at various control bias voltages have been successfully simulated up to 30 Gb/s operation.

VI. CONCLUSIONS

The new types of IC applications using a monolithic quantum-effect device technology based on the RTD/HBT heterostructure design were described. As a digital IC, a low power/high-speed MOBILE (MOnostable-BIstable transition Logic Element)-based D-flip flop IC operating in a non-return-to-zero (NRZ) mode was proposed and developed. The operation of the fabricated MOBILE-based NRZ D-flip flop with the differential outputs has been confirmed with an output voltage swing of 100 mV at 34 Gb/s with a low power consumption of 35 mW. As an analog IC, the 14.75 GHz RTD/HBT differential-mode VCO was implemented with extremely low power consumption of 0.62 mW and good phase noise performance of -99 dBc/Hz at 1 MHz frequency offeset. Moreover, the CML-type multi-functional logic gate was designed and the various logic gate operations of the circuit with respect to the control biases were successfully simulated up to 30 Gb/s. These results indicate the potential of the RTD based ICs for high speed/low power digital/analog applications.

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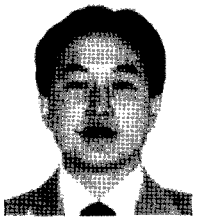

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