Analytical Model for Metal Insulator Semiconductor High Electron Mobility Transistor (MISHEMT) for its High Frequency and High Power Applications

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Abstract—**A new analytical model has been proposed for predicting the sheet carrier density of Metal insulator Semiconductor High Electron Mobility Transistor (MISHEMT). The model takes into account the non-linear relationship between sheet carrier density and quasi Fermi energy level to consider the quantum effects and to validate it from subthreshold region to high conduction region. Then model has been formulated in such a way that it is applicable to MESFET/HEMT/MISFET with few adjustable parameters. The model can also be used to evaluate the characteristics for different gate insulator geometries like T-gate etc. The model has been extended to forecast the drain current, conductance and high frequency performance. The results so obtained from the analysis show excellent agreement with previous models and simulated results that proves the validity of our model.**

Index Terms—**MISHEMT, HEMT, MESFET, MISF ET, Threshold voltage, Conductances.**

I. INTRODUCTION

High electron mobility transistors (HEMTs) play a vital role in optical fiber communication and millimeter wave applications due to higher transport properties and larger sheet carrier density in the two-dimensional quantum well. However, some analog applications of HEMTs are still limited by gate-drain breakdown mechanism as well as by forward bias current drawn by Schottky barrier gate [1-8]. Several approaches have been used to overcome this problem. A higher channel doping concentration results in larger drain current and low series resistance, desirable for higher output power. On the contrary, increasing channel doping concen tration decreases the breakdown voltage of the Schottky barrier gate. A deep gate recess combined with thick, lightly doped channel layer may achieve high I_{DS} but the processing is made more difficult, and this design lowers the gate-drain avalanche breakdown voltage [9]. Device improvement can also be achieved by altering the doped layer concentration from uniformly doped to delta doped and eliminates some problems like reduced trapping effect, low breakdown voltage and high gate leakage current. Furthermore an introduction of Schottky layer between gate and doped layer provides high channel electron density, improved threshold voltage control, reduced parallel conduction at high gate-to-source voltage, and improved current drive capability and high transconductance which is due to high electron density and small gate-to-channel spacing. However, the resistivity of an undoped AlGaAs (InAlAs) layer is insufficient to achieve true MIS like gate characteristics, so a perfect insulator is clearly needed. Growing the insulator on AlGaAs/GaAs (InAlAs/InGaAs) heteros tructure improves the device performance further, as this device is attributed to MIS structure as well as hetero-structure. MISFET's with different types of insulators layers (LT AlGaAs (InAlAs) layer on GaAs (InGaAs/ InP or InP) or MIS like structure [10-29]) have been fabricated and have shown some success [12] to improve

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the power performance of FET's. Improved breakdown voltages and power capability have been demonstrated for these MISFET's compared to conventional MES FET's and HEMT's.

In the present paper this structure has been analyzed analytically considering an insulator between the gate and high band gap semiconductor forming hetero junction with low band gap semiconductor and is shown in Fig. 1. Sheet carrier density has been formulated considering two isolated structure (MIS and hetero juction) brought in contact [31], where MIS can be converter to MS contact and effect of heterojuction can be completed eliminated with few adjustable parameters.

Hence a model has been developed to give a common representation (or a single analytical model) for heterojunction MISFET, MISFET, MESFET, HEMT devices. The model also takes into account the non-linear relationship between sheet carrier density and quasi Fermi energy level [32] to consider the quantum effects and to validate it from subthreshold region to high conduction region. The expression for sheet carrier density obtained from the analysis shows excellent agreement with previous models that proves the validity of our model. The model has been extended to forecast the drain current, conductance and high frequency performance. The results obtained have also been verified with simulated and previous published results.

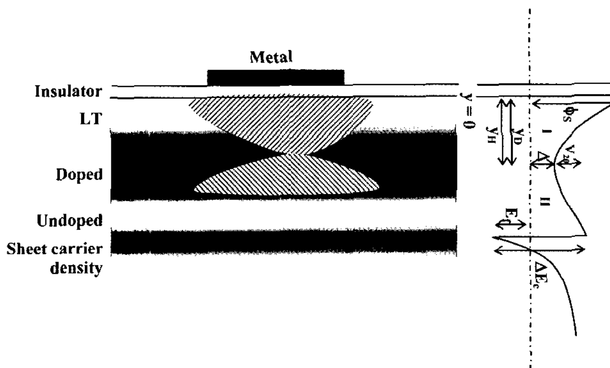

Fig. 1. Cross-sectional view of Pulsed doped Heterojunction Metal insulator semiconductor field effect transistor along with the coordinate system and conduction band diagram.

II. MODEL FORMULATION

MISHEMT can be viewed as two separate isolated structures brought in contact (one is the Metal insulator Semiconductor and the other is the heterostructure). When the two regions are coupled, the depletion regions at both sides will overlap and interpenetrate before parallel conduction starts thus raising the potential (Δ) at the interface of overlapped depletions and forming region-I and region-II as shown in Fig. 1. The 2DEG results from the transfer of free carriers from the undepleted region to the quantum well.

Analysis for region I

In the band diagram $y=d_T$ represents the hetero junction and $y=0$, represents the MIS contact. Depletion due to MIS contact gives rise to depletion width, y_D and overlapping of two regions give rise to potential, Δ. The Poisson equation in depletion region-I is

$$\frac{\partial^2 \psi_1}{\partial y^2} = -\frac{\rho}{\varepsilon_o . \varepsilon_s} \tag{1}$$

and is subjected to the following boundary conditions

$$\psi_1 = \phi_s,\ \frac{\partial \psi_1}{\partial y} = -E_s \quad \text{at} \quad y=0$$

$$\frac{\partial \psi_1}{\partial y} = 0,\ \psi_1 = \Delta \quad \text{at} \quad y=y_D \tag{2}$$

where the effect of overlapping of two regions is considered in boundary condition for $y = y_D$, ε_s is the dielectric permittivity of high band gap semiconductor layer and ρ is the space charge density given by

$$\rho = q\,N(y) \quad \text{for} \quad y \geq y_D = 0$$
$$\text{for} \quad y < y_D \tag{3}$$

and for pulsed doped structure,

$$N(y) = 0 \quad \text{for} \quad 0 \leq y \leq d_i$$
$$= N_D \quad \text{for} \quad d_i \leq y \leq d_i + d_a$$
$$= 0 \quad \text{for} \quad d_i + d_a \leq y \leq d_T \tag{4}$$

in which d_i is the thickness of (low-temperature grown) LT high band gap semiconductor, d_a is the dopant layer thickness and d_T (= $d_s + d_a + d_i$) is the channel depth. Solving (1) leads to

$$E_s = -\frac{qN_D}{\varepsilon}(y_D - d_i)$$

$$\phi_s = \Delta + \frac{q.N_D}{2.\varepsilon}\left(-y_D^2 + d_i^2\right) \quad (5)$$

and from charge neutrality condition at the metal insulator semiconductor interface

$$\phi_s = V_g - \phi_{ms} - V_I \quad (6)$$

in which, $\phi_{ms}\left(=\phi_m - \left(\chi_s + E_g/2 - \phi_n + \phi_p\right)\right)$ is the work function difference between bulk semiconductor and the gate electrode, $V_I\left(= -qN_D t_I (y_D - d_i)/\varepsilon_o\varepsilon_I\right)$ is voltage across the insulator, and $\phi_n = \frac{k.T}{q}\ln\left(\frac{N_D}{n_i}\right)$. Substituting the value of ϕ_{ms}, ϕ_n and V_I in (6) and using (5) leads to

$$y_D = -\frac{\varepsilon_s.t_I}{\varepsilon_I} + \sqrt{\left(\frac{\varepsilon_s.t_I}{\varepsilon_I}\right)^2 + \frac{2.\varepsilon_s.t_I.d_i}{\varepsilon_I} + d_i^2 + \frac{2.\varepsilon_o.\varepsilon_s}{q.N_D}.\left(\phi_{ms} - V_g + \Delta\right)} \quad (7)$$

the free carrier density can be obtained as

$$n_s = N_D\left(d_i + d_a - y_D\right) \quad (8)$$

these free carriers are transferred to the quantum well depending on the value of Δ i.e., the free carrier density will be equal to 2DEG sheet carrier density before Δ=0. The rest of the free carriers will participate in conduction in high band gap semiconductor region (condition for parallel conduction). It can be noted here that (8) can be used for calculating the free carrier density of buried channel MISFET by substituting Δ=0 and the same expression can also be used for the analysis of MESFET by substituting $t_I = 0$ for any arbitrary non zero value of ε_I.

Analysis for region II

At equilibrium, relation between Δ and V_{20} can be seen from Fig. 1 as

$$\Delta + V_{20} = -\Delta E_c + E_f \quad (9)$$

V_{20} is obtained by solving Poisson's equation in the depletion region-II due to heterostructure and assuming the density of free carriers to be non zero in the undepleted region present after being depleted by the gate electrode, i.e., carriers obtained from region I are given by

$$N(y) = N_D \quad \text{for} \quad y_H \le y \le y_H + d_s$$
$$N(y) = 0 \quad \text{for} \quad y_H + d_s \le y \le d_T \quad (10)$$

in which y_H is the depletion width formed by transfer of carriers to the quantum well. On solving the Poisson's equation

$$\frac{\partial^2\psi_2}{\partial y^2} = -\frac{\rho}{\varepsilon} \quad (11)$$

for depletion region-II under the following boundary conditions

$$\frac{\partial\psi_2}{\partial y} = 0,\ \psi_2 = \Delta \quad \text{at} \quad y = y_H$$
$$\psi_2 = V_{20} + \Delta \quad \text{at} \quad y = d_T \quad (12)$$

we get,

$$V_{20} = -\frac{qN_D d_a^2}{2.\varepsilon_o.\varepsilon_s} - \frac{q.N_D.d_a.d_s}{\varepsilon_o.\varepsilon_s} + \frac{q.N_D.d_T}{\varepsilon_o.\varepsilon_s}.\left(y_H - d_i\right) + \frac{q.N_D}{2.\varepsilon_o.\varepsilon_s}.\left(-y_H^2 + d_i^2\right) \quad (13)$$

then from (9)

$$\Delta = \frac{qN_D d_a^2}{2.\varepsilon_o.\varepsilon_s} + \frac{q.N_D.d_a.d_s}{\varepsilon_o.\varepsilon_s} - \frac{q.N_D.d_T}{\varepsilon_o.\varepsilon_s}.\left(y_H - d_i\right) - \frac{q.N_D}{2.\varepsilon_o.\varepsilon_s}.\left(-y_H^2 + d_i^2\right) - \left(\Delta E_c - E_f\right) \quad (14)$$

where the above equation is valid before parallel conduction start, otherwise Δ = 0. Before parallel conduction starts all the undepleted charges left out from metal-insulator-semiconductor contact are transfered to the quantum well, then y_D and y_H are the same. Substituting the value of Δ in (7), for $y_D = y_H$ we get

$$y_D = \frac{d_T.d_i + d_a.d_s + \frac{d_a^2}{2} + \frac{\varepsilon_s.t_I.d_i}{\varepsilon_I} - \frac{\varepsilon_o.\varepsilon_s.(V_g - \phi_{ms} + \Delta E_c - E_f)}{q.N_D}}{d_T + \frac{\varepsilon_s.t_I}{\varepsilon_I}} \quad (15)$$

in which d_i is the Schottky layer thickness, then substituting the value of y_D in (8), one can easily obtain the expression for sheet carrier density of heterojunction MISFET, and is given by

$$n_s = \frac{\varepsilon_o.\varepsilon_s}{q.\left(d_T + \frac{\varepsilon_s.t_I}{\varepsilon_I}\right)}.\left(\frac{q.N_D.t_I.d_a}{\varepsilon_o.\varepsilon_I} + \frac{q.N_D.d_a^2}{2.\varepsilon_o.\varepsilon_s}.\left(1 + \frac{2.d_i}{d_a}\right) + V_g - \phi_{ms} + \Delta E_c - E_f\right) \quad (16)$$

for $t_I = 0$ (for HEMT) leads to

$$n_s = \frac{\varepsilon_o.\varepsilon_s}{q.d_T}.\left(\frac{q.N_D.d_a^2}{2.\varepsilon_o.\varepsilon_s}.\left(1 + \frac{2.d_i}{d_a}\right) + V_g - \phi_{ms} + \Delta E_c - E_f\right)$$

which is found to be the same expression as reported earlier [33].

Threshold voltage

Channel is said to reach at threshold if free carriers are zero i.e., depletion width due to metal-insulator-semi conductor contact is equal to $d_i + d_a$, and is obtained as.

$$V_{TH}|_{HMISFET} = \phi_{ms} - \Delta E_c - \frac{q.N_D.d_a^2}{2.\varepsilon_o.\varepsilon_s}\left(1 + \frac{2.d_i}{d_a}\right) - \frac{q.N_D.t_I.d_a}{\varepsilon_o.\varepsilon_I} + k_1 \quad (17)$$

where k_1 is resulted from variation of quasi Fermi level with 2DEG sheet carrier density to include subthreshold region. In the absence of heterostructure it is defined as

$$V_{TH}|_{MISFET} = \phi_{ms} - \frac{q.N_D.d_a^2}{2.\varepsilon_o.\varepsilon_s}\left(1 + \frac{2.d_i}{d_a}\right) - \frac{q.N_D.t_I.d_a}{\varepsilon_o.\varepsilon_I} \quad (18)$$

Substituting $t_I = 0$ in (17) leads to the expression of threshold voltage for HEMT, given by

$$V_{TH}|_{HEMT} = \phi_{ms} - \Delta E_c - \frac{q.N_D.d_a^2}{2.\varepsilon_o.\varepsilon_s}\left(1 + \frac{2.d_i}{d_a}\right) + k_1 \quad (19)$$

which is found to be the same expression as reported earlier [33]. In the absence of heterostructure it is defined as

$$V_{TH}|_{MESFET} = \phi_{ms} - \frac{q.N_D.d_a^2}{2.\varepsilon_o.\varepsilon_s}\left(1 + \frac{2.d_i}{d_a}\right) \quad (20)$$

this shows that introduction of insulator between metal and semiconductor decreases the threshold voltage by an amount equal to $\frac{q.N_D.t_I.d_a}{\varepsilon_o.\varepsilon_I}$ and the formation of heterostructure increases the threshold voltage to an amount equal to $\Delta E_c - k_1$ in comparison to MESFET and MISFET, i.e.,

$$\begin{aligned}
V_{TH}|_{HMISFET} &= V_{TH}|_{HEMT} - \frac{q.N_D.t_I.d_a}{\varepsilon_o.\varepsilon_I} \\
V_{TH}|_{HMISFET} &= V_{TH}|_{MISFET} - \Delta E_c + k_1 \\
V_{TH}|_{HEMT} &= V_{TH}|_{MESFET} - \Delta E_c + k_1 \\
V_{TH}|_{HMISFET} &= V_{TH}|_{MESFET} - \frac{q.N_D.t_I.d_a}{\varepsilon_o.\varepsilon_I} - \Delta E_c + k_1
\end{aligned} \quad (21)$$

III. Drain Current and Conductances

The expression for drain current and conductances can easily be derived from the expression proposed in our earlier work [33] by replacing the expression of threshold voltage with newer one and $\beta = \frac{\varepsilon_o.\varepsilon_S}{q\left(d_T + \frac{\varepsilon_S.t_I}{\varepsilon_I}\right)}$.

IV. LT-MISHEMT and Perfect Insulator MISHEMT

Threshold voltage of LT-MISFET is given by (18) whereas for perfect insulator MISHEMT (in which there is no LT layer, i.e. $d_i = 0$) it is given by

$$V_{TH}\big|_{HMISFET} = \phi_{ms} - \Delta E_c - \frac{q.N_D.d_a^{\,2}}{2.\varepsilon_o.\varepsilon_s} - \frac{q.N_D.t_I.d_a}{\varepsilon_o.\varepsilon_I} + k_1 \quad (22)$$

equating (18) and (22) gives the equivalence between LT-MISHEMT and MISHEMT, and is given by

$$t_I = \frac{d_i\varepsilon_I}{\varepsilon_s} \quad (23)$$

here it can be noted that the same equivalence can be established between the perfect insulator MISFET and the LT-MISFET.

V. Results and Discussion

The model have been formulated to predict the sheet carrier density of Metal insulator heterojunction FET (MISHFET), MISFET, HEMT and MESFET and has been extended to evaluate drain current, conductance and cut-off frequency of the device. The parameters used for comparing the characteristics of these devices are of SiO2/InAlAs/InGaAs and are tabulated in Table. 1.

The variation of depletion width with gate voltage for two isolated structures (one is the metal semiconductor contact with or without insulator and other is the heterostructure) is shown in Fig.2. The depletion width as a result of metal semiconductor contact with or without insulator reaches its maximum value at gate voltage of -1.761V and–0.696V (threshold voltage) showing the availability of zero free carriers in the conduction band of high band gap semiconductor. This

Table 1. List of Parameters.

Parameters	Value
d_s (Å)	20
d_a (Å)	100
d_i (Å)	100
N_d (m^{-3})	2.0×10^{24}
L (μm)	0.25
t_I	100
μ (m^2/V sec)	1
v_{sat} (m/sec)	3.2×10^5
R_s (Ω)	0.3
R_d (Ω)	1
T (K)	300

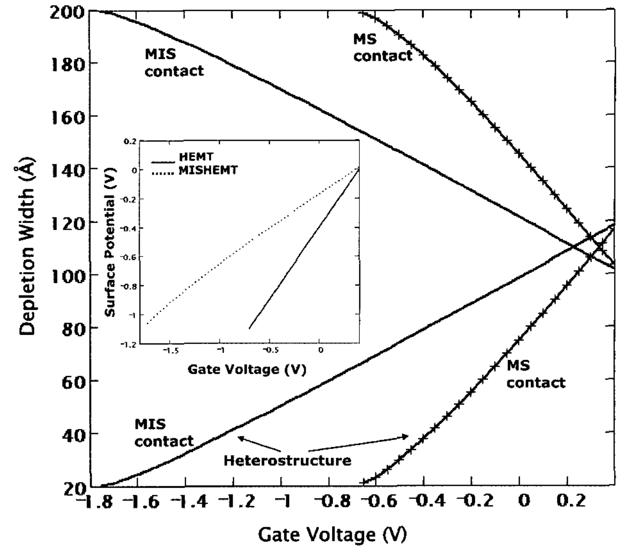

Fig. 2. Variation of depletion width with gate voltage for metal semiconductor contact and heterostructure with or without insulator.(inset) Variation of surface potential with gate voltage for heterojunction metal insulator semiconductor field effect transistor.

elucidates that with the introduction of insulator between metal and semiconductor, threshold voltage increases owing to the additional voltage drop across the insulator (inset of the figure). With increase in gate voltage from threshold voltage, the depletion width due to metal semiconductor contact reduces. As a result some electrons will transfer from high band gap semiconductor to low band gap semiconductor thereby increasing the 2DEG sheet carrier density. From the figure it is clear that the decrease in depletion width due to metal semiconductor contact is more effective in contrast to device with insulator. This will lead to increase in overall gate voltage swing; which is an important parameter for designing a large signal amplifier. Further increase in gate voltage (i.e. 0.2V and 0.35V for metal semiconductor with or without insulator) increases 2DEG sheet carrier density to its maximum value. After this gate voltage, no further transfer of free carriers from high band gap semiconductor to quantum well takes place, which results in some free carriers or undepleted region in high band gap semiconductor. At this voltage conduction band in high band gap semiconductor region crosses the Fermi-level (showing Δ = 0). Further increase in gate voltage will only undeplete the dopant region leading to increase in free carriers in the high band gap semiconductor and the 2DEG remain

unaffected.

The variation of sheet carrier density is shown in Fig.3 for four different devices–Metal insulator semiconductor with heterostructure; Metal semiconductor with heterostructure; Metal insulator semiconductor without insulator; Metal semiconductor device without insulator to show the importance of insulator and conduction band discontinuity. Figure shows that threshold voltage for metal insulator semiconductor with and without heterojunction is –1.761V and -1.1V respectively i.e. introduction of insulator raises the threshold voltage by an amount $\frac{q.N_D.t_I.d_a}{\varepsilon_o.\varepsilon_I}$ while for devices without insulator these values changes to -0.696V and -0.036V i.e. introduction of heterojunction increases the threshold voltage by an amount $\Delta E_c - k_1$. The point at Which parallel conduction starts is the point where both densities equalize each other or no charges will transfer to the quantum well. Figure also shows that introduction of heterojunction or insulator in the device only lead to change in gate voltage swing and have no effect on maximum value of sheet carrier density or this will only going to effect the variation in sheet carrier density that can be used to improve device performance with different choice of the device.

The variation of potential (Δ) across the interface of two depletion regions with gate voltage for heterojunction metal semiconductor device with or without insulator is shown in Fig.4. More the potential, more the depletion width, lesser the free carriers available in high band gap semiconductor that can transfer to the quantum well and lesser will be the sheet carrier density. The gate voltage at which parallel conduction starts is the gate voltage at which Δ is equal to zero or conduction band in high band gap semiconductor crosses the Fermi level. For both the devices Δ decrease from the threshold point of the device and from the same value and reaches its minimum value at the parallel conduction point. This variation corresponds to the voltage drop across the insulator.

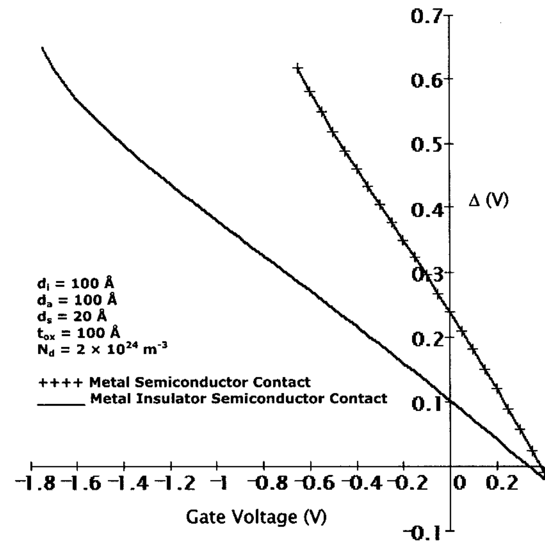

Fig. 4. Variation of potential where two structures coupled (Δ) with gate voltage for MISHEMT and HEMT.

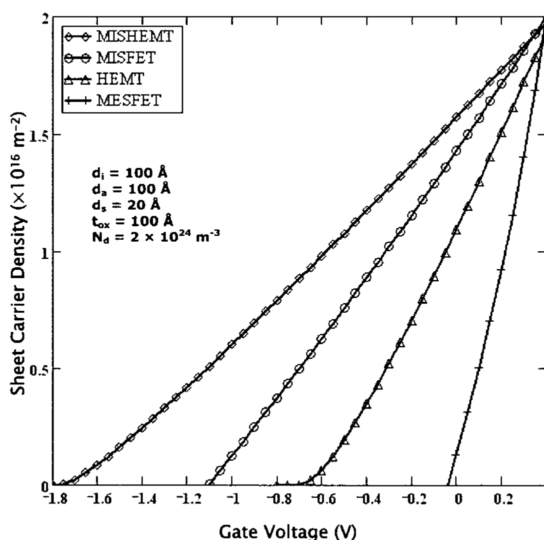

Fig. 3. Variation of sheet carrier density with gate voltage for MISHEMT, MISFET, HEMT and MESFET.

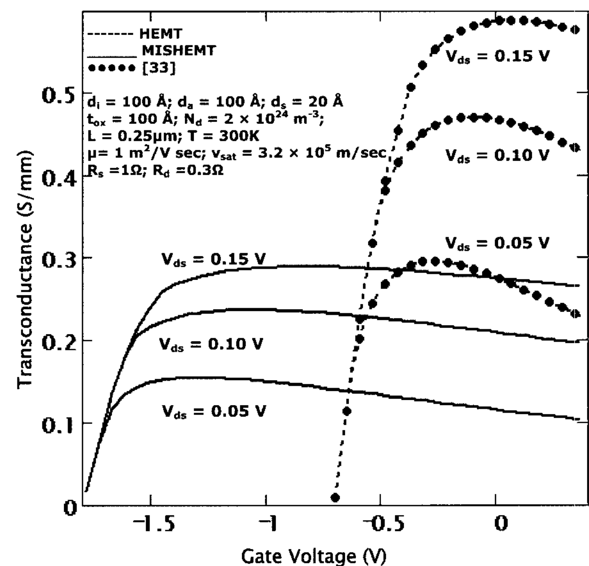

Fig. 5. Variation of Transconductance with gate voltage for MISHEMT and HEMT for different drain voltages.

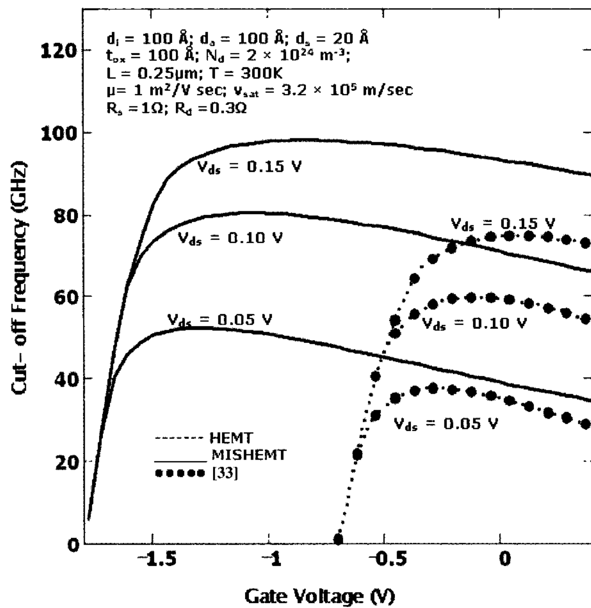

Fig. 6. Variation of Cut-off Frequency with gate voltage for MISHEMT and HEMT for different drain voltages.

To see the effect of insulator on the device characteristics, transconductance have been plotted in Fig.5 with gate voltage for HEMT device with or without insulator. Figure shows that HEMT with insulator although have half the value in comparison with HEMT without insulator but have almost constant variation of transconductance for large range of gate voltage which makes it useful for high performance amplifications. The corresponding values of cut-off frequency have been plotted in Fig.6. From the figure the maximum value of cut-off frequency obtained is 98GHz and 76GHz for MISHEMT and HEMT respectively.

VI. CONCLUSIONS

An analytical model has been proposed for predicting the characteristics of heterojunction MISFET (MISHEMT). The expression for sheet carrier density obtained from the analysis shows excellent agreement with previous models that proves the validity of our model. The comparison between characteristics and expressions of HEMT/MESFET/MISHEMT/MISFET shows that with the introduction of insulator between metal and semiconductor leads to increase in threshold voltage by an amount $\frac{q.N_D.t_I.d_a}{\varepsilon_o.\varepsilon_I}$ as a result of voltage drop across the insulator, while introduction of heterojunction leads to increase in threshold voltage by an amount $\Delta E_c - k_1$ for almost the same value of parallel conduction voltage. This will lead to larger gate voltage swing that makes it suitable for large signal amplifications. The comparison of transconductance shows that HEMT with insulator although have half the value in comparison with HEMT but have almost constant variation for large range of gate voltage which makes it suitable for high performance amplifiers. Same characteristics can be achieved with perfect insulator MISHEMT (MISFET) as with the LT-MISHEMT (MISFET) by choosing the thickness of perfect insulator to be $\varepsilon_I/\varepsilon_S$ times the thickness of LT-layer.

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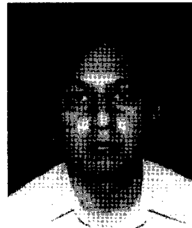

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