Analytical Thermal Noise Model of Deep-submicron MOSFETs

Hyungcheol Shin, Seyoung Kim, and Jongwook Jeon

Abstract—**This paper presents an analytical noise model for the drain thermal noise, the induced gate noise, and their correlation coefficient in deep-submicron MOSFETs, which is valid in both linear region and saturation region. The impedance field method was used to calculate the external drain thermal noise current. The effect of channel length modulation was included in the analytical equation. The noise behavior of MOSFETs with decreasing channel length was successfully predicted from our model.**

Index Terms—**RF CMOS, drain thermal noise, induced gate noise, velocity saturation effect, impedance field method**

I. INTRODUCTION

The continuous and aggressive down-scaling of the CMOS devices has made them enter into the field of RF applications [1-2]. Accurate modeling of RF CMOS is very important in optimizing circuit performance and reducing development time. Especially in RF frequencies, thermal noise has been found to be the dominant noise source. While the channel thermal noise of MOSFETs agree with the Van der Ziel model for long-channel devices [3], it have been reported that the thermal noise generated in short-channel MOSFETs is higher than predicted by the long-channel model [4].

Recently, for the drain thermal noise current, we showed that the simple well-known $\mu Q_{inv}/L^2$ formula, previously derived for long channels, remained valid even for devices with short channel [5]. In addition, the induced gate noise model and the correlation coefficient in short-channel MOSFETs also were developed and applied on LNA design [6]. However the previous induced gate noise model could be applied on the saturation regime only. In order to exploit the noise model more efficiently, an extended noise model which can cover entire device operation region of linear region and saturation region is required.

In this work, an extended noise model was developed. The new model covers both the linear and the saturation regime. The analytical expressions for drain thermal noise and induced gate noise currents are derived by using the impedance field method [5]. The modulated channel length due to drain bias was directly extracted from DC-measurements [7]. The noise model was verified with noise measurements for various devices with different channel lengths.

II. ANALYTICAL MODEL OF THERMAL NOISE OF MOSFETS

For a short-channel MOSFET with velocity saturation effect, the drain thermal noise current can be derived in integral form using the impedance field method as follows [8],

$$\left\langle i_{dn}^{\,2}\right\rangle = \frac{4kT_0\Delta f}{I_{DS}L_{elec}^{\,2}\left(1+\frac{V_{ds}}{L_{elec}E_c}\right)^2}\int_0^{V_{ds}} g_0^{\,2}(V)\left(1+\frac{E}{E_c}\right)dV \cdot \quad (1)$$

where $g_0(V)=\mu Wqn_{inv}=\mu WC_{ox}(V_{GT}-V)$ is channel conductance for unit length, C_{ox} is the gate oxide

Manuscript received Nov. 20, 2005; revised Aug. 2, 2006.
School of Electrical Engineering, Seoul National University, San 56-1, Shinlim-dong, Kwanak-gu, Seoul 151-742, Korea
E-mail : hcshin@snu.ac.kr

capacitance per unit area, V_{GT} is the gate overdrive voltage (V_{GS}-V_{TH}), E is the electric field, E_c is the critical electric field, and L_{elec} is the electrical channel length. The integral in (1) could be evaluated with applied bias analytically with the information of electric field E as a function of x [7]. Then the drain thermal noise power spectral density $<i_{dn}^2>$ can be rewritten as

$$\left\langle i_{dn}^{\ 2}\right\rangle = 4kT_0\Delta f G_{d0}\gamma \tag{2}$$

where

$$\gamma = \frac{L_{eff}}{L_{elec}}\left(\frac{1-u+\frac{1}{3}u^2}{(1-u/2)(1+z)}+\frac{z}{1+z}(1-u/2)\right) \tag{3}$$

where $G_{d0}=(\mu_{eff}WC_{ox}V_{GT}/L_{eff})$ is the intrinsic drain conductance at $V_{DS}=0$ V, $u=\alpha V_{DS}/V_{GT}$, $z=V_{DS}/V_L$,$V_L=L_{elec}E_C$, and $V_{GT}=V_G-V_T$. L_{elec} is the electrical channel length and can be obtained as [7]

$$L_{elec} = \frac{V_{GT}(V_{GT}-V')}{\alpha E_C V'} \tag{4}$$

where $V'= I_{DS} / WC_{ox}v_{sat}$, which can be extracted from the dc measurement.

The drain current noise Δi_{dn} causes a local channel voltage fluctuations Δv, which causes so-called induced gate noise. According to the procedure in [5], we can obtain the equation for Δv with neglecting the second-order terms in Δv as

$$\frac{d}{dx}[(g_0(V)-\frac{I_d}{E_c})\Delta v] = \Delta i_{dn}(1+\frac{dV}{dx}/E_c) \tag{5}$$

if we take the positive gate current direction as going into the device, the induced gate noise generated from Δv is found by solving (5) in terms of Δv and substituting it into

$$\Delta i_{gn} = -j\omega WC_{ox}\int_0^{L_{elec}}\Delta v dx \tag{6}$$

after some algebraic steps, the analytic expression for the induced gate noise spectral density can be written

$$\left\langle i_{gn}^{\ 2}\right\rangle = \sum\left\langle \Delta i_{gn}\right\rangle^2 \tag{7}$$
$$= 4kT_0\Delta f\frac{(W\omega C_{ox})^2}{I_d^{\ 3}}\int_0^{V_{ds}} g_0^{\ 2}(1+E/E_c)(V_{as}-V)^2 dV$$

where

$$V_{as} \equiv V_{ds} - \frac{V_{ds}}{2}\frac{V_{GT}-\alpha V_{ds}/3}{V_{GT}-\alpha V_{ds}/2} \tag{8}$$

the integral in (7) can be evaluated and the PSD is given by

$$\left\langle i_{gn}^2\right\rangle = 4kT_0\Delta f\frac{(\frac{2}{3}\omega C_{ox}WL_{elec})^2}{5G_{d0}}\beta \tag{9}$$

where

$$\beta = \frac{L_{elec}}{L_{eff}}\cdot\frac{2(45-90u+63u^2-18u^3+2u^4)}{3(2-u)^5}(1+z)^4 \tag{10}$$

the above equation (10) can be used in linear region as well as saturation region. In the similar manner, the correlation between the induced gate noise and the drain thermal noise can be derived as

$$\left\langle i_{gn}i_{dn}^{\ *}\right\rangle = 4kT_0\Delta f(j\frac{2}{3}\omega WL_{elec}C_{ox})\frac{u(6-6u+u^2)}{6(2-u)^3}(1+z)^2 \tag{11}$$

and the correlation coefficient C can be calculated using the above results as

$$C = \frac{<i_{gn}i_{dn}^*>}{\sqrt{<i_{gn}^2><i_{dn}^2>}} = j\frac{\frac{u(6-6u+u^2)}{6(2-u)^3}(1+z)^2}{\sqrt{\frac{\gamma\beta}{5}}} \tag{12}$$

III. EXPERIMEMTAL RESULTS AND DISCUSSIONS

The test devices were fabricated by 0.18 μm CMOS technology and have multi-fingered structure. The unit finger width and the number of finger were fixed to 5

μm and 16, respectively. Device model parameters were extracted from DC-measurements as well as S-parameter measurements. The high frequency device noise was measured on-wafer with a noise figure analyzer and electrical tuner. The drain thermal noise and the induced gate noise for various channel length including the linear regime are depicted in Fig. 1 and Fig. 2, and shows excellent agreement with the measurement. The modeled correlation coefficients are compared with the measurement in Fig. 3. As the channel length decreases, the correlation coefficient of the MOSFETs is getting smaller than the long channel value of 0.395. From the above results, it is verified that this analytical model predicts the bias dependency of each noise current of the test devices from long channel to deep-submicron MOSFETs accurately. With the model, noise factors versus various channel length can be predicted as shown in Fig. 4. When the channel length is 0.18 μm, γ is increased to about 1, β is increased to about 4 and C is decreased to about 0.25.

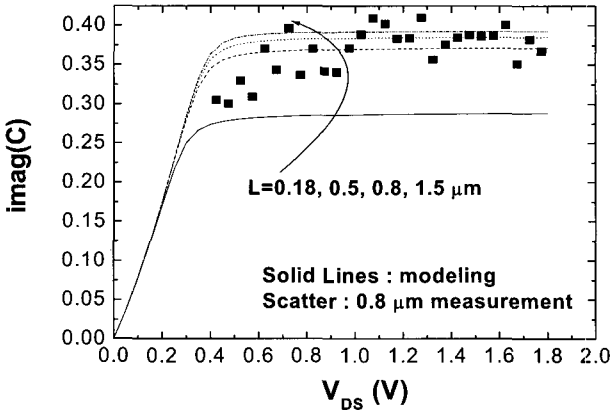

Fig. 3. Correlation coefficients versus V_{DS}. Long channel devices are measured and compared. It is shown that the data agree with those predicted in the long channel theory j0.395.

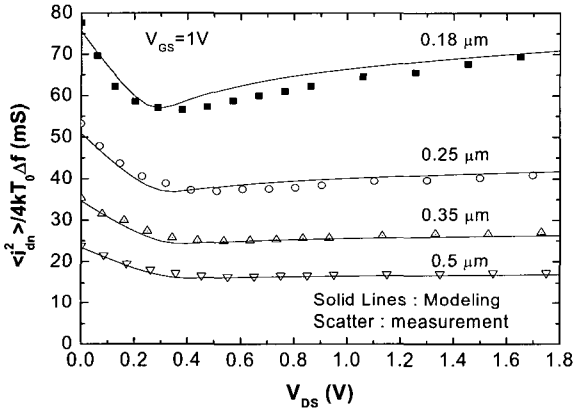

Fig. 1. Drain thermal noise with different channel lengths versus V_{DS}. Symbols and lines are the measured and modeled data, respectively.

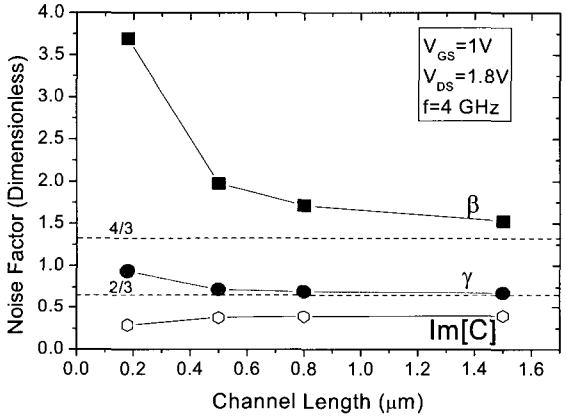

Fig. 4. Gate length dependence of noise parameters predicted by the proposed model.

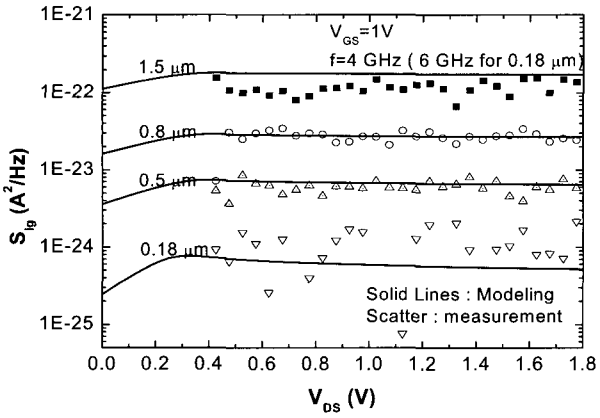

Fig. 2. Induced gate thermal noise with different channel lengths versus V_{DS}. Symbols and lines are the measured and modeled data, respectively.

IV. CONCLUSIONS

In this paper, simple analytical expressions for the drain thermal noise, the induced gate noise, and the correlation coefficient of MOSFETs which are valid in both linear and saturation regions have been presented. Thermal noise in the test devices including long channel and deep-submicron MOSFETs were fabricated and measured. The validity of the model was demonstrated by agreement with noise measurements. The derived models can be implemented in circuit simulators for RF circuit design and are very helpful in predicting circuit noise performance.

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REFERENCES

[1] M. Je, I. Kwon, H. Shin, and K. Lee, "MOSFET modeling and parameter extraction for RF-ICs," in CMOS RF Modeling, Chanracterization and Applications. Singapore: World Scientific, pp. 67-120, 2002.

[2] E. Morifuji, H. S. Momose, T. Ohguro, T. Yoshitomi, and H. Kimijima, "Future perspective and scaling down roadmap for RF CMOS," Symp VLSI Technology, pp. 163-164, 1999.

[3] A. Van Der Ziel, Noise in Solid State Devices and Circuits, New York: Wiley, 1986.

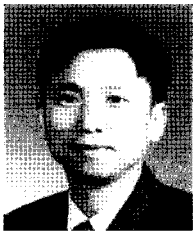
[4] M. Miura-Mattausch, H. J. Mattausch, T. Ohguro, T. Iizuka, M. Taguchi, S. Kumashiro, and S. Miyamoto, "MOSFET Model HiSIM Based on Surface-Potential Description for Enabling Accurate RF-CMOS Design," Journal of Semiconductor Tech. and Science(JSTS), vol. 4, pp.133-140, Sep. 2004.

[5] K. Han, H. Shin, and K. Lee, "Analytical Drain Thermal Noise Current Model Valid for Deep Submicron MOSFETs," IEEE Trans. Electron Devices, vol. 51, pp. 261-269, Feb. 2004.

[6] K. Han, J. Gil, S. Song, J. Han, and H. Shin, "Complete High frequency Thermal Noise Modeling of Short-Channel MOSFETs and Design of 5.2-GHz Low Noise Amplifier," IEEE J. Solid-State Circuits, vol. 40, no. 3, pp. 726-735, Mar. 2005.

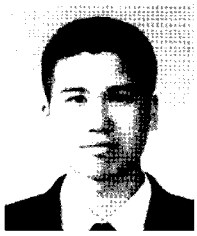
[7] S. Asgaran, M. J. Deen, and C. H. Chen, "Analytical Modeling of MOSFETs Channel Noise and Noise Parameters," IEEE Trans. Electron Devices, vol. 51, pp. 2109-2114, Dec. 2004.

[8] J. Jeon, S. Kim, I. Kang, K. Han, K. Lee, and H. Shin, "Analytical Thermal Noise Modeling Suitable for Circuit Design Using Short-Channel MOSFETs", IEEE Radio Frequency Integrated Circuits(RFIC2005) Symposium, pp. 637-640, June 2005.



Hyungcheol Shin received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1985 and 1987, respectively, and Ph.D. degree in electrical engineering from the University of California, Berkeley, in 1993. From 1994 to 1996, he was with Motorola Advanced Custom Technologies as a Senior Device Engineer. In 1996, he joined the Department of Electrical Engineering and Computer Sciences, KAIST, Taejon, in 1996 as an Assistant Professor. During his sabbatical leave from 2001 to 2002, he was with Berkana Wireless as a Staff Scientist in charge of CMOS RF modeling. In 2003, he joined the school of Electrical Engineering and Computer Science, Seoul National University, as an Associate Professor. His current research interests include RF circuit, CMOS RF modeling, CIS, and nanoscale CMOS. Dr. Shin has served as a committee member of several international conferences, including the IEEE Electron Devices Meeting. He is a Lifetime Member of the Institute of Electronics Engineering of Korea(IEEK).

Seyoung Kim received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 2003 and 2005, respectively. Since 2005, he has been with Samsung Electronics company, Ltd., Kyungki-Do, Korea. His current research interests are CMOS RF modeling and electrostatic discharge (ESD) devices.



Jongwook Jeon was born in Ma-San, Korea, on July 7, 1981. He received the B.S. degree in school of information and communication engineering from the Sungkyunkwan University, Suwon, Korea, in 2004, and he is currently working toward the Ph.D. degree in electrical engineering at Seoul National University. His current research interests are RF CMOS noise modeling and circuit design.