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A New High Efficiency Half Bridge Converter with Improved ZVS Performance

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ABSTRACT

A new asymmetrical pulse width modulation (PWM) half bridge converter with improved ZVS performance is proposed. The ZVS operation of the proposed converter can be maintained from no load to full load conditions since the magnetizing current of the transformer contributes to the ZVS operation at light loads without considerable conduction loss of the transformer and switch. Synchronous rectification is employed to reduce the rectification loss. Operational principles, large signal modeling, ZVS analysis and design equations are presented. Experimental results demonstrate that the proposed converter can achieve a large ZVS range and significant improvement in efficiency for a 100W (5V, 20A) prototype converter.

Keywords: DC/DC power conversion, pulse width modulation, power supplies, power distribution

1. Introduction

In general, the hard switching operation of the power switch results in high switching loss, high EMI noise and high switch voltage stress. Therefore, many soft switching DC/DC converters have been proposed to achieve high efficiency and high power density. Among them, active clamp flyback converters[1] and active clamp forward converters[2] are attractive due to their simple structure and good ZVS performance. However, since the sum of the input voltage and transformer primary voltage is applied to their power switches, they suffer from high voltage stress. Therefore, asymmetrical half bridge converters [3-6], which can achieve ZVS operation of power switches as well as low switch voltage stresses, are gaining popularity. However, since these converters lose their ZVS condition at light loads, they suffer from low efficiency and high EMI noise as the load decreases. The simplest technique to achieve ZVS operation even at the light loads is to increase the magnetizing current by reducing the magnetizing inductance[7]. However, the large current, which is the sum of the magnetizing current and reflected load current, causes serious conduction losses in the transformer and power switch. The asymmetrical half bridge flyback converter can achieve the ZVS operation from no load to full load conditions[8]. However, the secondary diode current has large ripple and large peak values.

To overcome these drawbacks, a new asymmetrical half bridge forward converter with a flyback type transformer is proposed. It is easy to achieve the ZVS operation of

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power switches from no load to full load conditions since the magnetizing current of the transformer contributes to the ZVS operation at light loads. This results in high efficiency and considerably reduced EMI noise levels throughout all load conditions. Since the secondary diode current is the same as that of conventional forward converters, it shows reduced current stress. In addition, it is recommended that the Schottky diodes are replaced by power MOSFETs used as synchronous rectifiers in order to improve the overall system efficiency.

The operational principles, large signal modeling, ZVS analysis, design equations and experimental results are presented to confirm the validity of the proposed converter.

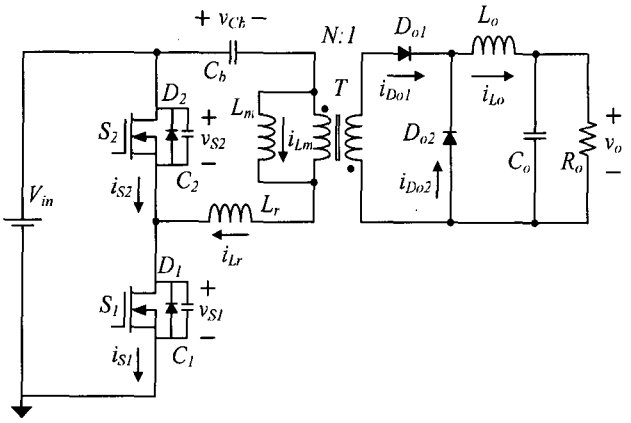


Fig. 1 Schematic of the proposed converter

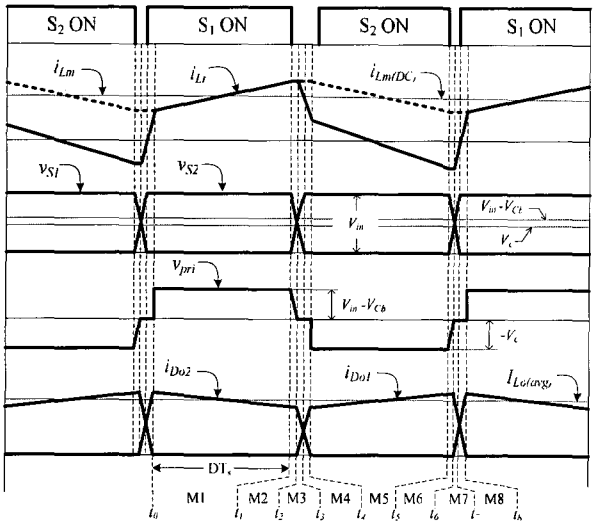


Fig. 2 Key waveforms for the mode analysis

2. Operational Principles

Fig. 1 shows the circuit diagram of the proposed converter. Its primary and secondary sides are similar to those of the conventional half bridge and forward converters, respectively. However, the polarity of the transformer is reversed like that of the flyback converter.

Fig. 2 shows the operating waveforms of the proposed converter in a the steady state. Each switching period is subdivided into eight modes and their topological stages are shown in Fig. 3. In order to illustrate a steady state operation, several assumptions are made as follows:

(a) S_1 and S_2 are ideal except for their capacitors C_1=C_2=C_s and internal diode.
(b) The blocking capacitor voltage V_{Cb} is assumed to be a constant.
(c) The output voltage V_o is assumed to be a constant.
(d) The transformer magnetizing current $i_{Lm}(t)$ is assumed to be constant during the time interval t_1~t_2 and t_5~t_6.

Mode 1(t_0~t_1): Mode 1 begins when the commutation of secondary diode currents, $i_{Do1}(t)$ and $i_{Do2}(t)$, is completed. Then diode D_{o1} and D_{o2} are reverse and forward biased respectively. Since S_1 is on and S_2 is in off state, voltage V_{in}-V_{Cb} is applied to magnetizing inductor L_m and leakage inductor L_r. The currents flowing in L_m and L_r can be expressed as follows:

$$i_{Lm}(t)=\frac{V_{in}-V_{Cb}}{L_m+L_r}t+i_{Lm}(t_o)=i_{Lr}(t)=i_{S1}(t) \quad (1)$$

$$i_{Lo}(t)=\frac{V_o}{L_o}t+i_{Lo}(t_0)=i_{Do2}(t)\simeq i_{Lo(avg)} \quad (2)$$

where

$$i_{Lm}(t_o)=\frac{i_{Lo(avg)}}{n}(1-D)-\frac{V_{in}-V_{Cb}}{2(L_m+L_r)}DT_s$$

Because of the different form of the conventional asymmetrical half bridge converter, the load current of the proposed converter does not reflect to the primary switch. Therefore, the conduction loss of the transformer and power switch can be considerably reduced in this mode.

Mode 2(t_1~t_2): When S_1 is turned off, this mode begins. Since $v_{S2}(t)$ is higher than V_{Cb}, the dotted end of the transformer is positive with respect to undotted end and diode D_{o1} is still reversely biased. Therefore, the output capacitors of S_1 and S_2 are charged and discharged respectively by magnetizing current $i_{Lm}(t)$. $v_{S1}(t)$ can be expressed with the assumption (4) as follows:

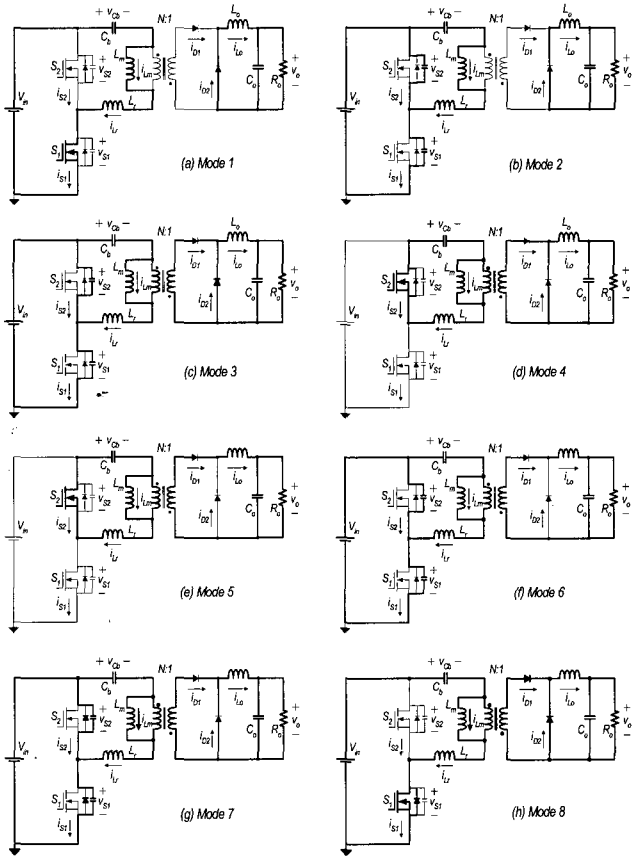


Fig. 3 Equivalent circuit of the proposed converter

$$v_{S1}(t)=\frac{i_{Lm}(t_1)}{2C_s}t \tag{3}$$

where

$$i_{Lm}(t_1)=\frac{i_{Lo(avg)}}{n}(1-D)+\frac{V_{in}-V_{Cb}}{2(L_m+L_r)}DT_s$$

Mode 2 ends at time t_2 when $v_{S1}(t)$ increases to V_{in}-V_{Cb}.

Mode 3(t_2~t_3): After $v_{S1}(t)$ increase to V_{in}-V_{Cb}, the output inductor current $i_{Lo}(t)$ begins to freewheel through output diode D_{o1} and D_{o2}. Since the primary voltage of the transformer is zero, $v_{S1}(t)$ is charged as a resonant manner of L_r and C_s. $i_{Lr}(t)$ and $v_{S1}(t)$ can be expressed as follows:

$$i_{Lr}(t)=i_{Lm}(t_2)\cdot\cos\left(\sqrt{\frac{1}{2L_rC_s}}t\right) \tag{4}$$

$$v_{S1}(t)=\sqrt{\frac{L_r}{2C_s}}\cdot i_{Lm}(t_2)\cdot\sin\left(\sqrt{\frac{1}{2L_rC_s}}t\right)+(V_{in}-V_{Cb}) \tag{5}$$

After $v_{S1}(t)$ and $v_{S2}(t)$ reach V_{in} and 0V, respectively, $i_{Lr}(t)$ flows through the diode D_2 and zero voltage across S_2 is maintained. Therefore, switch S_2 can be turned on with ZVS condition at the next mode.

Mode 4(t_3~t_4): When S_2 is turned on, this mode begins. As can be seen in Fig. 3(c), $i_{Lr}(t)$ flows through diode D_2 of switch S_2 at t_3. Thus, S_2 can be turned on with ZVS condition. A detailed analysis of the ZVS operation with load variations is described in the next section. Since D_{o1} and D_{o2} are still conducting with S_2, the voltage across the transformer is 0V and -V_{Cb} is applied to the leakage inductor. Therefore, the leakage inductor current linearly decreases as follows:

$$i_{Lr}(t)=-\frac{V_{Cb}}{L_r}t+i_{Lr}(t_3) \tag{6}$$

where

$$i_{Lr}(t_3)=\sqrt{i_{Lm}^2(t_2)-\frac{2C_sV_{Cb}^2}{L_r}}$$

which can be derived from equation (4) and (5).

Mode 4 ends at time t_4 when $i_{Lr}(t)$ reaches $i_{Lm}(t)$-$i_{Lo}(t)$/n.

Mode 5(t_4~t_5): When $i_{Lr}(t)$ reaches $i_{Lm}(t)$-$i_{Lo}(t)$/n, output inductor current completes its freewheeling and diode D_{o1} and D_{o2} are positively and negatively biased, respectively. V_{Cb} is applied to L_m+L_r and V_{Cb}/n-V_o is applied to L_o. $i_{Lm}(t)$, $i_{Lo}(t)$ and $i_{Lr}(t)$ can be expressed as follows:

$$i_{Lm}(t)=-\frac{V_{Cb}}{L_m-L_r}t+i_{Lm}(t_4) \tag{7}$$

$$i_{Lo}(t)=\frac{\frac{V_{Cb}}{n}-V_o}{L_o}t+i_{Lo}(t_4)=i_{Do1}(t)\simeq i_{Lo(avg)} \tag{8}$$

$$i_{Lr}(t)=i_{Lm}(t)-\frac{i_{Lo}(t)}{n}. \tag{9}$$

Mode 5 ends at the time t_5 when switch S_2 is turned off.

Mode 6 (t_5~t_6): The operation of this mode is similar to that of mode 2. During $v_{S2}(t)$ is less than V_{Cb}, the

output capacitor of S_2 is charged rapidly by $i_{Lo}(t)/n$-$i_{Lm}(t)$. When $v_{s2}(t) \le V_{Cb}$, $v_{S2}(t)$ can be expressed as follows:

$$v_{S2}(t) = \frac{\frac{i_{Lo}(t_5)}{n} - i_{Lm}(t_5)}{2C_s} t . \quad (10)$$

Mode 6 ends at the time t_6 when $v_{S2}(t)$ reaches to V_{Cb}.

Mode 7 (t_6~t_7) : The operation of this mode is similar to that of mode 3. After $v_{S2}(t)$ increases over V_{Cb}, $i_{Lr}(t)$ starts to increase in a resonant manner of L_r and C_s. When $v_{s2}(t) \ge V_{Cb}$, $i_{Lr}(t)$ and $v_{S2}(t)$ can be expressed as follows:

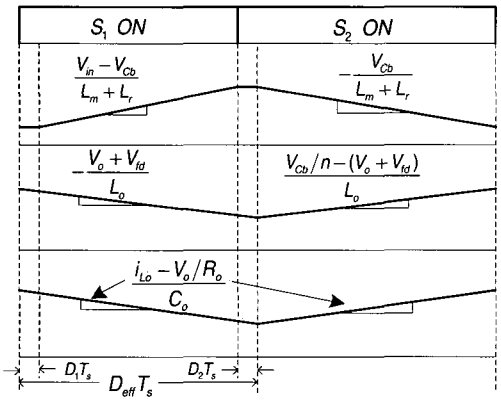


Fig. 4 The Waveforms of the state variables for the large signal analysis

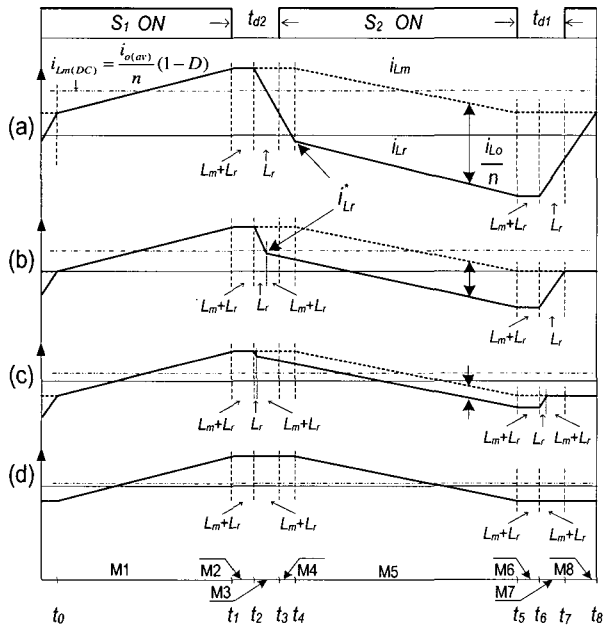


Fig. 5 Magnetizing and leakage inductor current for ZVS analysis with the load variation

$$i_{Lr}(t) \doteq \left(i_{Lm}(t_6) - \frac{i_{Lo}(t_6)}{n} \right) \cdot \cos\left(\sqrt{\frac{1}{2L_rC_s}}\, t \right) \quad (11)$$

$$v_{S2}(t) = \sqrt{\frac{L_r}{2C_s}} \left(\frac{i_{Lo}(t_6)}{n} - i_{Lm}(t_6) \right) \cdot \sin\left(\sqrt{\frac{1}{2L_rC_s}}\, t \right) + V_{Cb} \quad (12)$$

After $v_{S1}(t)$ and $v_{S2}(t)$ reach 0V and V_{in}, respectively, $i_{Lr}(t)$ flows through the diode D_1 and the zero voltage across S_1 is maintained.

Mode 8 (t_7~t_8): When S_1 is turned on, this mode begins As can be seen in Fig. 3(g) $i_{Lr}(t)$ flows through the diode D_1 of switch S_1 at t_7. Thus, S_1 can be turned on with ZVS condition. Since D_{o1} and D_{o2} are still conducting with S_1, the voltage across the transformer is 0V and V_{in}-V_{Cb} is applied to the leakage inductor. Therefore, the leakage inductor current linearly increases as follows:

$$i_{Lr}(t) = \frac{V_{in} - V_{Cb}}{L_r} t + i_{Lr}(t_7) \quad (13)$$

where

$$i_{Lr}(t_7) = \sqrt{\left(i_{Lm}(t_0) - \frac{i_{Lo(avg)}}{n} \right)^2 + \frac{2C_s(V_{in} - V_{Cb})^2}{L_r}}$$

Mode 8 ends at time t_8 when $i_{Lr}(t)$ reaches $i_{Lm}(t)$. After the end of mode 8, one switching period is completed and the operation is repeated.

3. Analysis of the Proposed Converter

In this section, large signal modeling and ZVS operation with load conditions are accomplished.

3.1 Large signal modeling:

Large signal modeling can be obtained by averaging the currents and voltages over one switching cycle. The state variables are the magnetizing current $i_{Lm}(t)$, output inductor current $i_{Lo}(t)$ and output voltage $V_o(t)$. The slope of the state variables and the freewheeling times of the output current, D_1T_s and D_2T_s, are depicted in Fig. 4. The resulting large signal equations can be obtained as follows:

$$\frac{di_{Lm}(t)}{dt} = \frac{V_{in} - V_{Cb}}{L_m + L_r} D_{eff} - \frac{V_{Cb}}{L_m + L_r} \left(1 - D_{eff} - D_1 - D_2 \right) \quad (14)$$

$$\frac{di_{Lo}(t)}{dt} = -\frac{V_o(t)-V_{fd}}{L_o}\left(D_{eff}+D_1+D_2\right) + \frac{\frac{V_{Cb}}{n}-\left(V_o(t)+V_{fd}\right)}{L_o}\left(1-D_{eff}-D_1-D_2\right) \quad (15)$$

$$\frac{dV_o(t)}{dt} = \frac{i_{Lo}-\frac{V_o(t)}{R_o}}{L_o} \quad (16)$$

where V_{fd} is the forward voltage drop of secondary diode. From equations (14) and (15), the voltage transfer ration of the proposed converter can be derived as follows:

$$V_o = \frac{V_{in}}{n}\frac{D_{eff}}{1-D_1-D_2}\left(1-D_{eff}-D_1-D_2\right)-V_{fd} \quad (17)$$

3.2 ZVS analysis with load conditions:

The ZVS operation of the power switch in the proposed converter is maintained from no load to full load conditions. The reasons are described below according to the different load conditions: a heavy load, light load and no load. Fig. 5 shows the magnetizing current $i_{Lm}(t)$ and leakage inductor current $i_{Lr}(t)$ under the different load conditions.

(a) Heavy load condition: The DC offset of magnetizing current $i_{Lm(DC)}$ can be derived using the current-second balance of blocking capacitor C_b and can be expressed as follows:

$$i_{Lm(DC)} = \frac{i_{Lo(av)}}{n}(1-D) \quad (18)$$

It is noted in Fig. 5(a) that since $i_{Lm}(t)$ swings along a positive DC offset and $i_{Lr}(t)$ flows in the negative direction when it reaches i^*_{Lr}, ZVS operation is the same as the mode analysis. That is when $v_{S2}(t)\geq V_{Cb}$ the output capacitor of S_2 is discharged by the energy stored in L_m+L_r and when $v_{S2}(t)\leq V_{Cb}$ it is discharged to a zero voltage by the energy stored in L_r. Since $L_m \gg L_r$, $v_{S2}(t)$ can be easily discharged to V_{Cb}. Therefore the ZVS condition of S_2 and S_1 can be expressed respectively as follows:

$$\frac{1}{2}L_r i_{Lr}^2(t_2) \geq 2\cdot\frac{1}{2}C_s V_{Cb}^2 \quad (19)$$

$$\frac{1}{2}L_r\left(\frac{i_{Lo}}{n}-i_{Lm}(t_6)\right)^2 \geq 2\cdot\frac{1}{2}C_s\left(V_{in}-V_{Cb}\right)^2 \quad (20)$$

(b) Light load condition: As the load current decreases, iLr(t) is changed from a negative value to a positive value when it reaches i*Lr. Fig. 5(b) shows that vS2(t) is discharged by the energy stored in Lm+Lr when vS2(t)≥VCb and discharged by the energy stored in Lr until iLr(t) reaches i*Lr. in light loads, iLm(t)>iLo(t)/n when iLr(t)=i*Lr, iLr(t) still flows in a positive direction. Therefore vS2(t) is further discharged to zero voltage by the energy stored in Lm+Lr. The time interval Δt_α where S2 is discharged only by the energy stored in Lr is derived from equation (4) and can be expressed as follows:

$$\Delta t_\alpha = \sqrt{2L_rC_s}\cdot\cos^{-1}\left(\frac{i_{Lm}(t_2)-\frac{i_{Lo(avg)}}{n}}{i_{Lm}(t_2)}\right) \quad (21)$$

Switch S_1 is a boundary situation in Fig 5(b). If the load current decreases further $i_{Lm(DC)}$ also goes down and finally $i_{Lm}(t)$ changes its polarities for some duration as shown in Fig. 5(c). Therefore, the output capacitor of S_1 is discharged by the energy stored in L_m+L_r when $v_{S1}\geq V_{in}-V_{Cb}$ and discharged by the energy stored in L_r until $i_{Lr}(t)$ reaches $i_{Lm}(t)$. Since $i_{Lm}(t)$ is a negative value at this time, it is further discharged to zero voltage by the energy stored in L_m+L_r. The time interval Δt_β where S_1 is discharged only by the energy stored in L_r is derived from equation (11) and can be expressed as follows:

$$\Delta t_\beta = \sqrt{2L_rC_s}\cdot\cos^{-1}\left(\frac{i_{Lo(avg)}}{n}\right) \quad (22)$$

When the magnetizing inductor plays a role in the ZVS operation, ZVS is easily achieved. Therefore the leakage inductor should be designed in the boundary situation of S_1 in Fig. 5(b) for ZVS operation over a whole load range.

(c) No load condition: Fig. 5(d) shows that output capacitors of S_2 and S_1 are discharged to a zero voltage only by the energy stored in L_m+L_r at a no load condition. Therefore ZVS operation is easily achieved.

4. Design Example

To validate the characteristics of the proposed converter a prototype converter was designed with the following specifications:

- Input voltage V_{in}, 400V DC
- Output voltage V_o, 5V
- Maximum output power $P_{o(max)}$, 100W
- Switching frequency f_s, 100kHz
- Maximum duty ratio of S_1, D_{max}, 0.45 at V_{in}=400V and P_o=100W

4.1 Selection of turn ratio, n

Since the Schottky diode has a large forward voltage drop V_{fb}, it is a well-known fact that synchronous rectifiers are used as output rectifiers instead of Schottky diodes. Assuming that the forward voltage drop caused by the turn-on resistance of synchronous rectifier in the secondary side is 0.05V (turn on resistance of IRF3703 is 2.8mΩ) and D_{eff}=0.45, the turn ratio of the transformer n can be derived from equation (17) and expressed as follows:

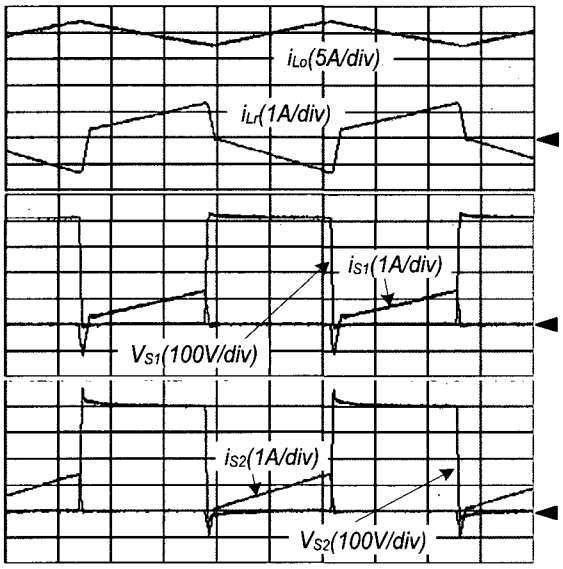


Fig. 6 Experimental key waveforms at full load

$$n=\frac{V_{in}}{(V_o+V_{fd})}\cdot\frac{D_{eff}}{1-D_1-D_2}(1-D_{eff}-D_1-D_2) \tag{23}$$

4.2 Selection of output inductance, Lo

L_o can be selected by determining the ripple current size of the output capacitor. When a continuous conduction mode (CCM) operation is desired until 10% of the full load, the ripple current of the output capacitor, Δi_{Co}, should be 4A. Then L_o can be obtained as follows:

$$L_o=\frac{V_o}{\Delta i_{Co}}DT_S \tag{24}$$

4.3 Selection of leakage inductance, Lr

As long as the ZVS operation is achieved, it is desirable that the leakage inductance of the smallest possible transformer should be selected since it reduces the effectiveness of the duty ratio. Since the ZVS operation can be easily achieved by the energy stored in L_m in a light load, leakage inductance should be selected in boundary load conditions of S_1 as shown in Fig. 5(b). Considering $i_{Lm}(t_6)$=0 in the boundary load condition of S_1 and V_{Cb}=DV_{in}, leakage inductance can be derived from equation (20) and expressed as follows:

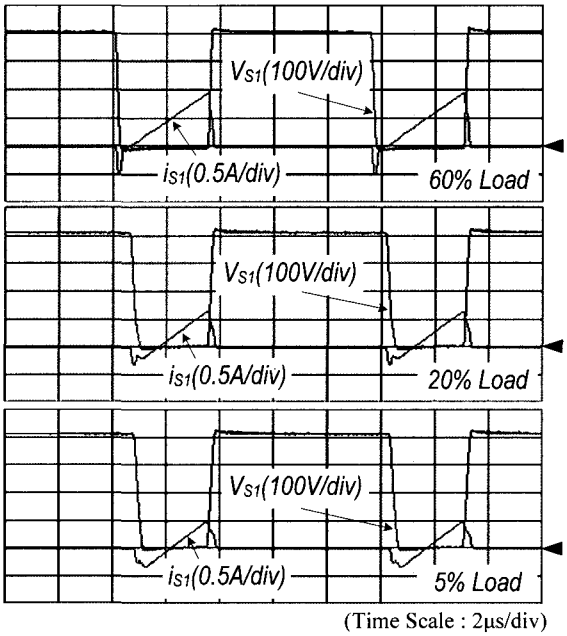
$$L_r>\frac{2n^2C_{oss}V_{in}^2(1-D)^2}{\left(i_{Lo}^{'}\right)^2} \tag{25}$$

where

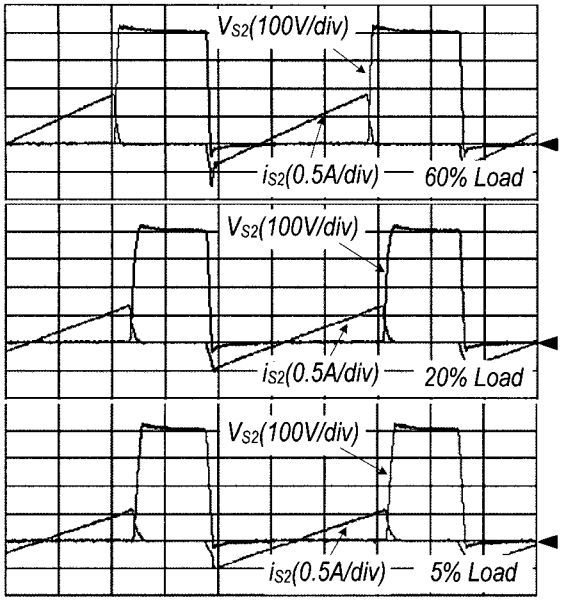
$$i_{Lo}^{'}=\frac{n}{1-D}i_{Lm(DC)(boundary)}$$

4.4 Selection of magnetizing inductance, Lm

Since L_r is chosen to guarantee ZVS operation until 60% of full load, the minimum of $i_{Lm}(t)$ should be zero at the boundary load condition to maintain ZVS operation from a no load to a full load condition. To satisfy this,



(a) ZVS operation of S_1



(b) ZVS operation of S_2

Fig. 7 Experimental ZVS waveforms with the load variation

$\Delta i_{Lm}(t)$ should be twice of $i_{Lm(DC)}$ at the boundary load condition as shown in Fig. 5(b). Considering $i_{Lo(avg)}$=12A at the boundary load condition, L_m can be derived from equation (1) and (18) and expressed as follows:

$$L_m = \frac{nV_{in}DT_s}{2i_{Lo(avg)}} \tag{26}$$

4.5 Selection of dead times between switching, td1, td2

As shown in Fig. 5, dead times, t_{d1} and t_{d2}, should be carefully designed because they affect the ZVS operation of the power switch. Since L_r and L_m were designed to guarantee the ZVS operation of the whole load range, dead times, t_{d1} and t_{d2}, should be longer than the discharging time of the output capacitors of the power switches. When we assume the boundary load conditions of switch S_1 and S_2 are 60% and 90% of the full load respectively, dead time t_{d1} and t_{d2} can be derived from equations (10), (25) and (3), (24) and can be expressed as follows:

$$t_{d1} \geq \frac{2C_sV_{Cb}}{\frac{i_{Lo(avg)}}{n} - i_{Lm}(t_0)} + \sqrt{2L_rC_s}\cdot\cos^{-1}\left(\frac{i_{Lo(avg)}}{n}\right) \tag{27}$$

$$t_{d2} \geq \frac{2C_s(V_{in}-V_{Cb})}{i_{Lm}(t_1)} + \sqrt{2L_rC_s}\cdot\cos^{-1}\left(\frac{i_{Lm}(t_2) - \frac{i_{Lo(avg)}}{n}}{i_{Lm}(t_2)}\right) \tag{28}$$

5. Experimental Results

Based on the designed parameters in the preceding section, a prototype of a 5V, 100W converter operated at 100kHz was built. The power stage consists of the following parameters: Switch S_1 and S_2: IRFP450A. Diode D_{o1} and D_{o2} (synchronous switch): IRF3703. Blocking capacitor C_b: 2.2μF. Output Capacitor C_o: 35V, 1000μF. Magnetizing Inductor L_m: 816μH. Leakage Inductor L_r: 24μH. Output Inductor L_o: 5.6μH. Transformer T: 28 turns of primary, 2 turns of secondary. Fig. 6 shows key waveforms of the proposed converter at full load condition. Output inductor current $i_{Lo}(t)$ and leakage inductor current $i_{Lr}(t)$ act in accordance with the theoretical analysis of Fig. 2. The ZVS operation of S_1 and S_2 is easily achieved at full load condition. Fig .7 shows the voltages and currents of switch S_1 and S_2 at different load conditions. It is noted that the ZVS operation of each switch is maintained from no load to full load condition. The efficiency of the converter is plotted in Fig. 8. A high efficiency of 85% along a wide load range can be obtained.

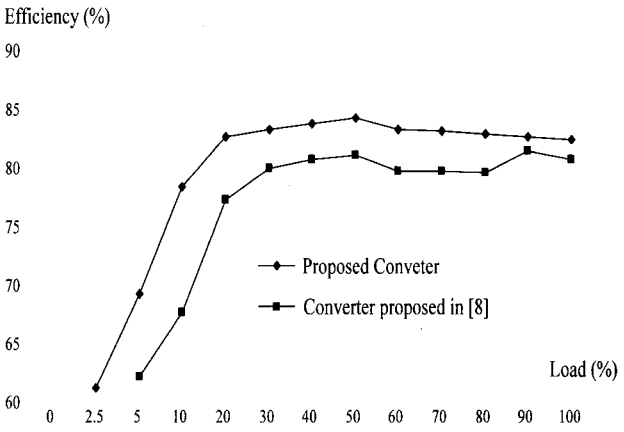


Fig. 8 Efficiency comparison with the load variations

6. Conclusions

This paper presented the analysis and experimental

results of a DC/DC converter with ZVS operations from a no load to a full load condition. ZVS operation can be easily achieved in heavy load conditions by employing a large leakage inductor current. Since the magnetizing inductor current of the transformer contributed to the ZVS operation of switches as the load decreased, the ZVS range of switches can be maintained from a no load to a full load condition. The operational principles were presented in the mode analysis, and the design equations were derived in large signal modeling and ZVS analysis. Based on the design equations, a prototype converter was optimally designed and tested in experiments. The experimental results of the 100W prototype converter prove the key characteristics of the proposed converter. The efficiency of the proposed converter obtained is about 85.5% over wide load ranges of 400V input.

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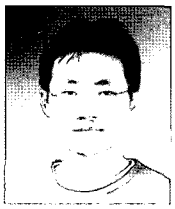

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