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A New High Efficiency ZVZCS Bidirectional DC/DC Converter for HEV 42V Power Systems

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ABSTRACT

A new high efficiency zero-voltage and zero-current switching (ZVZCS) bidirectional DC/DC converter is proposed in this paper. The proposed converter consists of two symmetric half-bridge cells as the input and output stages. MOSFETs of input stage are turned-on in ZVS condition, and those of output stage are turned-off in ZCS condition. In addition, MOSFETs of input and output stages have low voltage stresses clamped to input and output voltage, respectively. Therefore, the proposed converter has high efficiency and high power density. The operational principles are analyzed and the advantages of the proposed converter are described. The 300W prototype of the proposed converter is implemented for 42V hybrid electric vehicle (HEV) application in order to verify the operational principles and advantages.

Key Words: bidirectional DC/DC converter, zero-voltage switching (ZVS), zero-current switching (ZCS), hybrid electric vehicle (HEV)

1. Introduction

Until now, various electrical systems such as car audio system, air conditioning systems, and global positioning systems (GPS) have been used mainly in vehicles. In addition, new electrical technologies are applied to automotive applications, for example, electrical steering, braking, and suspension systems. Therefore, electrical power consumed in vehicles has greatly increased. In order to satisfy this large power consumption, the high voltage power system of 42V is essential in the manufacture of future vehicles. As the battery voltage of vehicles increases from 14V to 42V, the supply current of a battery decreases by one third. As a result, in 42V power systems, since electrical wires of motors and electrical systems decrease in thickness, it is expected that weight of vehicles decreases and fuel efficiency can be improved.

Recently, in order to reduce fuel energy consumption and to constrain environmental pollution by the exhaust gas, HEVs are proposed and investigated. HEVs use fuel and electrical energy of the battery in driving and regenerate electrical energy to the battery in braking. In HEVs, since electrical energy, supplied by the battery and regenerated to the battery, is largely increased, 42V power system must be adopted.

The energy storage system (ESS) of the 42V power system for HEVs, which stores and supplies electrical energy, is shown in Fig. 1. ESS has both a battery and super capacitor to supply high instant current [1,2]. Moreover, in ESS, the energy management system (EMS) observes the

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status of battery and super capacitor and controls electrical energy flow of the battery and super capacitor by the bidirectional DC/DC converter and switches, Q_B and Q_C [3,4].

A bidirectional DC/DC converter, Sepic converter and non-inverting Buck-Boost converter have been applied to the conventional ESS [4]. The Sepic converter, presented in Fig. 2 (a), has a non-inverting output voltage and minimized active components count. However, the main disadvantages are high voltage and current stresses of the active components and increased passive components count. Additionally, efficiency of this converter deteriorates by hard switching of active components. On the other hand, a non-inverting Buck-Boost converter, shown in Fig. 2 (b), has low voltage and current stresses and minimized passive components count. Nevertheless, this converter has many active components, which are turned-off in hard-switching conditions.

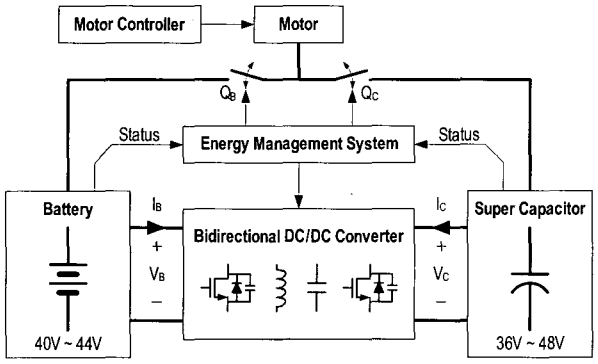


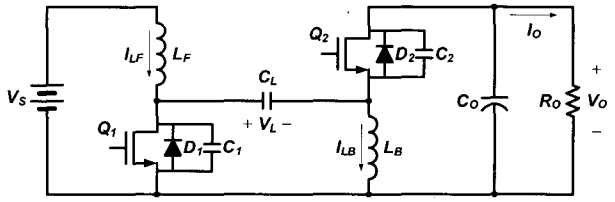
Fig. 1 ESS of 42V power system for HEVs

To overcome the disadvantages of these converters, a new high efficiency ZVZCS bidirectional DC/DC converter is proposed in this paper. The operational principles of the proposed converter are analyzed and verified by the experimental results using the 300W prototype for 42V power systems.

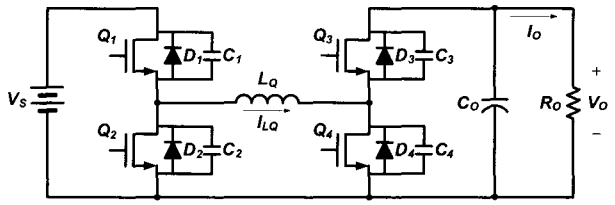
2. Operational Principles

2.1 Circuit configuration

As shown in Fig. 3, the proposed converter consists of two symmetrical half-bridge cells as the input and output stages. C_F and C_B are forward and backward half-bridge capacitor, respectively. Likewise, L_F and L_B are forward and backward series inductor, respectively. L_G is the dummy inductor to balance the voltages of C_F and C_B. The proposed converter has four MOSFETs, which are modeled as ideal unidirectional MOSFET, anti-parallel body diode, and parasitic output capacitor.



(a) Sepic converter



(b) Non-inverting Buck-Boost converter

Fig. 2 Conventional bidirectional DC/DC converters

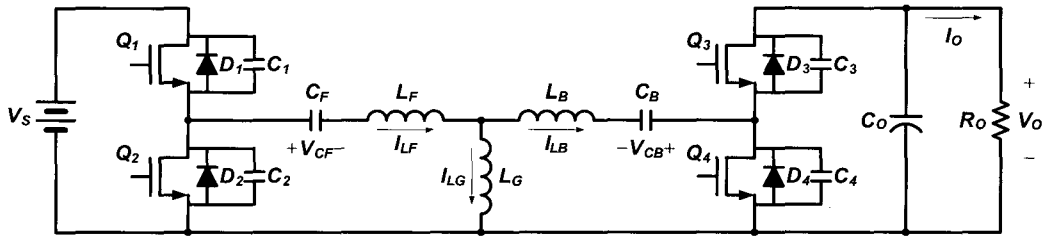


Fig. 3 Circuit diagram of the proposed converter

2.2 Modal analysis

The proposed converter operates in six modes according to the switching states of four MOSFETs, as shown in Fig. 4, and key waveforms are presented in Fig. 5. In addition, when L_G is sufficiently large, I_{LG} can be assumed zero and I_{LF} equals to I_{LB} in the modal analysis. Before t_0, I_{LF} flows through Q_2 and D_4.

Mode 1 (M_1, $t_0 \sim t_1$): When Q_2 is turned-off at t_0, mode 1 begins as shown in Fig. 4(a). I_{LF} discharges C_1 from V_S and charges C_2 from zero. When the voltage of C_1 reaches zero, I_{LF} flows through D_1 and D_4, and then it is increased with the steep slope given by

$$(d/dt)I_{L_F} = (V_S - V_{C_F} + V_{C_B})/(L_F + L_B) \quad (1)$$

Mode 2 (M_2, $t_1 \sim t_2$): When Q_1 is turned-on in ZVS condition and I_{LF} is increased to zero, mode 2 begins and D_4 is turned-off in ZCS condition at t_1, as shown in Fig. 4(b). I_{LF} flows through Q_1 and C_3, and I_{LF} is abruptly increased and C_3 rapidly discharges by resonance.

Mode 3 (M_3, $t_2 \sim t_3$): When C_3 is fully discharged to zero, mode 3 begins and D_3 is turned-on at t_2, as shown in Fig. 4(c). I_{LF} flows through Q_1 and D_3, and it is linearly increased with the slope given by

$$(d/dt)I_{L_F} = (V_S - V_{C_F} + V_{C_B} - V_O)/(L_F + L_B) \quad (2)$$

Mode 4 (M_4, $t_3 \sim t_4$): When Q_1 is turned-off at t_3, mode 4 begins as shown in Fig. 4(d). I_{LF} charges C_1 from zero and discharges C_2 from V_S. When the voltage of C_2 reaches zero, I_{LF} flows through D_2 and D_3, and then it decreases with the steep slope given by

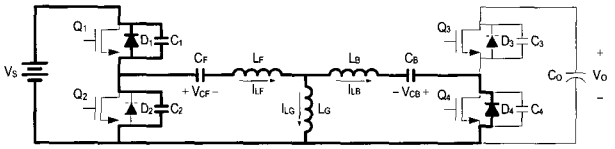
$$(d/dt)I_{L_F} = (-V_{C_F} + V_{C_B} - V_O)/(L_F + L_B) \quad (3)$$

Mode 5 (M_5, $t_4 \sim t_5$): When Q_2 is turned-on in ZVS condition and I_{LF} is decreased to zero, mode 5 begins and D_3 is turned-off in ZCS condition at t_4, as shown in Fig. 4(e). I_{LF} flows through Q_2 and C_4, and I_{LF} is abruptly decreased and C_4 is rapidly discharged by resonance.

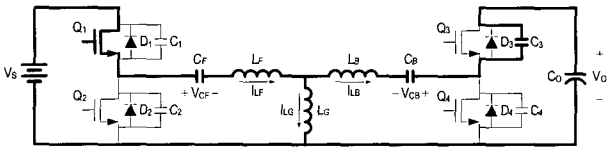
Mode 6 (M_6, $t_5 \sim t_0$'): When C_4 is fully discharged to zero, mode 6 begins and D_4 is turned-on at t_5, as shown in Fig. 4(f). I_{LF} flows through Q_2 and D_4, and it is linearly increased with the slope given by

$$(d/dt)I_{L_F} = (-V_{C_F} + V_{C_B})/(L_F + L_B) \quad (4)$$

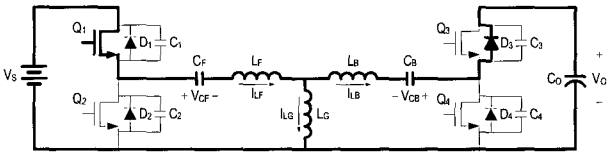
When Q_1 is turned-off at t_0', mode 6 ends and mode 1 begins again.



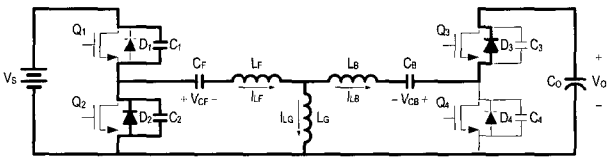
(a) Mode 1



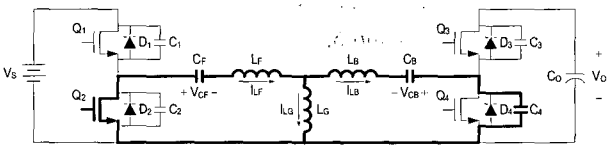
(b) Mode 2



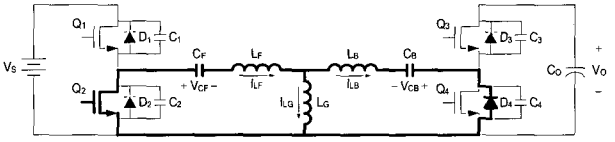
(c) Mode 3



(d) Mode 4

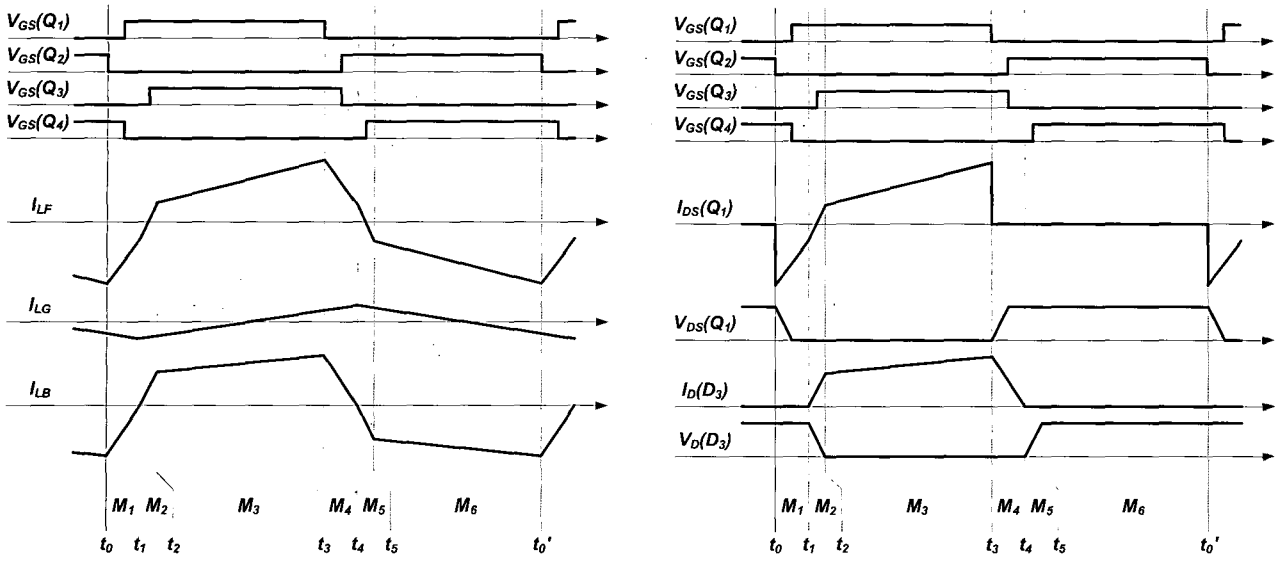


(e) Mode 5



(f) Mode 6

Fig. 4 Operational modes of the proposed converter



(a) Key current waveforms (b) Key switching waveforms

Fig. 5 Key waveforms of the proposed converter

2.3 Input-output voltage conversion ratio

In order to obtain the input-output voltage conversion ratio of the proposed converter, the following are assumed:

- The proposed converter is operating in steady-state.
- All components are ideal except that all MOSFETs include the parasitic components, such as anti-parallel diodes and output capacitors
- Since C_F, C_B, and C_O are sufficiently large, these capacitors can be regarded as a constant voltage source, which has the voltages, V_{CF}, V_{CB}, and V_O.
- The time intervals of Mode 1, 2, 4, and 5 are can be ignored because they are very short compared with those of Mode 3 and 6.
- Since L_G has large inductance, I_{LG} is assumed to be zero.

By applying the voltage-second product equations on L_F, L_B, and L_G during one switching period, the following equations can be easily obtained:

$$V_{CF} = DV_S \tag{5}$$

$$V_{CB} = DV_O \tag{6}$$

The output load current, I_O, equals the average current of D_3, as shown in Fig. 6, and this is expressed by the following equation:

$$I_O = \frac{V_O}{R_O} = \left[I_1 + \frac{1}{2} \times (I_2 - I_1) \right] \times DT_S \times \frac{1}{T_S} \tag{7}$$

Moreover, I_1 and $(I_2\text{-}I_1)$ can be obtained from the modal analysis as these equations:

$$I_1 = \frac{(1-D)V_S + DV_O}{\sqrt{\frac{L_F + L_B}{C_3 + C_4}}} \tag{8}$$

$$I_2 - I_1 = \frac{(1-D)(V_S - V_O)}{L_F + L_B} \times DT_S \tag{9}$$

Substituting the equations (8) and (9) into (7), the input-output voltage conversion ratio of the proposed converter can be obtained as follows:

$$\frac{V_O}{V_S} = \frac{DT_S + 2\sqrt{(L_F + L_B)(C_3 + C_4)}}{DT_S - 2\sqrt{(L_F + L_B)(C_3 + C_4)} + \frac{2(L_F + L_B)}{D(1-D)R_O}} \tag{10}$$

The input-output voltage conversion ratio is plotted in Fig. 7 as a function of the duty ratio D, varying the output load resistance, R_O, with the condition that $V_S = 42V$, $L_F = L_B = 0.39\mu H$, $C_F = C_B = 220\mu F$, $C_1 = C_2 = 1nF$, $F_S = 50kHz$. The input-output voltage conversion ratio is proportional to both D and R_O.

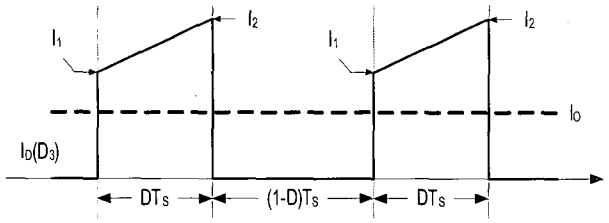


Fig. 6 Simplified current waveform of D_3

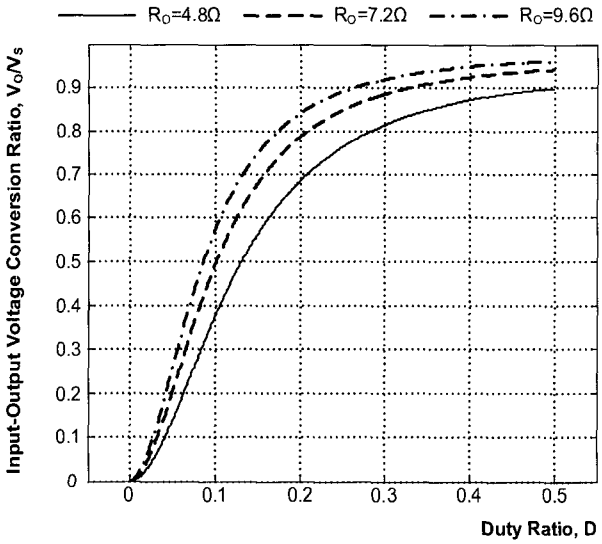


Fig. 7 Input-output voltage conversion ratio

2.4 Output Voltage Ripple Ratio

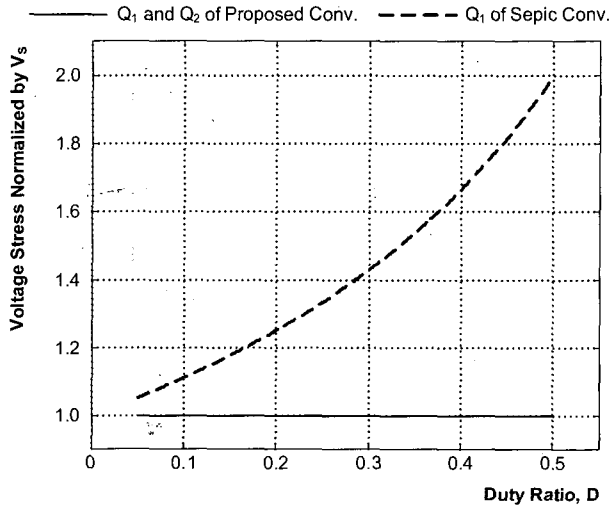
The output capacitor of the proposed converter is charged by the difference of $I_D(D_3)$ and I_O and discharged by I_O, as shown in Fig. 6. The decreased charges of the output capacitor is expressed by

$$\Delta Q = C_O \Delta V_O = I_O \times (1-D)T_S \tag{11}$$

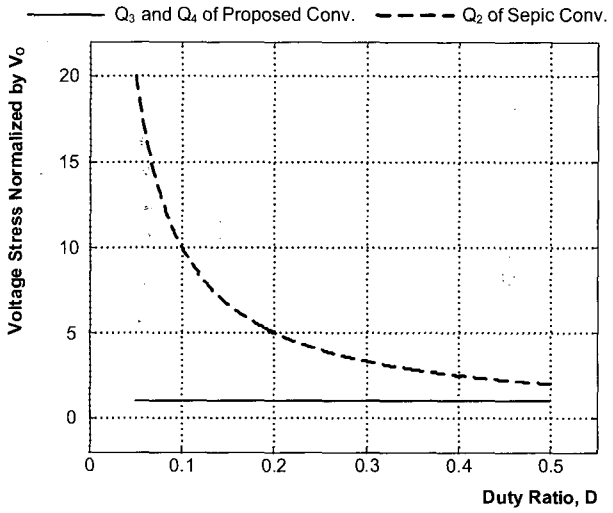
Arranging the above equation, we can obtain the output voltage ripple ratio of the proposed converter as the following equation:

$$\frac{\Delta V_O}{V_O} = \frac{(1-D)T_S}{C_O R_O} \tag{12}$$

The output voltage ripple ratio of the proposed converter is similar to those of the Sepic converter and non-inverting Buck -Boost converter.



(a) MOSFETs of input stage



(b) MOSFETs of output stage

Fig. 8 Voltage stresses of MOSFETs

2.5 Characteristics of Proposed Converter

The proposed converter overcomes the defects of the conventional converters. The advantages of the proposed converter are as follows:

i) Since All MOSFETs of the conventional converters are turned-on and turned-off in hard-switching condition, they have large switching losses. Moreover, the large reverse recovery currents of D_2 in the Sepic converter and D_2, D_3 in non-inverting Buck -Boost converter cause the additional switching losses. Thus, All MOSFETs of the

conventional converters show considerable heat dissipation and need the large heat sinks. On the other hand, MOSFETs, Q_1 and Q_2, of input stage in the proposed converter are turned-on in ZVS condition as described in the modal analysis. Furthermore, MOSFETs, Q_3 and Q_4, of output stage are turned-off in ZCS condition. Therefore, MOSFETs of the proposed converter show the low switching loss and the low heat dissipation, and the heat sinks of MOSFETs in the proposed converter can be minimized.

ii) MOSFETs of the Sepic converter have high voltage stresses as the sum of link capacitor voltage, V_L and output voltage, V_O given by

$$V_{STRESS}(Q_1) = \frac{V_S}{1-D} \tag{13}$$

$$V_{STRESS}(Q_2) = \frac{V_O}{D} \tag{14}$$

Thus, as the duty ratio, D, goes away from 0.5, the voltage stresses increased abruptly. On the other hand, all MOSFETs of the proposed converter have low voltage stresses. In fact, the voltage stresses of Q_1 and Q_2 are clamped to input voltage, V_S, and those of Q_3 and Q_4 are clamped to output voltage, V_O.

$$V_{STRESS}(Q_1) = V_{STRESS}(Q_2) = V_S \tag{15}$$

$$V_{STRESS}(Q_3) = V_{STRESS}(Q_4) = V_O \tag{16}$$

The voltage stresses of MOSFETs in both converters are plotted in Fig. 8 as a function of the duty ratio, D. Therefore, the proposed converter has small conduction losses since MOSFETs of the proposed converter have low on-resistances.

3. Experimental Results

To verify the operational principles and performances of the proposed converter, the 300W prototype for 42V power system HEVs is implemented. The design specifications of the prototype are presented in Table 1, and circuit parameters and components are selected as shown in Table 2.

Key current and voltage waveforms are shown in Fig. 7 and matched the theoretical waveforms. Reducing the capacities of half-bridge capacitors, C_F and C_B, we can obtain lower current stresses of the overall components. Since I_{LG} is sufficiently small, I_{LF} equals I_{LB}. Although the voltages of C_F and C_B show some voltage ripples, the average voltages are well regulated, as presented in the equation (5) and (6), to $V_S/2$ and $V_O/2$, respectively.

Table 1 Design Specification for 42V power system of HEVs

Input Voltage, V_S	42V
Output Voltage, V_O	38V
Maximum Output Power, $P_{O,max}$	300W
Switching Frequency, F_S	50kHz

Table 2 Circuit Parameters for 42V power system of HEVs

L_F, L_B	0.39μH, Air Core
L_G	100μH, 55206A2 (Magnetics)
C_F, C_B	22uF, 25V, MLCC, 5EA
C_O	10000uF, 50V, Electrolytic
Q_1, Q_2, Q_3, Q_4	IXTK250N10, TO-264 AA

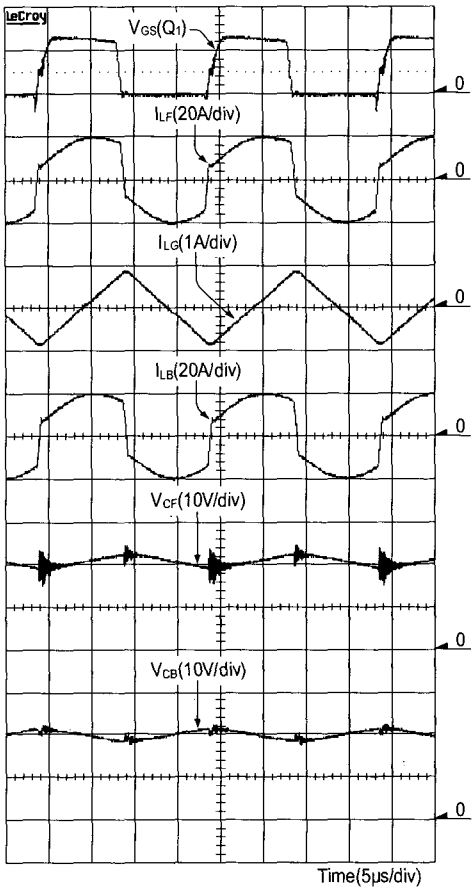


Fig. 9 Key current and voltage waveforms

The switching waveforms of Q_1 and D_3 are presented in Fig. 10. Q_1 and D_3 have the low voltage stresses of 60V and 50V, respectively. The voltage oscillations shown in Fig. 10 are caused by leakage inductances of leads for current measurements. Fig.11 shows the turn-on transient waveforms of Q_1, and we confirmed that Q_1 is turned-on in the ZVS condition. Similarly, Fig.12 shows the turn-off transient waveforms of D_3, and ZCS turn-off of D_3 is verified. The switching waveforms of Q_2 and D_4 are symmetrically the same as those of Q_1 and D_3, respectively.

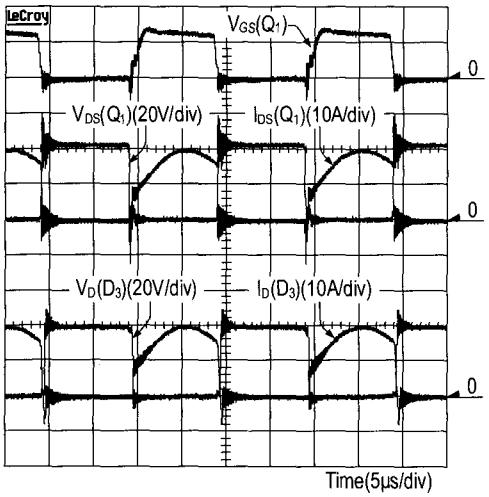


Fig. 10 Switching waveforms of Q_1 and D_3

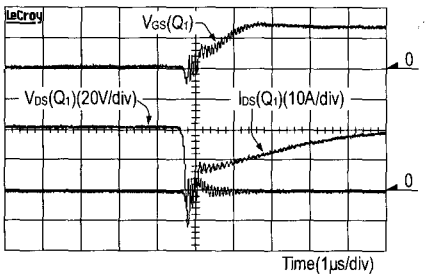


Fig. 11 Turn-on transient waveforms of Q_1

Moreover, the measured efficiencies of the conventional converters and the proposed converter are presented in Fig.13. The proposed converter has the maximum efficiency of 92% at full load condition, and it shows higher efficiency than the conventional converters.

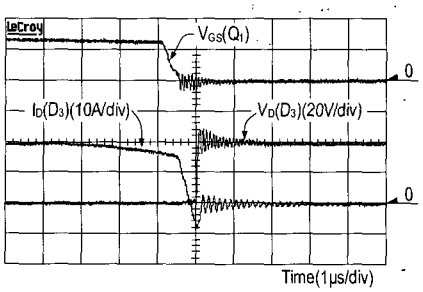


Fig. 12 Turn-off transient waveforms of D_3

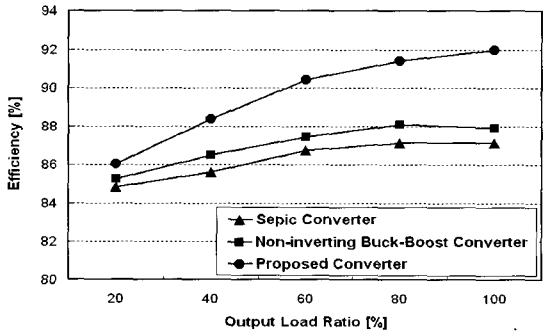


Fig. 13 Measured efficiencies

4. Application to ESS for 42V Power system

The proposed converter can be applied to ESS for 42V power systems of HEVs easily and the circuit configuration for ESS is shown in Fig. 14. When the voltage of a super capacitor, V_C, becomes lower than 38V, the proposed converter operates in the forward mode. On the other hand, when V_C exceeds 46V, the proposed converter operates in the backward mode.

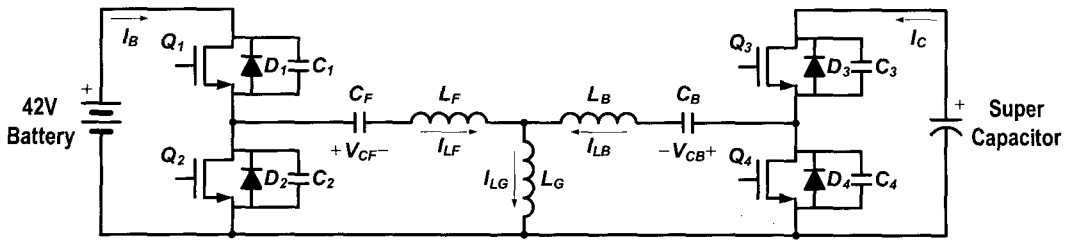


Fig. 14 Circuit configuration for ESS of 42V power system of HEV

5. Conclusions

In this paper, a new high efficiency ZVZCS bidirectional DC/DC converter is proposed. The proposed converter has the minimized components count and shows high efficiency due to low voltage and current stresses and soft switching of MOSFETs. The operational principles of the proposed converter are analyzed and verified by the experimental results using the 300W prototype for 42V power systems. The proposed converter is expected to be suitable for ESS for 42V power systems of HEVs and other low voltage and high current applications.

References

[1] R. A. Dougal, S. Lui, R. E. White, "Power and life extension of battery-ultracapacitor hybrids," IEEE Transactions on Components and Packaging Technologies, vol. 25, issue 1, pp. 120-131, March, 2002

[2] R. M. Schupbach and J. C. Balda, M. Zolot, B. Kramer, "Design methodology of a combined battery-ultracapacitor energy storage unit for vehicle power management," Proceedings of Power Electronics Specialist Conference, IEEE, June, 2003, vol. 1, pp. 88-93.

[3] B. J. Amet, L. P. Haines, "High power DC-to-DC Converter for supercapacitors," Proceedings of International Electronic Machines and Drives Conference, IEEE, 2001, pp. 985-990.

[4] R. M. Schupbach and J. C. Balda, "Comparing DC-DC Converters for Power Management in Hybrid Electric Vehicles," Proceedings of International Electric Machines and Drives Conference, IEEE, June, 2003, vol. 3, pp. 1369-1374.

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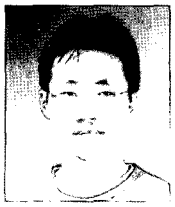

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