Review of alternative gate stack technology research during the last decade

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Abstract

Scaling of the gate stack has been one of the major contributors to the performance enhancement of CMOSFET devices in past technology generations. The scalability of gate stack has diminished in recent years and alternative gate stack technology such as metal electrode and high-k dielectrics has been intensively studied during the last decade. Today the performance of high-k dielectrics almost matches that of conventional SiO_2-based gate dielectrics. However, many technical challenges remain to be resolved before alternative gate stacks can be introduced into mainstream technology. This paper reviews the research in alternative gate stack technologies to provide insights for future research.

1. Introduction to device scaling trend

The performance of a CMOS device is determined by many factors, as shown in Fig.1. For example, a IR drop in the source-drain bias ($V_{SD}' = V_{SD}-I_d*R_{ext}$) reduces the effective source-to-drain bias applied to the channel region. Thus, when external resistance components are increased by high silicide resistance or low extension doping, device performance degrades proportionally. To simplify the discussion, if the external impedance factors shown in Fig.1 are ignored, the drive current of MOSFETs can be expressed by equation (1),

$$I_{D,Sat} \sim \frac{\mu_n C_{OX}}{2} * \frac{W}{L_{Eff}} * f(V_{GS}, V_{DS}), \tag{1}$$

V_{GS} and V_{DS} are the biases applied to substrate and source. Since the MOSFET has capacitance components, its speed can be expressed by the time constant τ, indicating how fast the capacitor components of the MOSFET can be charged or discharged through $I_{d,sat}$. τ can be expressed by equation (2).

$$\tau = \frac{CV}{I} = \frac{C_{OX} * f(V_{GS}, V_{DS})}{2 * I_{DSat}} \sim \frac{L_{Eff}}{\mu_n} \tag{2}$$

In this equation, C_{ox} in the numerator is canceled out by C_{ox} in the $I_{d,sat}$ and the effective channel length L_{eff} and channel carrier mobility μ_n dominate the speed of signal propagation through the MOSFET. Note that parasitic capacitance components are not included in this calculation. However, qualitatively, it is clear that physical scaling is the only way to improve device operation speed. Thus, over the last four decades, the performance of the modern CMOS device has been improved primarily by L_{eff} scaling, as shown in Fig.2.[1]

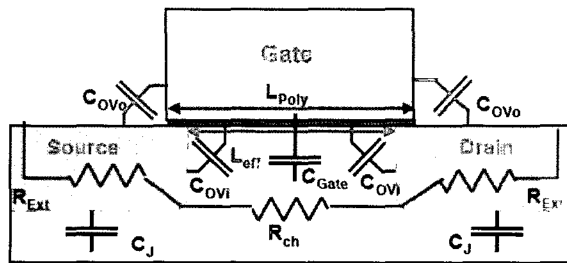


Fig. 1. A Schematic of MOSFET showing various device parameters.

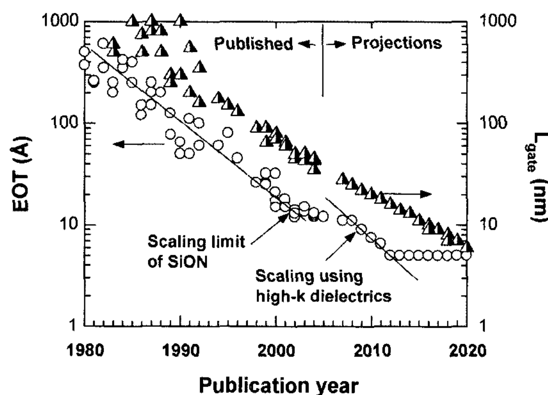


Fig. 2. Scaling trend of gate oxide thickness and L_{gate} over the past five technology generations from the 0.18 μm to 65 nm node. Experimental data or L_{gate} and equivalent oxide thickness (EOT) are collected from device papers presented at major technical conferences and projected value f is based on the 2005 ITRS. When only inversion oxide thickness (T_{inv}) is provided in the literature, 8 Å is subtracted from T_{inv} to account for the additional capacitance components due to poly depletion at the gate side and the quantum mechanical effect at the channel side.

The physical scaling of MOSFETs using shorter wavelength lithography and advanced patterning technologies accompanies many other challenges. As the L_{eff} scales, the cross talk between the source-side junction and the drain-side junction causes various short channel effects. To avoid detrimental short channel effects, all other dimensions of the device such as junction depth and gate oxide thickness need to be scaled together with L_{eff}. The physical scaling of source/drain depth requires a low energy-high current implantation, low resistance silicide, and low heat cycle rapid thermal activation. In particular, gate stack scaling has been one of the key technologies enhancing the performance of semiconductor devices. Gate oxide thickness has been scaled approximately 0.75 times per each technology generation, assuming a 3-year cycle per technology node, as shown in Fig. 2. However, the thickness of the gate oxide has scaled more slowly than the historical pace at an equivalent oxide thickness (EOT) of ~1 nm for the past two to three generations, because of issues such as process controllability, high leakage current, and reliability limitation. Although it was not clear at the time, the physical scaling of SiO_2 gate dielectric was effectively ended around 2002. However, the industry has not yet been able to implement an alternative gate stack and thus a major driver of performance enhancement has been lost, signaling an end to the scaling era and the advent of a new era of material and device evolution.

Since 2002, CMOS devices were continuously improved by controlling the transport properties of channel electrons using strain applied to silicon channels[2-5] and more elaborate control of short channel devices while the control of short channel effects became more difficult due to limited gate oxide scaling. The trade-off between short channel effects and device performance was offset by more precise device design and mobility improvement, another factor shown in equation (2). For more precise device control to optimize short channel devices and parasitic resistance, multiple spacers and precise control of extension doping using an advanced activation anneal such as laser and flash anneal were employed. However, the performance loss due to the trade-off cannot be fully compensated for in the coming technology generations without proper gate oxide scaling. That is why the *International Technology Roadmap for Semiconductors* (ITRS) requires that gate oxide scaling be resumed around 2008 using alternative gate stacks, as shown in Fig. 2.

2. Chronicles of alternative gate stack research

The demise of SiO_2 scaling has been predicted since the 1980s because of the increasing gate leakage current due to direct tunneling current. To reduce the tunneling current, the physical thickness of the gate dielectric had to be increased beyond the tunneling limit. Thus, as early as the 1970s, dielectric materials with dielectric constants higher than SiO_2 were proposed as a possible solution.

As shown in Fig. 3, in the 1980s, CeO_2 and Y_2O_3 were actively studied to replace gate oxides with an EOT ~6 nm.[6-9] Since most of the high-k dielectrics demonstrated severe crystallization-induced leakage current and worse reliability in thick EOT regions, research on high-k dielectrics was phased out as nitrided SiO_2 was successfully implemented in CMOS technology.

In the mid-90s, interest in high-k dielectrics was renewed as the thickness of SiO_2 approached 2 nm, which is the electron tunneling limit of SiO_2. Early work on alternative gate dielectrics focused on TiO_2, Ta_2O_5, and $BaSrTiO_3$, which were inherited from DRAM capacitor dielectric research at that time.[9-14] However, these materials showed relatively high leakage current due to their small band gap. Around 1998, research on high-k dielectrics quickly converged on the Al_2O_3, HfO_2, and ZrO_2 family, which has band gaps larger than 5.0 eV.[16-21] HfO_2 and ZrO_2 received the most attention in the late 1990s due to their better thermal stability with silicon.[22-24] It is interesting that HfO_2 and ZrO_2 were studied as early as the 1970s.[25-27] Various high-k dielectrics studied in this period are listed in Table 1, and a more detailed list of material characteristics is shown in Table 2. A more thorough review of the research during this time can be found in the paper by Wilk et al.[27]

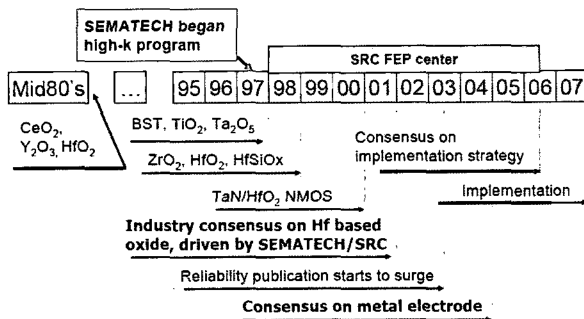


Fig. 3. Summary of key research progress in alternative gate stack research.

The first metal gate/high-k dielectric MOSFET with an EOT ~1 nm was reported at the 2000 IEDM with a TaN/HfO_2 stack, as indicated in Fig. 3. However, at that time, introducing two different materials at the same technology node was unprecedented and considered too aggressive an approach. In 2002, a HfO_2-based dielectric became widely accepted by a leading candidate, primarily driven by SEMATECH and SRC research groups, because ZrO_2 was found to be less stable with a polysilicon gate and can form Zr-silicide during the heat cycle when ZrO_2 is dissociated by the hydrogen incorporated during polysilicon deposition. The difference in the thermal stability of HfO_2 and ZrO_2 can be deduced from the self-diffusion coefficient in Si shown in Table 2. ZrO_2 shows a self-diffusion coefficient several orders of magnitude higher than that of HfO_2, indicating a potential reaction with silicon atoms in the polysilicon gate.

Because of thermal stability issues when in contact with a polysilicon gate,[30] high-k dielectrics were often studied with metals such as Pt or Al at low temperature. Thus, it took some time to discover that the effective work-function (EWF) of a polysilicon gate could not be easily altered by doping when it was used with high-k dielectrics, primarily because the EWF of a polysilicon gate/high-k dielectric stack is determined by Si-metal atom bonding instead of the Fermi level of the polysilicon gate.[31] This problem is often called "Fermi-level pinning," referring to the phenomenon of the EWF of polysilicon being fixed at a certain point near the silicon conduction band edge. As a result, PMOS devices with a

Table 1. List of high-k gate dielectric materials with dielectric constant[29]

Material	ε	Material	ε	Material	ε
Al_2O_3	8-11.5	$LaScO_3$	30	Ta_2O_5-TiO_2	
$Al_xSi_yO_z$		La_2O_3-SiO_2	5-16	TiO_2	86-95
$(Ba,Sr)TiO_3$	200-300	$MgAl_2O_4$	8.3-9.4	TiO_2-SiO_2	
$BeAl_2O_4$	8.3-9.43	Pr_2O_3	14.9	TiO_2/Si_3N_4	
CeO_2	16.6-26	$PrAlO_3$	25	Y_2O_3	8-11.6
$CeHfO_4$	10-20	$NdAlO_3$	22.5	$Y_xSi_yO_z$	
$CoTiO_3$		Sc_2O_3	13	ZrO_2	22.2-28
$EuAlO_3$	22.5	Si_3N_4	7	Zr-Al-O	12-18
HfO_2	26-30	$SmAlO_3$	19	Zr silicate	11-12.6
Hf silicate	11	$SrTiO_3$	150-250	$(Zr,Hf)SnTiO_4$	40-60
La_2O_3	18-20.8	Ta_2O_5	25-45	Ta_2O_5-TiO_2	
$LaAlO_3$	23.8-27	TaON		Y_2O_3	8-11.6

polysilicon gate/high-k dielectric stack show very high threshold voltage (V_{th}) values, beyond the practical range. This problem can be alleviated by using high-k materials with a pinning point close to the silicon valence band edge, favorable to PMOS. Very thin Al_2O_3 or AlN capping has been proposed for this kind of application, but the usable range of EWF is limited even with these capping materials[32-34] and an impact on overall EOT and mobility degradation was pointed out as a limitation.

Around 2003, the limited Vth controllability was recognized as a serious challenge in the implementation of high-k dielectric because the EWF of NMOS and PMOS should be close to the conduction band (Ec~4.05eV) and valance band (Ev~5.15eV) of Si to obtain the best performing CMOS devices and the margin for effective workfunction should be less than 100mV[35]. The reduced adjustable effective workfunction range of polysilicon gate/high-k dielectric stack limits its application to low power applications where the requirement for threshold voltage is not as strict as in high performance devices. Thus, around 2004, the industry reached a rough consensus that metal electrodes should be used with high-k dielectrics. It is ironic to see that the very reason for choosing Hf-based oxide was due to its compatibility with polysilicon gate, but polysilicon gate was discarded due to its incompatibility with Hf based high-k dielectrics. The search for the right metal electrode for nMOS and pMOS applications has not been as easy as it was thought to be in 2003, and it remains an ongoing challenge.

Table 2. Material properties of selected high-k materials.[29] Thermal expansion coefficient of silicon = $2.6x10^{-6}$ K^{-1}. Lattice constant of silicon = 5.43 Å.

	HfO_2	ZrO_2	CeO_2	Y_2O_3	Al_2O_3	SiO_2
Bandgap (eV)	5.68	5.16	5.5	5.5	8.3	9
Barrier height to Si (eV)	1.6	1.5			2.08	3.2
Dielectric constant	~30	~25	26	14-17	8-10	3.9
Dielectric strength (MV/cm)	2-4.5			3-4.5	>1.0	5-10
DC resistivity (Ω/cm)	$4.5x10^{-3}$ @1100℃	10^6 @385℃			10^{14}	10^{14}-10^{16}
Dit	~10^{11}	~10^{11}		~10^{11}	~10^{11}	<$5x10^{10}$
Heat of formation (Kcal/mol)	271	261.9		454.3	399	
ΔG for silicidation ($Si+MO_x \rightarrow MSi_x+SiO_2$)		5.914	7.098		n.a.	n.a.
ΔG for reduction ($Si+MO_x \rightarrow M+SiO_2$)	47.648	42.326	36.29	116.8	64.39	n.a.
Refractive index	2.2	2.05	2.28	1.85-1.93	1.68-1.77	1.468
Density(g/cm³)	9.68	5.9-6.1	6.86	5.03	3.94-3.98	2.27
Thermal conductivity (W/cm℃)		3.06			0.2	0.014
Melting point(℃)	2900	2677	2600	2420	2072	
Thermal expansion Coefficient(10^{-6} K^{-1})	5.3	7.01		8.3	6.7	0.5
Lattice constant	5.11	5.10	5.411	10.60	4.7-5.2	
Self diffusion coefficient @900(℃)	2.8227 $x10^{-17}$	6.0009 $x10^{-10}$			1.5048 $x10^{-7}$	
Transition temperature(℃)	1700	1265				

3. Recent advances in metal electrode/ high-k dielectric development

As mentioned above, around 2002, Hf-based oxides, including HfO_2 and HfSiOx, emerged as promising candidates because of their excellent thermal stability with silicon. However, the mobility and reliability of these materials were not satisfactory for device applications. Mobility degradation of high-k dielectrics was thought to be an intrinsic characteristic due to optical phonon scattering and remote charge scattering. In 2003, A. Kerber et al. proposed that transient charging might have skewed the mobility measurement[36,37] and in 2004, B.H. Lee and C. Young et al. showed that there is very fast transient charging due to the carrier exchange between the channel carrier and trapping sites in high-k dielectric.[38,39] Fast transient charge trapping increases the threshold voltage of high-k devices in μseconds, reducing their drive current accordingly. Since conventional current-voltage (I-V) meters integrate signals on the order of milliseconds and the time scale of capacitance voltage (CV) measurements and I-V measurements does not exactly match, mobility calculations using I_d-I_g curves and CV curves tend to underestimate the mobility value, as shown in Fig. 4.[38] In Fig. 4, the integration time to measure the drain current was set by the pulse width to measure the drain current and the drain current averaged during the pulse width was gradually recovered as the integration time was reduced. If mobility is recalculated using the I_d-V_g curve measured with a pulse measurement method, the intrinsic mobility degradation is much less than the value usually reported in the literature. Using the understanding from the pulse measurement, the intrinsic mobility of high-k devices was studied in detail and it was understood that reducing transient charging was the key to improving high-k device mobility. The key breakthroughs that enabled an enhancement in mobility were 1) understanding of transient charging behaviors in high-k devices [36-40] and 2) scaling of the high-k thickness below the tunneling limit to eliminate residual tunneling carriers in the high-k layer.[41-43] In 2005, drastically improved mobility values, almost matching that of nitride oxide at an EOT of ~1 nm, were reported.[44,45]

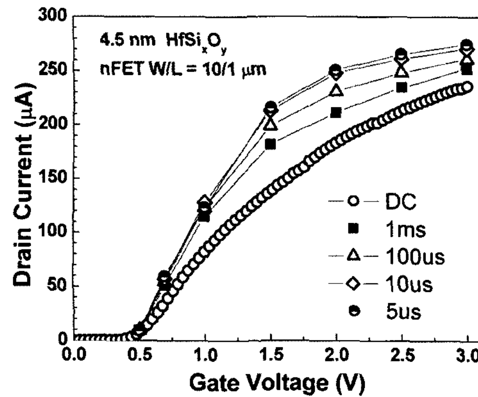


Fig. 4. I_d-V_g curve measured with single pulse measurement. Each points of I_d-V_g curves are the drain current values measured and averaged during the pulse width in a range of 5 μsec to 1 msec.

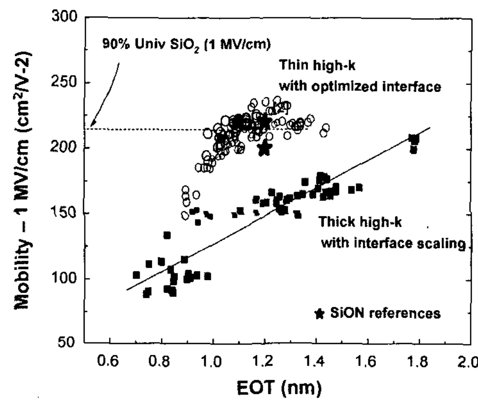
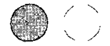


Fig. 5. Scatter chart of high field mobility (1 MV/cm) vs. EOT of various high-k devices fabricated at SEMATECH. Filled square data are obtained from devices with high-k dielectrics thicker than 30 Å while open circle data are obtained from devices with high-k dielectrics thinner than 25 Å. Reference line represents the 90% of SiO_2 universal mobility at 1 MV/cm, which is close to the high field mobility of heavily nitrided oxides used in 90 nm technology. Three reference data points are also indicated by the star symbol.

By keeping the thickness of the high-k layer below 2 nm, the mobility degradation due to transient charging

effects can be eliminated. The high field mobility value vs. EOT curve shown in Fig. 5 clearly demonstrates this observation. However, thinning the high-k layer is only a temporary measure that works for a limited range of EOTs and leakage currents. Low standby power (LSTP) applications require a very low leakage current, and, to meet LSTP targets, the thickness of the high-k dielectric must be increased without degrading mobility. Careful optimization of the bottom oxide and Hf-silicate composition is also necessary. For high-performance applications, more aggressive EOT scaling is needed, but the physical scaling of the HfSiON layer can be limited to an EOT of ~0.8 nm to keep mobility above 85% of the universal curve.[44] Thus, to scale the EOT of the total stack, the interfacial oxide layer should be further optimized. Scaling the interfacial layer, however, imposes serious limitations on the process window in terms of the applicable high-k layer and heat cycle. Additionally, mobility decreases rapidly as the thickness of the interfacial layer is scaled. When an interfacial oxide is thinner than 0.9 nm, the impacts of optical phonon scattering[46] or remote charge scattering [47] on channel carrier mobility rapidly increase. To avoid the trade-off between EOT scaling and mobility, it is important to 1) eliminate the charge scattering source within the high-k layer using elaborate passivation processes[48-50] and 2) increase the dielectric constant of the interfacial oxide with a minimal impact on interface state density.[51] While HfSiON can be used for the 45 nm and 32 nm generations, any further extension of high-k dielectrics will require materials with a dielectric constant higher than HfO_2. Lanthanide oxides have been proposed as higher-k materials, but many of them exhibit worse dielectric characteristics than Hf oxides.[52-54] An alternative path to future scaling is to use channel materials other than silicon. For example, the formation of interfacial oxide can be suppressed when a high-k dielectric is deposited on Ge or GaAs substrates.[55-57] While the quality of the interface may be compromised with these channel materials, the scalability of the high-k dielectric stack will be enhanced. The challenges of this approach are to overcome the problems associated with the degraded interface and to make use of the benefits of high carrier mobility in Ge or other channel materials. If Hf-based oxide can be successfully implemented with these channel materials, Hf-based oxide might still be usable beyond the 32 nm node.

As mentioned above, the application of poly/high-k stacks is limited by V_{th} controllability, poor reliability, dopant penetration, and inversion oxide thickness (T_{inv}) scalability. Thus, n-type and p-type polysilicon gates must be replaced by metal electrode materials with proper EWFs close to Ec and Ev of the silicon substrate. Although the concept of the metal electrode is not new because the first semiconductor devices used Al electrode in the 1960s, there is a huge gap in understanding of the role of metal electrodes. The main technical challenge in this research is that the vacuum workfunction values of metals are not directly correlated to the V_{th} of devices because of 1) dipole formation due to the charge transfer between metal atoms and dielectric atoms,[58] 2) interface mixing during CMOS processing,[59] 3) oxygen redistribution across the metal/high-k interface,[60] 4) formation of interface defects and charge redistribution around the defects, 5) the effect of impurities,[61] and 6) localized compositional variations in electrode materials.[62] Thus, overall electrode processes such as the deposition method, heat cycle, and dielectric composition need to be optimized together to develop a well defined metal electrode process. These problems have been recognized only recently; many of the issues listed above are not well understood for most materials.

Since 2000, many publications have addressed metal electrodes, but there was little consensus on which electrode should be used with high-k dielectrics. For the same material, many different workfunction values have been reported, as shown in Fig. 6. One of the obvious rea-

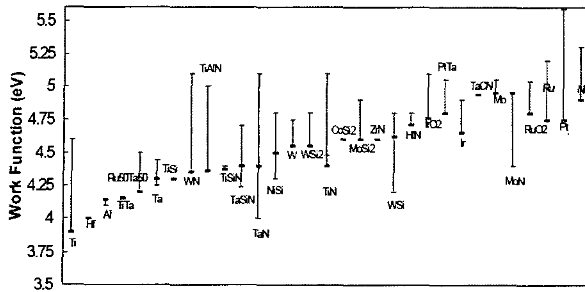


Fig. 6. Workfunction values reported in the literatures vary widely for the same material system depending on deposition method and differences in subsequent processes.[63]

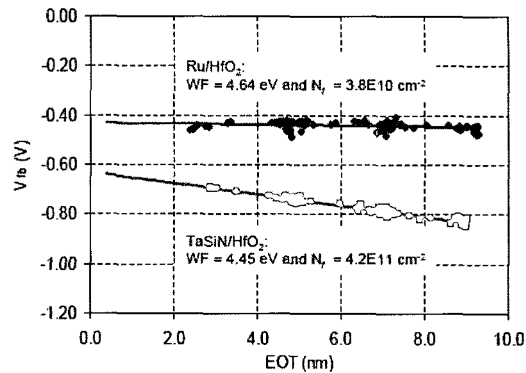


Fig. 7. An example of a V_{fb}-EOT curve generated from a terraced oxide wafer.

sons for such variation is the diverse factors affecting the EWF, but a less obvious reason is that the way the workfunction values were extracted was not accurate. In many publications, workfunction values were extracted using 3-5 points scattered around a linear curve, especially using thick oxide. However, an EWF that determines the threshold voltage of a device should be extracted at the thickness range where the device operates, i.e., at an EOT ~1 nm. Otherwise, the workfunction values extracted in the wrong thickness range or at limited data points do not have a practical meaning.

In 2005, SEMATECH proposed a "terraced oxide wafer technology," which uses a single wafer containing several bands of gate dielectric thicknesses with EOTs from 1.5 nm to 9 nm.[64] Fig. 7 shows an example of EWF extraction using a terraced oxide wafer in the EOT range of 2.5 nm to 9 nm. In this method, more than 49 data points were used to extrapolate the workfunction. Using sufficient data points and extending the V_{fb} vs. EOT curve into a thin oxide region ensure the accuracy of this extraction. Today, more groups are using methodologies similar to the terraced oxide wafer. Note that in this paper, "EWF" is used instead of "workfunction" to define the physical properties of electrodes because in the conventional meaning of workfunction, the work needed to extract an electron from the metal surface does not have a direct correlation with the threshold voltage of metal gate devices. The threshold voltage of a device with a metal gate/high-k dielectric gate stack is determined by the bonding configuration at the interface between the metal electrode and high-k dielectric instead of the vacuum workfunction of the metal electrode, and the bonding configuration is influenced by the many factors listed above. Thus, very careful investigation is necessary to define the EWF of a metal electrode system, which cannot be separated from the underlying dielectric or subsequent processes. In short, EWF is no longer a characteristic of metal electrodes, but a characteristic of the overall gate stack and should be defined as such.

Finding a metal electrode system that meets the specifications for a scaled device has been challenging. Not only the scattered data in the literature, but also the limited infrastructure to study metal gate devices have constrained overall progress and the fierce competition to arrive at a metal electrode solution has forced the leading research group to refrain from sharing its learning. Thus, only limited information about metal electrode systems is available in the open literature. In 2003, Intel announced that their metal electrode solution was ready without disclosing the material system.[65] In 2005, SEMATECH also showed an EWF chart including material systems with a band edge electrode solution, again without specifying the metal electrode, as shown in Fig. 8.[66]

In Fig. 8, several metal systems showed EWF values

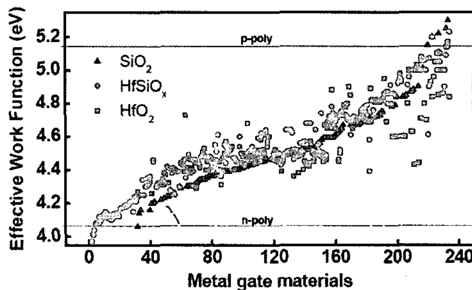


Fig. 8. EWF values of various metal systems extracted after 1000℃, 5sec anneal. The X axis represents the material systems and three groups of data points showed EWFs obtained with two different gate dielectrics (SiO_2, and HfSiOx). Data included in Fig. 8 were obtained using a terraced oxide wafer.[61] To study the change in EWF at the metal/high-k interface, very thin HfSiON layers were deposited on a terraced oxide wafer.

near the conduction and valence band edge of silicon even after high temperature processing, satisfying the requirements for gate-first CMOS integration (EWF of electrodes should be close to $E_{c,si}$ for nMOS and $E_{v,si}$ for pMOS after the CMOS heat cycle, which is typically a 1100℃ spike anneal or 1000℃, 5sec rapid thermal anneal). Metal electrode systems are not specified in Fig. 8 because the EWF of a metal/high-k stack can be controlled by many factors described above and, in fact, electrode and high-k dielectrics are better considered as a single materials system that requires simultaneous optimization. A detailed method of controlling the EWF of metal electrode/high-k dielectrics will be discussed in the future publications.

Due to difficulties associated with metal electrode research such as material definition and contamination control, several research groups have investigated the feasibility of silicide electrodes. Fully silicided (FUSI) gate has received considerable attention since 2001 because the polysilicon gate can be silicided with a relatively low heat cycle with minimal damage to the gate dielectric after device fabrication. Gate silicidation after source/drain silicidation eliminates the concern about metal contamination in the front-end process, and low heat cycle process appeared attractive. $CoSi_2$ was used in the initial demonstration of silicided gate,[67] but the focus quickly shifted to NiSi and $NiSi_3$ because the workfunction of Ni silicides could be modified with dopants in the polysilicon gate or a phase of Ni silicides.[68-71] However, the EWF range was still limited with silicide gate even though the FUSI process used only low temperature processes. Various silicides were studied to find a silicide gate with a band edge EWF. The most promising silicide gate materials are HfSi (~4.2 eV)[72] and ErSi (~4.2 eV) for NMOS and PtSi (~4.9 eV), Pt_2Si(5.0eV) for PMOS.[73] Even though the EWF range is not wide enough for high performance applications, these silicide gates can still be used in low power applications or applications requiring quarter gap electrodes (~4.3 eV for NMOS, ~4.8 eV for PMOS) such as FinFETs or fully depleted silicon-on-insulator (FDSOI) devices.[74] However, there are several potential challenges to the FUSI approach such as pattern dependent silicidation,[75,76] strain control due to volume expansion, and process complexity for a dual silicide approach. Also, the need for two different silicide materials to achieve lower nMOS and pMOS threshold voltages actually complicates the overall integration process as shown in Fig. 9. The proposal to use metal layers with different thicknesses for dense and sparse patterns

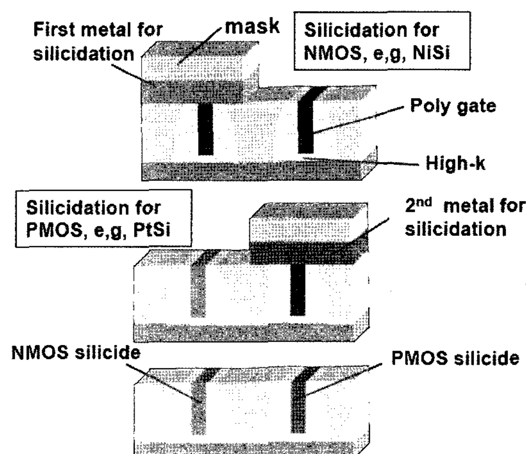


Fig. 9. A potential integration scheme for dual workfunction fully silicided (FUSI) gate devices.

to solve the problem of pattern-dependent silicidation further increases the complexity of the FOSI process. While the reliability of FUSI devices has not been explored extensively, an initial study indicates that it might be degraded by the reliability degradation mechanisms that have affected polysilicon gate/high-k dielectric stack devices. Polysilicon gate devices show a much higher level of bias temperature instability than metal gate devices, potentially due to higher electron-hole pair generation at the polysilicon/high-k dielectric interface.[77]

One subject not addressed in this paper is the reliability of a metal electrode/high-k dielectric stack. Once the electrode materials are chosen for each application, the impact of reliability should be studied in detail. While there are many publications on the reliability of high-k devices, they are in some ways very preliminary works because the influence of metal electrodes has not been accounted rigorously. Metal electrodes can affect the reliability of gate dielectrics in many ways: 1) diffusion and intermixing with the dielectric, 2) oxygen and nitrogen redistribution, and 3) impurity contamination. None of these topics has been well investigated, primarily because the material systems are not finalized yet.

6. Conclusion

In this article, the progress in alternative gate stack technology during the last decade has been reviewed and some current challenges described. Considering the rapid progress in recent years, an alternative gate stack with a metal gate/high-k dielectric will be implemented for silicon-based technology in the near future, but research on reliability will need significant acceleration.

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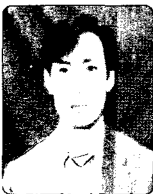

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Hsing-Huang Tseng joined the Advanced Products Research and Development Laboratory (APRDL) of Motorola in 1985. He has been responsible for process and integration development for a variety of gate dielectrics for advanced technologies such as high-K/metal gate stack and plasma nitridation oxynitride etc. Dr. Tseng is a Distinguished Member of Technical Staff and a Motorola Master Innovator with 25 issued U.S. patents. He received a Motorola High Impact Technology Award and a Bravo Award for his technical contributions. He has authored or co-authored over 60 papers in journals and conferences in semiconductor area and received a Golden Quills Award from Motorola for his high quality publications. Dr. Tseng was a Program Manager for Advanced Gate Stack with APRDL of Motorola before assuming the Chief Technologist and the CMOS Extension Program Manager of Front End Processes Division at SEMATECH as an assignee in 2005. He received the Ph.D. degree in Materials research from Princeton University and a BS degree in Physics from Fu-Jen Catholic University. Dr. Tseng has been invited to give talks and short courses in prestigious international conferences such as IEDM (2001) and IRPS (1996). He has served as a committee member for international conferences such as IEDM (1998, 1999) and SISC (1993-1995, 2003-2005) and is the Technical Chair of 2006 International Symposium of VLSI-Technology, System, and Applications. Dr. Tseng served on Program Advisory Board for Front End Processes of International SEMATECH and on Technical Advisory Board for Material and Process Sciences Program of Semiconductor Research Corporation (SRC) from 2001 to 2005.

◉◉ Dr. Rajarao

Dr. Rajarao "Raj" Jammy joined SEMATECH for a three-year assignment from IBM. He served as a manager of Advanced CMOS Gate Stack and Surface Preparation Technologies at the T.J. Watson Research Center in Yorktown Heights, NY and previously managed the Thermal Processes and Surface Preparation Group in the DRAM development alliance between IBM and Infineon.

He holds a doctorate in electrical engineering from Northwestern University and a master's degree from the University of Rochester in Rochester, NY. He also earned a bachelor's electrical engineering degree from Bangalore University in Bangalore, India. He holds 35 U.S. patents and has co-authored nearly 50 invited/peer-reviewed papers in professional journals.