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다중 고착 고장을 위한 효율적인 고장 진단 알고리즘

(An Efficient Diagnosis Algorithm for Multiple Stuck-at Faults)

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요 약

VLSI의 복잡도가 증가함에 따라, 보다 복잡한 고장이 나타나게 되었다. 단일 고장 진단을 위한 많은 방법들이 연구되어 왔다. 때로는 오류가 존재하는 칩에 대한 다중 결함이 실제 현상을 보다 더 정확하게 반영한다. 따라서 다중 고착 고장을 위한 효율적인 고장 진단 알고리즘을 제한하겠다. 제안하는 매칭 알고리즘은 완전일치공통부분을 고장 진단의 중요한 기준으로 사용함으로써 단일 고착 고장 시뮬레이터 환경에서도 다중 고착 고장을 진단할 수 있다. 또한 각 고장간의 식별성을 높여 다중 고착 고장을 진단함에도 불구하고, 고장 후보의 수를 획기적으로 줄일 수 있었다. 이를 위하여 출력단의 수에 따른 가중치 개념과 가산, 감산 연산을 사용하였다. 제안한 매칭 알고리즘은 ISCAS85회로와 완전 주사 스캔이 삽입된 ISCAS89회로에서 실험하여 성능을 입증하였다.

Abstract

With the increasing complexity of VLSI devices, more complex faults have appeared. Many methods for diagnosing the single stuck-at fault have been studied. Often multiple defects on a failing chip better reflect the reality. So, we propose an efficient diagnosis algorithm for multiple stuck-at faults. By using vectorwise intersections as an important metric of diagnosis, the proposed algorithm can diagnose multiple defects using single stuck-at fault simulator. In spite of multiple fault diagnosis, the number of candidate faults is also drastically reduced. For fault identification, positive calculations and negative calculations based on variable weights are used for the matching algorithm. Experimental results for ISCAS85 and full-scan version of ISCAS89 benchmark circuits prove the efficiency of the proposed algorithm.

Keywords : Multiple Stuck-at Faults, Diagnosis, Fault Simulation

I. Introduction

With the increasing complexity of VLSI devices, the demand for fault diagnosis has also increased. Fault diagnosis is the process that deduces the location of the defect which caused the failures. An accurate fault diagnosis can identify both design and process errors, thus improving yield. Therefore, it is very important to develop an efficient fault diagnosis methodology in order to improve device quality and reduce production cost^[1].

The score matching method is based on the

hypothesis that the more closely the simulated response for the fault matches the response from the tester, the closer the corresponding predicted fault site is to the actual defect site.

In the most advanced POIROT algorithm^[2], the calculation of the score is based on the metrics of intersections(vectorwise intersection), mispredictions and nonpredictions. The score of each candidate fault consists of the accumulated values for vectorwise intersections, intersections, nonintersections and mispredictions for all test patterns. While vectorwise intersection is the strongest metric, misprediction is the weakest metric.

The score matching method generally assumes the single fault assumption. While the single fault

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assumption simplifies the diagnosis process, it leads to problems with multiple and complex faults.

In this paper, we describe an efficient diagnosis algorithm for multiple stuck-at faults. Because of its accurate fault identification scoring, the size of candidate faults set is minimized.

II. The Proposed Diagnosis Algorithm

In a single stuck-at fault simulation, the fault scores are calculated by the matching algorithm and the vectorwise intersection table is generated. After fault simulation, the final fault candidates are decided with the fault scores and the vectorwise intersection. Figure 1 explains this process. For the diagnosis, the verilog design file, test patterns and tester responses of a faulty circuit are needed. The algorithm scores candidate faults and generates the vectorwise intersection table in the fault simulation. Finally, it outputs the diagnostic results after the fault simulation.

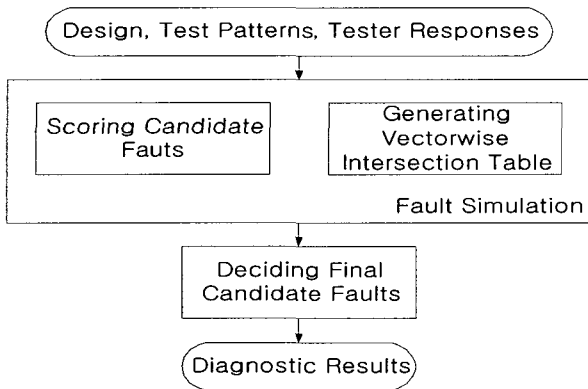


그림 1. 제안하는 매칭 알고리즘
Fig. 1. The proposed diagnosis algorithm.

III. Scoring Candidate Faults

The previous algorithm calculates fault scores using the number of patterns for vectorwise intersection, intersection, misprediction and nonprediction. Because of its low fault identification, it has many candidate faults. Vectorwise intersection dominates intersection, misprediction and nonprediction in the previous

algorithm. In a multiple faults case, the faulty response of a tester seems a mixture of the faulty response of each fault. Therefore, the score of a real fault is low for intersection.

We propose an efficient matching algorithm using the variable weight for the number of primary outputs. Unlike previous matching algorithms, our proposed matching algorithm simultaneously uses positive calculation, negative calculation and vectorwise intersection using the variable weight. The previous algorithm just counts the number of test patterns of vectorwise intersection, and it has the highest priority. But our proposed matching algorithm scores the variable weight for the number of primary outputs at the event of vectorwise intersection. The weight for vectorwise intersection has to differ in proportion with the size of the circuit. If the circuit has more primary outputs, it is more difficult that the fault simulation results are exactly matched with the tester outputs for that test pattern. We use the number of primary outputs as the variable weight.

Fault simulation consists of a double loop, with the outer one over all of the faults in the fault list and the inner one over all of the test patterns. After simulating faults for one pattern, the score is calculated with the matching algorithm. The score of each candidate fault is the accumulated score over all the test patterns.

The proposed matching algorithm classifies the faulty response into 5 types and calculates fault scores with each approach.

1) vectorwise intersection : Both the tester response and the simulation response have faulty responses, and they are exactly same. In this case, the score is increased by the number of the primary outputs.

2) intersection : Both the tester response and the simulation response have faulty responses, but they are not exactly the same. In this case, the score is increased by the number of simultaneously erroneous outputs. In a similar manner, the score is decreased by the number of independently erroneous outputs.

3) misprediction : The tester response does not

have faulty responses, but the simulation response has a faulty response. The score is decreased by the number of erroneous outputs of the simulation response.

4) nonprediction : The tester response has faulty responses. The simulation response does not have a faulty response. The score is decreased by the number of erroneous outputs of the tester response.

5) no error : Both the tester response and the simulation response do not have faulty responses. In this case, the fault score is not calculated.

For a more accurate diagnosis, we devised the variable weight of vectorwise intersection relative to the number of primary outputs. The number of primary outputs reflects the complexity and the size of circuits. The more primary outputs there are, the harder it is to correlate them with the faulty responses and the simulated results. Though both the tester response and the simulation response are exactly same, the proposed algorithm distinguishes between vectorwise intersection and no error by the existence of the faulty response. It relieves a problem where the fault that has the most no error cases is of the highest rank.

IV. Vectorwise Intersection Table

General scored matching algorithms have problems with diagnosing multiple stuck-at faults, because many faults have the highest score.

To find the way to relieve this problem, we analyzed the responses of the multiple stuck-at faults. We concluded that errors of the multiple stuck-at faults response are incorporation of each single stuck-at fault response in many cases. If the test pattern activates a single fault, the response of multiple stuck-at faults is the same as the response of a single stuck-at fault. If the test pattern activates multiple faults, the response of multiple stuck-at faults is the incorporation of each single stuck-at fault response or strange response. If the test pattern activates a single fault, the response of multiple stuck-at faults is the incorporation of

vectorwise intersections of a single fault. In the earlier SLAT paper, patterns that activate a single fault form a large majority^[3]. According to that assumption, we store faults and failing patterns whenever vectorwise intersection occurs, and it is said the vectorwise intersection table. The vectorwise intersection table and fault scores are employed to decide the final candidate faults.

V. Deciding Final Candidate Faults

After fault simulation, we can use fault scores that reflect the similarity between real defects and the vectorwise intersection table. Deciding the final candidate faults consists of the following steps:

1. Sort candidate faults according to their scores.
2. Select candidate faults that have the most vectorwise intersections in the top scored faults.
3. Select candidate fault that explains unexplained failing patterns and has the highest score in unselected candidate faults.
4. If there are unexplained failing patterns, iterate Step 3.

Simply selecting highest scored faults can not diagnose multiple stuck-at faults. Even if one fault is ranked top, other faults are ranked low. To relieve this problem, the vectorwise intersection table is employed. Although the fault score is low, if the fault has vectorwise intersection, the fault can be selected. The SLAT algorithm^[3] has the problem that the size

표 1. ISCAS85회로의 고장 진단 결과
Table 1. The Diagnosis Results of ISCAS85 circuits.

Circuits	SLAT [3]		The proposed algorithm	
	Detected faults	Candidate faults	Detected faults	Candidate Faults
c432	1.67	9.77	1.73	4.20
c499	1.23	31.27	1.37	2.73
c880	1.90	9.57	1.93	2.67
c1355	1.13	19.93	1.13	3.40
c1908	1.20	10.07	1.63	2.30
c2670	1.83	21.97	1.80	2.60
c3540	1.77	9.53	1.83	3.17
c5315	1.83	14.03	1.83	3.03
c6288	1.70	27.23	1.70	3.53
c7552	1.83	37.83	1.83	3.13
Average	1.61	19.12	1.68	3.08

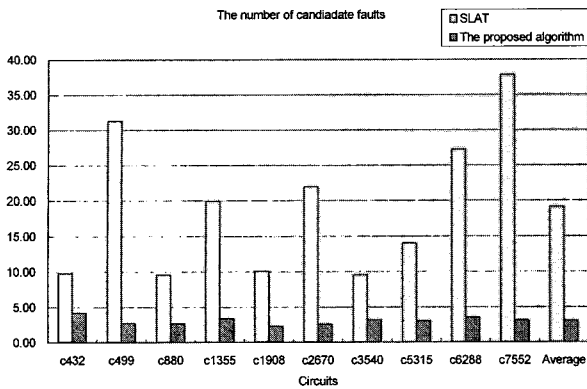


그림 2. ISCAS85회로에 대한 최종 고장 후보 수
 Fig. 2. The number of candidate faults of ISCAS85 circuits.

표 2. ISCAS89회로의 고장 진단 결과
 Table 2. The Diagnosis Results of ISCAS89 circuits.

Circuits	SLAT [3]		The proposed algorithm	
	Detected faults	Candidate faults	Detected faults	Candidate Faults
s1196	1.77	11.53	1.93	2.93
s1238	1.77	13.87	2.00	3.20
s1488	1.70	12.00	1.80	3.47
s1494	1.77	12.47	1.73	3.73
s5378	1.90	8.67	1.90	2.90
s9234	1.93	11.97	1.93	3.87
s13207	1.83	15.63	1.83	4.40
s15850	1.97	10.80	1.97	3.03
s35932	1.93	11.80	1.93	3.47
s38594	1.97	9.30	1.97	2.67
Average	1.85	11.80	1.90	3.37

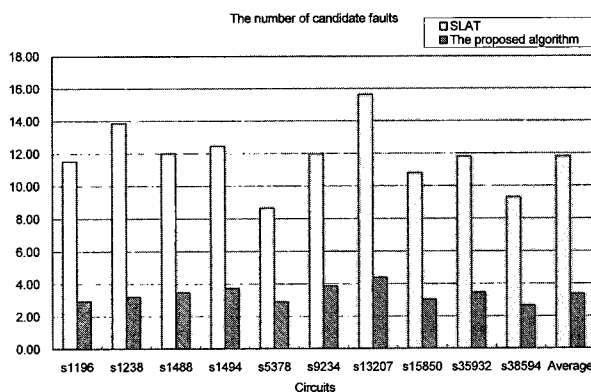


그림 3. ISCAS89회로에 대한 최종 고장 후보 수
 Fig. 3. The number of candidate faults of ISCAS89 circuits.

of candidate faults is large, but the proposed algorithm minimizes the size of candidate faults sets. In chapter 6, experimental results for ISCAS85 and full-scan version of ISCAS89 benchmark circuits

prove the efficiency of the proposed algorithm.

Table 1 illustrates that the number of faults which were diagnosed by the SLAT algorithm is 1.61, on average, and by the proposed algorithm is 1.68. The diagnostic accuracy of the proposed algorithm is almost the same as or slightly better than that of the SLAT algorithm. But the number of candidate faults of the proposed algorithm is much smaller than the number of the SLAT algorithm. The average number of candidate faults is 19.12 for the SLAT algorithm and 3.08 for the proposed algorithm. It is almost a six-fold difference. It means the proposed algorithm is more efficient. This difference is more easily observed in figure 2.

The proposed algorithm is greatly efficient for not only combination circuits but also large full scan circuits. Table 2 illustrates diagnostic results for the full scan version of ISCAS89 circuits. The number of faults which are diagnosed by the SLAT algorithm is 1.85, on average, and by the proposed algorithm is 1.90.

The average number of candidate faults is 11.80 for the SLAT algorithm and 3.37 for the proposed algorithm. It is almost a 4 times difference. The difference is illustrated clearly in Figure 3.

VI. Conclusions

In this paper, we have proposed an efficient diagnosis algorithm for multiple stuck-at faults. Because it uses vectorwise intersections as an important metric of diagnosis, the proposed algorithm can diagnose multiple defects using a single stuck-at fault simulator. The proposed matching algorithm considers positive calculation, negative calculation and vectorwise intersection with the variable weight to determine the number of primary outputs. The sophisticated matching algorithm can precisely identify each fault. In spite of multiple faults diagnosis, the number of candidate faults is drastically reduced.

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