논문 2006-43SC-5-4

CMOS OTA들 이용한 1MHz, 3.3-1 V 동기식 Buck DC/DC 컨버터

(A 1MHz, 3.3-V Synchornous Buck DC/DC Converter Using CMOS OTAs)

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요 약

본 논문은 회로 구성 블록으로 CMOS 연산 트랜스컨덕턴스 증폭기(OTA)를 사용한 새로운 3.3-1 V 동기식 buck DC/DC 컨버터를 제안한다. PWM 회로의 오차 증폭기 OTA는 온도 안정성 향상을 위해 보상되었다. 보상된 OTA 트랜스컨덕턴스 이득의 온도 계수는 0-100°C 범위에서 150 ppm/°C 이하이다. 0.35㎛ 표준 CMOS 공정으로 HSPICE 시뮬레이션을 수행한 결과는 40-125 mA의 부하 전류 범위에서 제안된 컨버터의 효율이 80% 이상임을 보여준다. 이러한 결과는 제안된 컨버터가 전지로 동작되는 시스템에 이용하기에 적당함을 보여준다.

Abstract

This paper presents a new 3.3-1 V synchronous buck DC/DC converter that employs CMOS operational transconducatance amplifiers (OTAs) as circuit-building blocks. An error amplifier OTA in a PWM circuit is compensated for to improve temperature stability. The temperature coefficient of the transconductance gain of the compensated OTA is less than 150 ppm/°C over 0-100°C. The HSPICE simulation results of the 0.35㎛ standard CMOS technology show that the efficiency of the proposed converter is as high as 80% in the load current range of 40-125 mA. These results show that the proposed converter is adequate for use in battery-operated systems.

Keywords: Synchronous buck converters, Operational transconductance amplifiers, Analog integrated circuits

I. Introduction

Portable products such as cellular phones, notebook computers, and personal digital assistants require low power circuitry for battery operation. This can be achieved by using low-voltage circuitry[1-2]. In such products, a highly efficient step-down DC/DC converter is necessary to operate low voltage circuitry and maximize battery life.

To reduce the conduction loss of a diode at a low voltage, buck converters based on synchronous rectification have been studied[3-5]. These converters show high efficiency with small size inductors. Since their output voltages are relatively higher than 3V, however, they are unsuitable for devices powered by lithium ion batteries. High efficiency synchronous

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※ 본 논문은 IT-SoC 핵심 설계 인력양성 사업 및 IDEC의 지원으로 수행된 결과임.
접수일자: 2006년 1월11일, 수정완료일: 2006년7월31일

buck converters with output voltages less than 1.8 V have also been reported[6-7]. They are sufficient for application in current mobile devices. With developments in CMOS technology, the supply voltage is decreasing every year, causing power consumption reduction. Recently, monolithic converters with output voltage of below 1 V have been mentioned in various literature[8-9]. These converters show superior efficiency of more than 80%.

When negative feedback is applied using operational amplifiers (op-amps), the closed-loop transfer function becomes independent of the gain of the op-amp and is determined by the feedback elements. Thus, op-amps are used to develop many useful analog circuits and systems. The converters mentioned so far also use op-amps as circuit-building blocks. To adjust circuit parameters, however, feedback elements must be trimmed. Because the gain of OTAs can be controlled by their bias current, the use of OTAs provides more flexibility for designing analog circuits. In addition, OTAs have simpler structures than op-amps, so are more suitable for integrated circuit designs.

This paper presents a new synchronous buck DC/DC converter using simple CMOS OTAs. Its configuration and operating principles are described in chapter Ⅱ. Chapter Ⅲ discusses the simple CMOS OTA used in the proposed converter and the temperature compensation of its transconductance gain. To demonstrate their performance, simulation results using HSPICE with 0.35㎛ CMOS n-well standard process technology are presented in chapter Ⅳ.

Ⅱ. Circuit Description and Operation

1. Synchronous Buck DC/DC Converter

A block diagram of a synchronous buck DC/DC converter is shown in Fig. 1. It is composed of two MOSFET switches *Mp* and *Mn*, an external inductor L_{EX}, an external capacitor C_{EX}, a load resistance

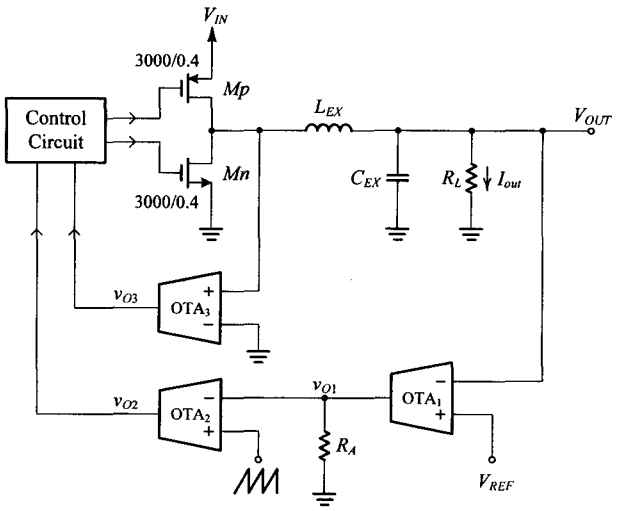

그림 1. 동기정류형 벅 DC/DC 컨버터 블록도
Fig. 1. Block diagram of a synchronous buck DC/DC converter.

R_L, an OTA-*R* error amplifier, two OTA comparators OTA_2 and OTA_3, and a switch control circuit. OTA2 creates a PWM signal by comparing the output voltage of the error amplifier v_{O1} with a saw-tooth wave. The duty cycle D of the PWM signal is given by

$$D = \frac{G_{m1} R_A}{V_M} (V_{REF} - V_{OUT}) \quad (1)$$

where G_{m1} is the transconductance gain of the OTA_1, V_M is the peak-to-peak amplitude of the saw-tooth wave, and V_{REF} is the reference voltage for the regulation. The duty cycle for step-down is determined by the differential of the reference voltage V_{REF} and the desired value of the output voltage V_{OUT}. When V_{OUT} increases more than the desired value, the duty cycle is reduced. When V_{OUT} decreases less than the desired value, the duty cycle is increased. Thus, the output voltage regulation is realized.

Instead of a schottky diode, the n-channel MOSFET *Mn* is employed as a switching element. It is possible for a significant current to flow through two MOSFETs when they are on simultaneously. This will cause power dissipation increase. To

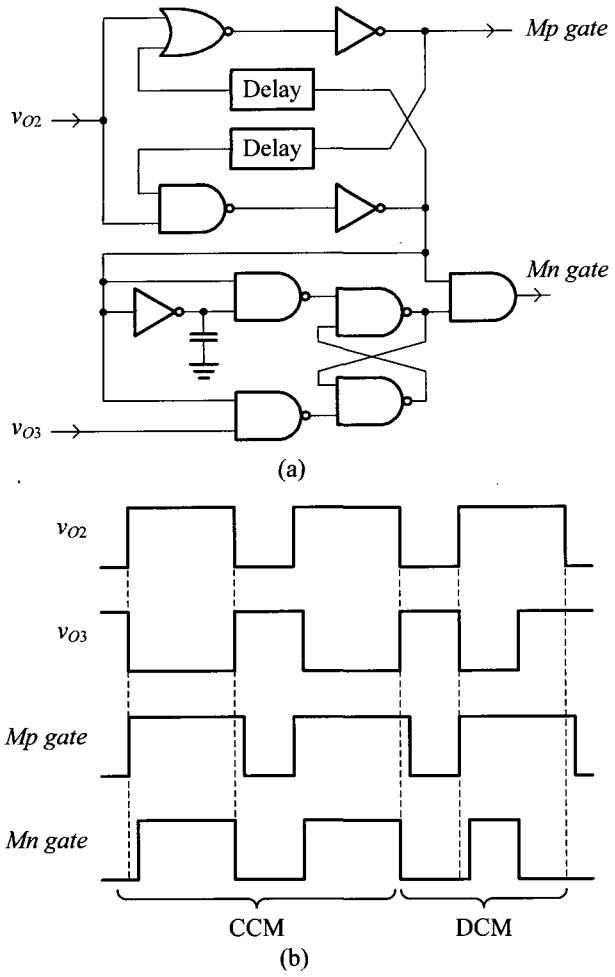

그림 2. (a) 제어회로 회로도와 (b) 타이밍도
Fig. 2. (a) Circuit diagram of the control circuit and (b) Its timing diagram.

prevent such drawback, the switches should be controlled by non-overlapping signals. Fig. 2 shows a circuit diagram of a non-overlapping switch control circuit and its timing diagram in the continuous current mode (CCM) and the discontinuous current mode (DCM). The control circuit consists of two blocks: the non-overlapping gate driver and a reverse current protection circuit. In DCM, the energy stored in L_{EX} is small. This energy is released to the load when the MOSFET *Mn* turns on. Without the reverse current protection circuit, the reverse current flows through the MOSFET *Mn*. Such current consumes the supplementary energy stored in C_{EX}. The protection circuit is needed to turn *Mn* off when the inductor current reaches zero. The comparator OTA_3 is used to sense the current of L_{EX}.

2. Saw-tooth Wave Generator

The saw-tooth wave generator shown in Fig. 1 can be realized using the OTA-R schmitt trigger, the OTA-C integrator, and an analog switch[10]. The original circuit has been slightly modified into a single-supply operation. Its circuit diagram is shown in Fig. 3. A voltage amplifier composed of OTA_1 and R_1, and a comparator composed of OTA_2 and its output resistance form a schmitt trigger with non-inverting transfer characteristics shown in Fig. 4. For the single-supply operation, the current I_R moves the low-threshold voltage of the schmitt trigger to the first quadrant. Note that the threshold voltage of the schmitt trigger is proportional to the bias current of OTA_2 I_{B2}. OTA_3 and the timing capacitor C form an integrator whose time constant is proportional to the bias current I_{B3}. The waveforms associated with the generator are shown in Fig. 5. To see how the generator operates, assume that the output voltage of the schmitt trigger v_O is at a low saturation level of 0 V, and that switch S is open. Since v_O is much lower than V_{REF}, a saturation current of OTA_3 equal to I_{B3} flows into the capacitor C. Thus, the input voltage of the schmitt trigger v_I continues to increase linearly with the slope of I_{B3}/C until v_I reaches the high-threshold voltage of the schmitt trigger, $V_{TH} = R_2(I_R + I_{B2})$. During the interval T_1 we

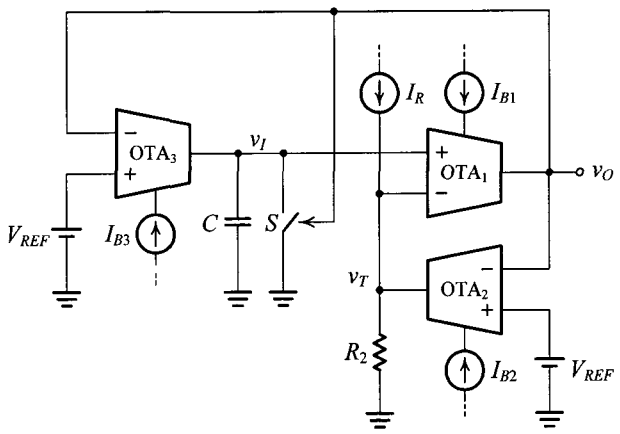

그림 3. 톱니파 발진기 회로도
Fig. 3. Circuit diagram of a saw-tooth wave generator.

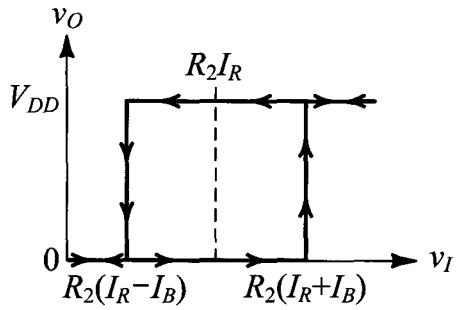

그림 4. 슈미트트리거 전달특성
Fig. 4. Transfer characteristic of the schmitt trigger.

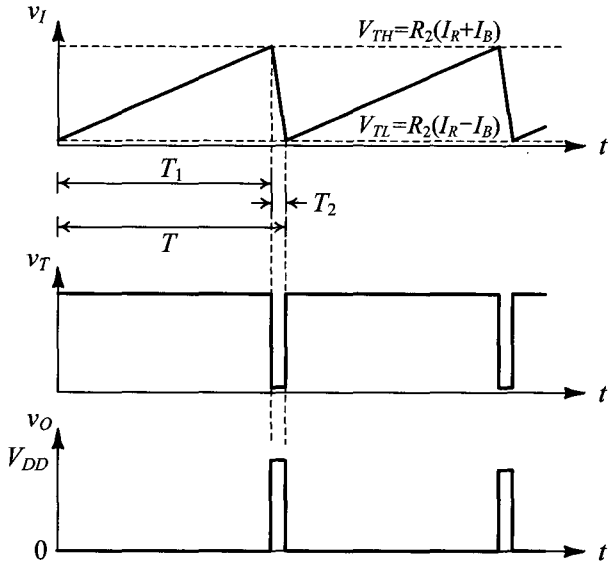

그림 5. 발진기의 다양한 노드에서의 전압 파형
Fig. 5. Voltage waveforms at various nodes of the generator.

have, from Fig. 5,

$$\frac{R_2(I_R+I_{B2})-R_2(I_R-I_{B2})}{T_1}=\frac{I_{B3}}{C} \tag{2}$$

Rearranging the equation gives

$$T_1=2CR_2\frac{I_{B2}}{I_{B3}} \tag{3}$$

When v_I reaches V_{TH}, v_O will switch to the high saturation level, V_{DD}. At this instant, the switch S is closed. This, in turn, rapidly discharges the capacitor C via the switch S. Interval T_2 can be neglected compared to T_1. The oscillation frequency of the generator is

$$f_s=\frac{1}{2CR_2}\frac{I_{B3}}{I_{B2}}. \tag{4}$$

Note that the oscillation frequency of the saw-tooth waveform is directly proportional to the bias currents ratio of the OTAs, I_{B3}/I_{B2}. Their temperature-dependent terms are cancelled out. Thus, neglecting the temperature coefficients of C and R_2, the oscillation frequency is stable against temperature variations.

3. Voltage Reference Circuit

To achieve a stable regulated voltage, the reference voltage of the error amplifier should be independent of the temperature and the supply voltage drift. Fig. 6 shows a typical bandgap reference, which is used in the proposed converter. It is formed using PTAT and CTAT current references. The reference voltage is as follows[11]:

$$V_{REF}=V_{D3}+L\cdot n\cdot \ln M\cdot V_T \tag{5}$$

where V_{D3} is the voltage across the diode D_3, n is the emission coefficient, V_T is the thermal voltage, and M and L imply that M diodes are connected in a parallel manner and L resistors are connected in series, respectively.

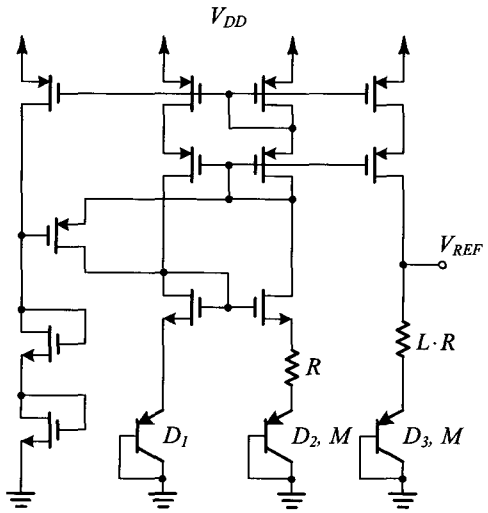

그림 6. 전형적인 밴드갭 레퍼런스 회로도
Fig. 6. Circuit diagram of atypical bandgap reference.

Ⅲ. CMOS OTA

Fig. 7 shows a circuit diagram of a CMOS OTA used in the converter. It consists of a differential pair formed by M_1 and M_2, and three simple current mirrors. The differential pair converts the differential input voltage $v_{IN}(= v_{IN1} - v_{IN2})$ to the currents i_{D1} and i_{D2} which are proportional to the transconductance of the differential pair. Using the simplified square-law relationship for a MOSFET in the saturation region and assuming M_1 and M_2 are perfectly matched, the output current i_{OUT} is given by[12]

$$i_{OUT} = \begin{cases} \sqrt{2I_B K_p} v_{IN} \sqrt{1 - \frac{K_p}{2I_B} v_{IN}^2} & |v_{IN}| \le \sqrt{\frac{I_B}{K_p}} \\ I_B \mathrm{sgn}(v_{IN}) & |v_{IN}| > \sqrt{\frac{I_B}{K_p}} \end{cases} \quad (6)$$

where $K_p = (1/2)\mu_p C_{OX} W/L$, μ_p is the mobility of the carriers, C_{OX} is the gate capacitance per unit area, and W and L are the channel width and the length, respectively.

The CMOS OTA operates linearly only over a limited range of v_{IN}. When the differential input voltage is more than $\sqrt{I_B/K_p}$, its output current becomes saturated as the bias curfent I_B. Differentiating equation (6) with respect to v_{IN} and setting $v_{IN} = 0$ gives the transconductance gain G_m of the OTA, which operates in the linear range as:

$$G_m = \left.\frac{\partial i_{OUT}}{\partial v_{IN}}\right|_{v_{IN}=0} = \sqrt{2K_p I_B} = \sqrt{\mu_p C_{OX} \frac{W}{L} I_B} \quad (7)$$

where μ_p is the temperature-dependent term. Thus, G_m is affected by temperature variations.

Equation (1) shows that the duty cycle D is directly proportional to the transconductance gain of the error amplifier G_{m1}. The temperature stability of G_{m1} affects that of the DC/DC converter. Fig. 8 shows a circuit diagram of a beta-multiplier reference. The reference current I_{REF} is given by[11],

$$I_{REF} = \frac{2}{R^2 \mu_n C_{OX} W_1/L_1} \left(1 - \frac{1}{\sqrt{M}}\right)^2 \quad (8)$$

where $M = W_2/W_1$ and $L_1 = L_2$. Substituting (8) into (7) gives

$$G_m = \frac{1}{R} \sqrt{\frac{2\mu_p}{\mu_n} \frac{W/L}{W_1/L_1}} \left(1 - \frac{1}{\sqrt{M}}\right) \quad (9)$$

Since the mobility variations on the temperature are balanced out in (9), the temperature-stable transconductance gain was obtained by biasing the OTA with the reference circuit shown in Fig. 8. As a result, the regulated voltage of the converter was constantly maintained under temperature drift.

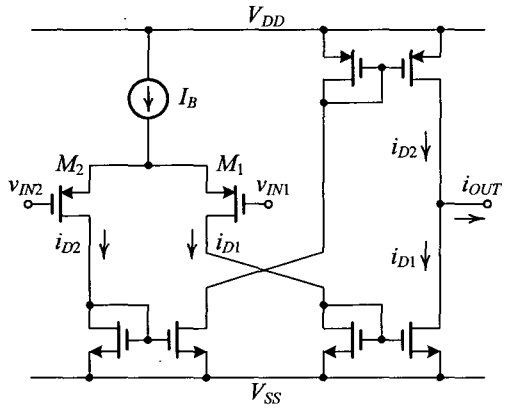

그림 7. CMOS OTA 회로도
Fig. 7. Circuit diagram of a CMOS OTA.

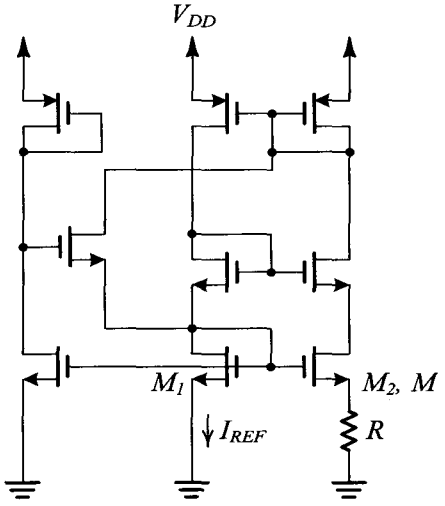

그림 8. 베타 멀티플라이어 레퍼런스 회로도
Fig. 8. Circuit diagram of a beta-multiplier reference.

IV. Simulation Results

The proposed synchronous DC/DC converter shown in Fig. 1 was simulated using HSPICE with 0.35 ㎛ CMOS n-well standard process parameters. The simulation was performed at the supply voltage of V_{IN} = 3.3 V. The values of the external inductor and capacitor were 15 μH and 47 μF, respectively. The reference voltage V_{REF} of 1.24 V was created by the bandgap reference shown in Fig. 6. To obtain the regulated voltage of 1 V, the resistor of the error amplifier R_1 was selected as 21 kΩ. In Fig. 3, to generate the saw-tooth wave with 1 MHz oscillation frequency and 2 V peak-to-peak amplitude, the values of the used elements were as follows: C = 45 pF and R_2 = 12 kΩ. The current I_R was set at 87 μA. The bias currents of the used OTAs were fixed at 85 μA.

When the bias current I_B of the OTA was 85 μA and its load resistance was 100 Ω, the 3-dB frequency was 85 MHz. Fig. 9 shows the temperature characteristics of the uncompensated and the compensated transconductance gains by the current source, shown in Fig. 8. The temperature coefficient of the compensated transconductance gain in the linear region was as low as 150 ppm/°C over 0-100°C.

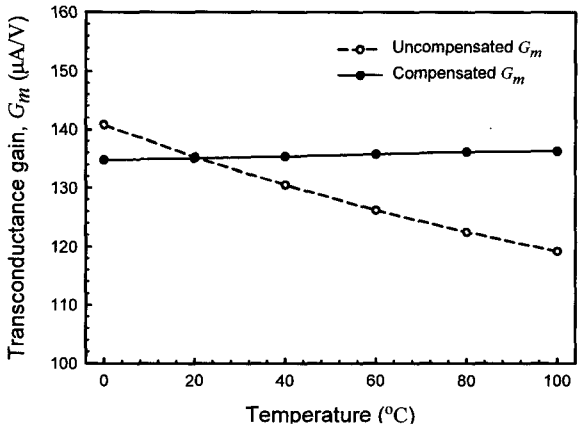

그림 9. 비보상된 트랜스컨덕턴스 이득과 보생된 트랜스컨덕턴스 이득의 온도 특성

Fig. 9. Temperature characteristics of the uncompensated and compensated transconductance gains.

Simulated waveforms of the inductor current, the source-to-drain voltage of *Mp*, and the regulated output voltage at the 100 mA load current are shown in Fig. 10. They show that the proposed DC/DC converter operates properly. Fig. 11 shows the simulated efficiency versus the load current with varying supply voltages. At 3.3 V, the efficiency was more than 80% in the current range of 40-125 mA.

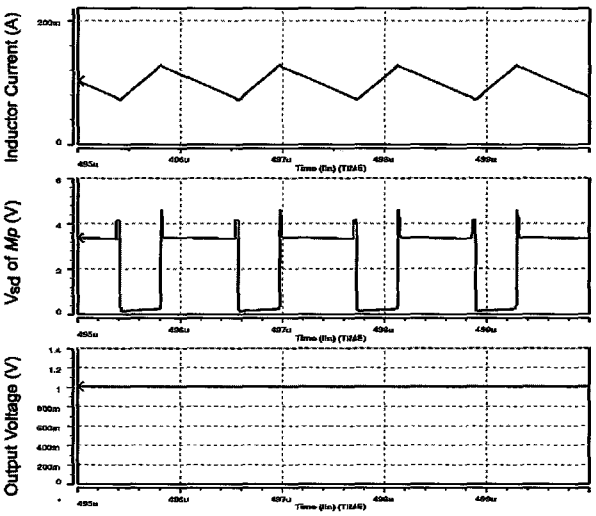

그림 10. 시뮬레이션된 100mA 부하 전류에서의 인덕터 전류, Mp의 소스 드레인간 전압, 그리고 출력 전압 파형

Fig. 10. Simulated waveforms of the inductor current, source-to-drain voltage of Mp, and output voltage at 100 mA load current.

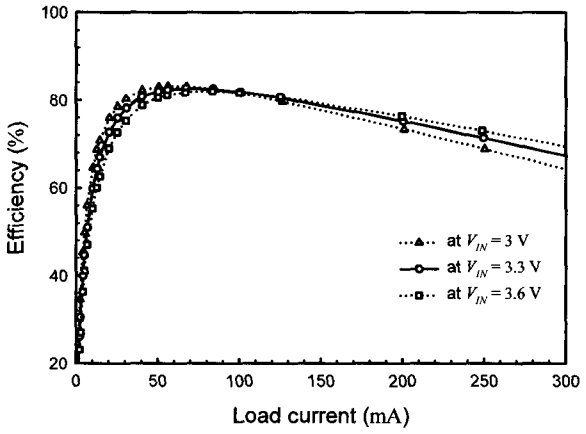

그림 11. 시뮬레이션된 다양한 공급 전압 변화에 따른 효율 대 부하 전류

Fig. 11. Simulated efficiency versus load current with varying supply voltages.

V. Conclusion

This paper presents the Synchronous buck DC/DC converter using CMOS OTAs. Its operation and performance were evaluated using HSPICE simulation. The proposed converter configuration is not only relatively simple but also easily integrates due to using OTAs as circuit-building blocks. It has a high efficiency of more than 80%. As such, it is expected to be used in battery-powered systems. The fabrication of the proposed converter using 0.35 ㎛ standard CMOS process should be the subject of future studies.

References

[1] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power CMOS digital design," *IEEE J. Solid-State Circuits*, vol. 27, no. 4, pp. 473-484, Apr. 1992.

[2] D. Liu and C. Svensson, "Trading speed for low power by choice of supply and threshold voltages," *IEEE J. Solid-State Circuits*, vol. 28, no. 1, pp. 10-17, Jan. 1993.

[3] W. Lau and S. R. Sanders, "An Integrated Controller for a High Frequency Buck Converter," *Proc. IEEE Power Electronics Specialists Conf.*, vol. 1, pp. 246-254, Jun. 1997.

[4] O. Djeki, M. Brokovi, and A. Roy, "High frequency Synchronous Buck Converter For Low Voltage Applications," *Proc. IEEE Power Electronics Specialists Conf.*, vol. 2, pp. 1248-1254, May 1998.

[5] S.-H. Jung, N.-S. Jung, J.-T. Hwang, and G.-H. Cho, "An Integrated CMOS DC-DC Converter for Battery-Operated Systems," *Proc. IEEE Power Electronics Specialists Conf.*, vol. 1, pp. 43-47, July 1999.

[6] A. J. Stratakos, S. R. Sanders, and R. W. Brodersen, "A Low-Voltage CMOS DC-DC Converter for a Portable Battery-Operated System," *Proc. IEEE Power Electronics Specialists Conf.*, vol. 1, pp. 619-626, Jun. 1994.

[7] S. Zhou, and G. A. Rincn-Mora, "A High Efficiency, Soft Switching DC-DC Converter with Adaptive Current-Ripple Control for Portable Applications," *IEEE Trans. Circuits Syst. II: Express Briefs*, Accepted for future publication, 2005.

[8] Y. Sugimoto and S. Kojima, "A 1MHz, Synchronous, Step-down from 3.6 V to 1 V, PWM CMOS DC-DC converter with more than 80% of Power Efficiency," *IEICE Trans. Electron.*, vol. E87-C, no. 3, Mar. 2004.

[9] W. Kursun, V. K. De, E. G. Friedman, and S. G. Narendra, "Monolithic voltage conversion in low-voltage CMOS technologies," *Micro-electronics Journal*, vol. 36, pp. 863-867, Sep. 2005.

[10] W.-S. Chung, H. Kim, H.-W. Cha, and H.-J. Kim, "Triangular/Square-Wave Generator With Independently Controllable Frequency and Amplitude," *IEEE Trans. Instrum. Meas.*, vol. 54, no. 1, pp. 105-109, Feb. 2005.

[11] R. Jacob Baker, *CMOS Circuit design, Layout, and Simulation 2nd Ed.*, IEEE Press Series, A John Wiley & Sons, Inc., 2005.

[12] P. E. Allen, and D. R. Holberg, *CMOS Analog Circuit Design 2nd Ed.*, Oxford Univ. press, New York, 2002.

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