Analytical Noise Parameter Model of Short-Channel RF MOSFETs

Jongwook Jeon, Byung-Gook Park, Jong Duk Lee, and Hyungcheol Shin

Abstract—**In this paper, a simple and improved noise parameter model of RF MOSFETs is developed and verified. Based on the analytical model of channel thermal noise, closed form expressions for four noise parameters are developed from proposed equivalent small signal circuit. The modeling results show a excellent agreement with the measured data of 0.13㎛ CMOS devices.**

Index Terms—**RF MOSFET, analytical modeling, channel thermal noise, small-signal modeling, noise parameters.**

I. INTRODUCTION

Due to continuous reduction of minimum channel length in CMOS technologies in the recent years, CMOS has become a candidate for RF applications[1, 2]. However, when working at high frequencies with short-channel MOSFETs, the noise generated within the device itself is one of the key issues in the low noise RF circuit design[3]. Thus, a physics-based accurate modeling of high-frequency noise of deep-submicron MOSFETs is important for a low noise RF circuit. Channel thermal noise is the most dominant noise source of short-channel MOSFETs in high-frequency[3]. Four noise parameters (NF_{min}, $Y_{opt} = G_{opt} + jB_{opt}$, *and* R_n) are commonly used to specify the noise performance of devices and circuits[4]. The purpose of this work is to develop a new analytical noise parameter model of short channel MOSFETs to give an estimation of the noise performance of RF MOSFETs. The results are based on analysis of each thermal noise source in the MOSFETs. Comparisons were made between the proposed noise model and the measured noise data.

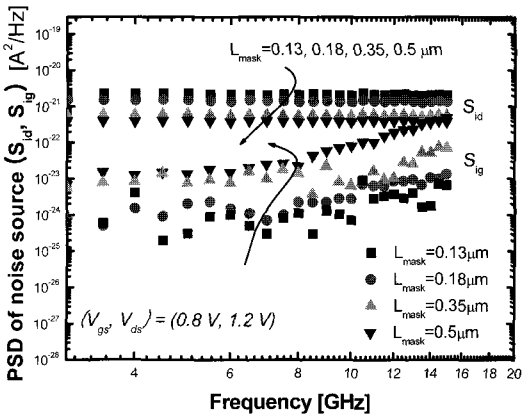

Fig. 1. Measured channel thermal noise and induced gate noise with different gate length.

II. ANALYTICAL MODELING OF THERMAL NOISE AND NOISE PARAMETERS

1. Channel Thermal Noise Model

The thermal fluctuations in a gradual channel region of MOSFET cause the noise current, which is so called channel thermal noise[5]. It is well known that the channel thermal noise becomes larger as the gate length scales down because the channel conductance becomes larger[6]. The devices were fabricated by 0.13㎛ CMOS technology. The unit finger width and the number of fingers were 1.8 ㎛ and 64, respectively. Fig. 1 shows the extracted PSD of each noise source; channel thermal noise and induced gate noise. As shown in Fig. 1, compared with the PSD of channel thermal noise the

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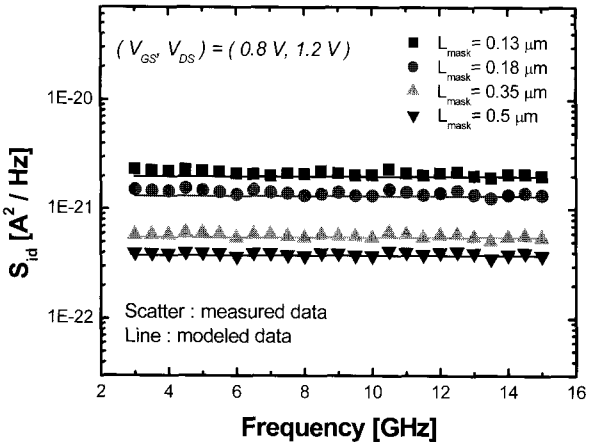


Fig. 2. Measured and modeled channel thermal noise as a function of frequency with different gate lengths.

induced gate noise can be ignored in 0.18 ㎛ or shorter devices. The PSD of the total channel thermal noise is modeled as [7]

$$S_{id} = 4kT_o \cdot \frac{4V_{GT}^2 + 10V_o^2 + 7V_oV_{GT} + \frac{3}{2}\frac{V_o^3}{V_{GT}-V_o}\ln\frac{|2V_{GT}-V_o|}{V_o}}{3(V_{GT}-V_o)(V_{GT}+V_o)^2} mI_{DS} \quad (1)$$

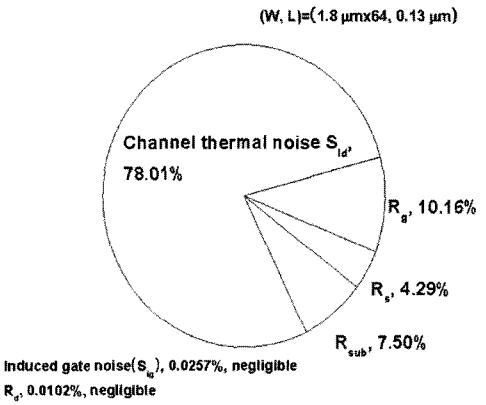
where $V_{GT}=V_{GS}-V_{th}$, and $V_o=I_{DS}/WC_{ox}v_{sat}$. This analytical channel thermal noise model takes into account mobility degradation, channel length modulation and carrier heating effects due to the lateral electric field in short channel MOSFETs. Fig. 2 shows the used channel thermal noise model, eq. (1), accurately predicts each noise current of DUT.

2. Thermal Noise Sources From Parasitic Resistances

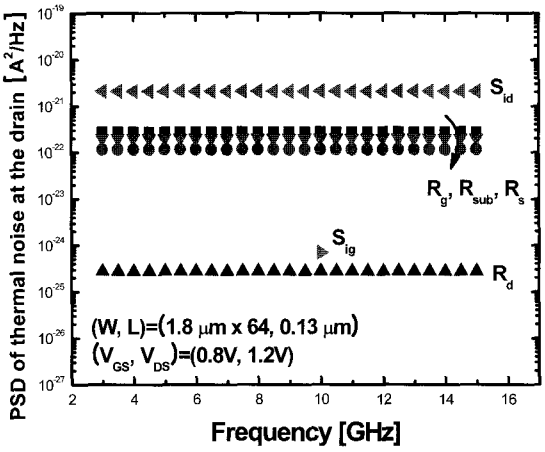
Substrate and gate resistance were obtained by using Y-parameter analysis from S-parameter measurement data. To investigate each contribution of thermal noise sources at the drain output terminal intrinsic g_m, g_{mb} and g_{ds} is needed, which are extracted from S-parameter measurement[8]. Table. 1 shows the summary of extracted device parameters of *0.13㎛* and *0.18㎛* NMOSFET at $V_{GS}=0.8V$ and $V_{DS}=1.2V$. At the drain terminal, PSD of the thermal noise from each resistance in the MOSFET as well as the channel thermal noise is calculated as shown in Fig. 3. The channel thermal noise, noise from the substrate resistance, and noise from the gate resistance are the top three most important noise source in short-channel MOSFETs.

Table. 1. Summary of small signal parameter extraction results at $V_{GS}=0.8V$ and $V_{DS}=1.2V$.

	g_m [mS]	g_{mb} [mS]	g_{ds} [mS]	$R_s=R_d$ [Ω]	R_{sub} [Ω]	R_g [Ω]
0.13 ㎛	86.2	18.1	3.8	1.2	38.5	2.3
0.18 ㎛	71.4	15.6	1.9	1.2	46.5	1.8



(a)



(b)

Fig. 3. (a) The contribution of each thermal noise source at drain output terminal and (b) power spectral density.

3. Noise Parameter Modeling

It is well known that a noisy two port can be represented by the same noiseless two-port network with an input-referred noise voltage source v_n having a PSD of $S_v=4kTR_n$ and an input-referred noise current source i_n having a PSD of $S_i=4kTG_n$ [9]. S_v and S_i depend on the internal physical noise sources and they are, therefore,

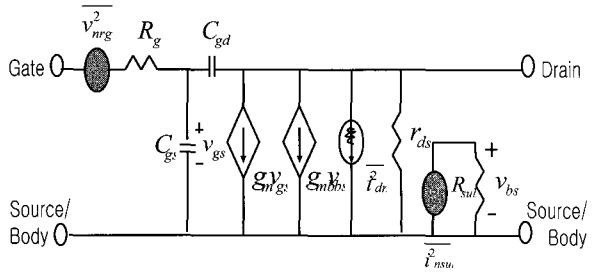


Fig. 4. Small-signal equivalent circuit for noise analysis.

generally correlated. Their cross-correlation can be taken into account by using cross-correlation admittance Y_c defined as

$$Y_c \equiv \frac{\overline{i_n v_n^*}}{\overline{v_n^2}} = G_c + jB_c \tag{2}$$

To characterize noise four parameters we need to formulate following four parameters ; R_n, G_n, G_c, and B_c. Based on the analysis of thermal noise sources of the short-channel MOSFET in section 2 and 3 we propose an improved equivalent small signal circuit of MOSFETs for noise characterization as shown in Fig. 4, which includes channel thermal noise source, substrate, and gate resistance. The equivalent noise voltage(v_n) and current(i_n) source as shown in Fig. 2 are determined as

$$v_n = v_{nrg} + \frac{i_{dn}}{Y_{21}} + \frac{g_{mb}R_{sub}i_{nsub}}{Y_{21}} \tag{3.1}$$

$$i_n = \frac{Y_{11}}{Y_{21}}i_{dn} + \frac{Y_{11}}{Y_{21}}g_{mb}R_{sub}i_{nsub} \tag{3.2}$$

The Y-parameters of the noiseless MOSFET can be obtained from the proposed small-signal circuit shown in Fig. 4 as

$$\begin{aligned} Y_{11} &= \frac{j\omega C_{gg}}{1+j\omega C_{gg}R_g} \\ Y_{12} &= -\frac{j\omega C_{gd}}{1+j\omega C_{gg}R_g} \\ Y_{21} &= \frac{g_m - j\omega C_{gd}}{1+j\omega C_{gg}R_g} \\ Y_{22} &= \frac{1}{r_{ds}} + j\omega C_{gd} + \frac{j\omega C_{gd}R_g(g_m - j\omega C_{gd})}{1+j\omega C_{gg}R_g} \end{aligned} \tag{4.1-4}$$

where $C_{gg}=C_{gs}+C_{gd}$. By using equation (3) and (4) the parameters of R_n, G_n, G_c, and B_c are calculated as

$$R_n \approx R_g + \frac{1}{|Y_{21}|^2}\left(\frac{S_{id}}{4kT} + g_{mb}^2 R_{sub}\right), \quad G_n \approx \frac{|Y_{11}|^2}{|Y_{21}|^2}\left(\frac{S_{id}}{4kT} + g_{mb}^2 R_{sub}\right) \tag{5.1-4}$$

$$G_c \approx \frac{1}{R_n}\left\{\frac{\mathrm{Re}[Y_{11}]}{|Y_{21}|^2}\left(\frac{S_{id}}{4kT} + g_{mb}^2 R_{sub}\right)\right\}, \quad B_c \approx \frac{1}{R_n}\left\{\frac{\mathrm{Im}[Y_{11}]}{|Y_{21}|^2}\left(\frac{S_{id}}{4kT} + g_{mb}^2 R_{sub}\right)\right\}$$

where S_{id} represents the PSD of channel thermal noise and we ignore induced gate noise and its correlation with channel thermal noise based on the analysis in section 2. The four noise parameters including R_n, G_{opt}, B_{opt}, and NF_{min} can be expressed as a function of R_n, G_n, G_c, and B_c[10].

$$\begin{aligned} NF_{\min} &= 1 + 2R_n(G_{opt} + G_c) \\ Y_{opt} &= G_{opt} + jB_{opt} = \sqrt{\frac{G_n}{R_n} - B_c^2} - jB_c \end{aligned} \tag{6.1-2}$$

The four noise parameters, therefore, can be obtained from equation (6) and (5) as following.

$$R_n = R_g + \frac{1}{|Y_{21}|^2}\left(\frac{S_{id}}{4kT} + g_{mb}^2 R_{sub}\right) \approx R_g + \frac{1}{g_m^2}\left(\frac{S_{id}}{4kT} + g_{mb}^2 R_{sub}\right)$$

$$B_{opt} = \frac{\mathrm{Im}[Y_{11}]\cdot\left(S_{id}/4kT + g_{mb}^2 R_{sub}\right)}{|Y_{21}|^2 R_g + S_{id}/4kT + g_{mb}^2 R_{sub}} \approx \left(\frac{f}{f_T}\right)\frac{S_{id}/4kT + g_{mb}^2 R_{sub}}{g_m R_n}$$

$$\begin{aligned} G_{opt} &= \frac{|Y_{11}||Y_{21}|\sqrt{R_g\left(S_{id}/4kT + g_{mb}^2 R_{sub}\right)}}{|Y_{21}|^2 R_g + S_{id}/4kT + g_{mb}^2 R_{sub}} \\ &\approx \left(\frac{f}{f_T}\right)\frac{\sqrt{R_g\left(S_{id}/4kT + g_{mb}^2 R_{sub}\right)}}{R_n} \end{aligned} \tag{7.1-4}$$

$$\begin{aligned} NF_{\min} &= 1 + \frac{2}{|Y_{21}|^2}\left\{|Y_{11}||Y_{21}|\sqrt{R_g\left(S_{id}/4kT + g_{mb}^2 R_{sub}\right)} + \mathrm{Re}[Y_{11}]\left(S_{id}/4kT + g_{mb}^2 R_{sub}\right)\right\} \\ &\approx 1 + 2\left\{\frac{f}{f_T}\sqrt{R_g\left(S_{id}/4kT + g_{mb}^2 R_{sub}\right)}\right\}\left\{1 + \frac{f}{f_T}\sqrt{R_g\left(S_{id}/4kT + g_{mb}^2 R_{sub}\right)}\right\} \end{aligned}$$

where $f_T = g_m/(2\pi C_{gg})$ is the unity gain frequency.

III. EXPERIMENTAL RESULTS

Noise parameters of short-channel MOSFETs obtained from proposed noise parameter equations (7.1-4) are

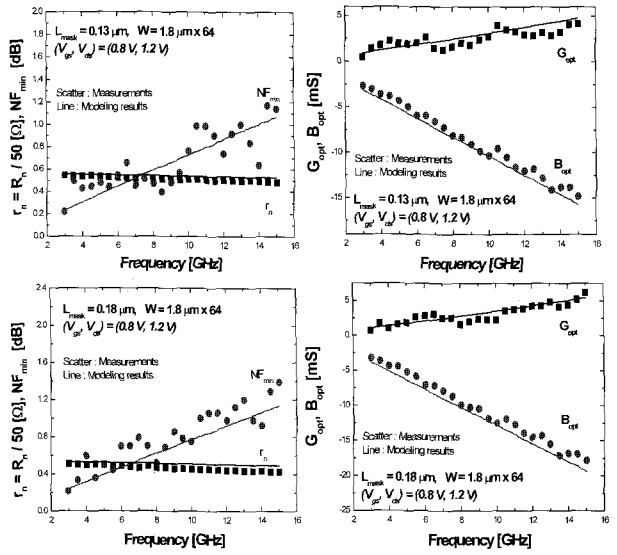


Fig. 5. Measured and modeled noise parameters of MOSFET as a function of frequency with Lmask = 0.13 ㎛ and 0.18㎛.

compared with measured noise parameters. Test devices have *W=1.8 ㎛ x 64*, and *L=0.13 ㎛* and *0.18㎛*. The comparison between predicted and measured MOSFETs noise parameters at V_{GS}=*0.8V* and V_{DS}=*1.2V* versus frequency as shown in Fig. 5. In Fig. 5, we verified the derived noise parameter equations, eq. (7.1-4), are accurate by comparison with the measurements.

IV. CONCLUSIONS

In this paper, new noise parameter equations were proposed and verified with 0.13㎛ RF MOSFETs. Before this task, channel thermal noise modeling and analysis of noise sources from parasitic resistance was performed. Based on the analysis of each noise source, a noise equivalent circuit is proposed. From this circuit, noise parameter equations were derived and verified with measurements. The proposed noise parameter equations accurately predicts noise performance of RF MOSFET. Using the model, the noise performance can be predicted from S-parameter of the device without any noise measurement.

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REFERENCES

[1] E. Morifuji, H. S. Momose, T. Ohguro, T. Yoshitomi, and H. Kimijima, "Future perspective and scaling down roadmap for RF CMOS," *Symp. VLSI Technology*, pp. 163-164, 1999.

[2] J. N. Burghartz, M. Hargrove, C. S. Webster, R. A. Groves, M. Keene, K. A. Jenkins, R. Logan, and E. Nowak, "RF potential of a 0.18-μm CMOS logic device technology," *IEEE Trans. Electron Devices,* vol. 47, no. 4, pp. 864-870, April 2000.

[3] G. Knoblinger, P. Klein, and M. Tiebout , "A new model for thermal channel noise of deep-submicron MOSFETs and its application in RF-CMOS design," *IEEE J. Solid-State Circuits,* vol. 36, pp. 831-837, May 2001.

[4] C. Enz, "An MOS Transistor Model for RF IC Design Valid in All Regions of Operation," *IEEE Trans. Microwave Theory and Techniques,* vol. 50, no. 1, pp. 342-359, Jan. 2002.

[5] H. Shin, S. Kim, and J. Jeon, "Analytical Thermal Noise Model of Deep-submicron MOSFETs," *Journal of Semiconductor Technology and Science*, vol. 5, no. 3, Sept, 2005.

[6] K. Han, H. Shin, and K. Lee, "Analytical drain thermal noise current model valid for deep submicron MOSFETs," *IEEE Trans. Electron Devices,* vol. 51, No. 2, pp. 261-269, Feb. 2004.

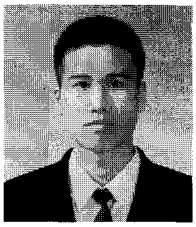
[7] J. Jeon, J. D. Lee, B. G. Park, and H. Shin, " An Analytical Channel Thermal Noise Model for Deep Sub-micron MOSFETs with Short Channel Effects," *Solid-State Electron*, to be published.

[8] I. Kwon, M. Je, K. Lee, and H. Shin, "A Simple and Analytical Parameter Extraction Method of MOSFET for Microwave Modeling," *IEEE Trans. Microwave Theory and Techniques,* vol. 50, no. 6, pp. 1503-1509, June 2002.

[9] T. H. Lee, "The Design of CMOS Radio-Fre quency Integrated Circuits," Cambridge, U.K. : Cambridge Univ. Press, 1998.

[10] S. Asgaran, M. J. Deen, and C. H. Chen, "Analytical Modeling of MOSFETs Channel Noise and Noise Parameters," *IEEE Trans.*

Electron Devices, vol. 51, no. 12, pp. 2109-2114, Dec. 2004.



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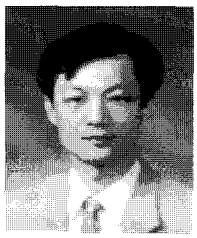

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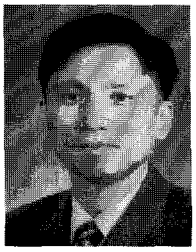

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