Optically Controlled Silicon MESFET Modeling Considering Diffusion Process

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Abstract— **An analytical model is proposed for an optically controlled Metal Semiconductor Field Effect Transistor (MESFET), known as Optical Field Effect Transistor (OPFET) considering the diffusion fabrication process. The electrical parameters such as threshold voltage, drain-source current, gate capacitances and switching response have been determined for the dark and various illuminated conditions. The Photovoltaic effect due to photo-generated carriers under illumination is shown to modulate the channel cross-section, which in turn significantly changes the threshold voltage, drain-source current, the gate capacitances and the device switching speed. The threshold voltage V_T is reduced under optical illumination condition, which leads the device to change the device property from enhancement mode to depletion mode depending on photon impurity flux density. The resulting I-V characteristics show that the drain-source current IDS for different gate-source voltage V_{gs} is significantly increased with optical illumination for photon flux densities of $\Phi = 10^{15}$ and 10^{17} /cm^{2}s compared to the dark condition. Further more, the drain-source current as a function of drain-source voltage V_{DS} is evaluated to find the I-V characteristics for various pinch-off voltages V_P for optimization of impurity flux density Q_{Diff} by diffusion process. The resulting I-V characteristics also show that the diffusion process introduces less process-induced damage compared to ion implantation, which suffers from current reduction due to a large number of defects introduced by the ion implantation process. Further the results show significant increase in gate-source capacitance C_{gs} and gate-drain capacitance C_{gd} for optical illuminations, where the photo-induced voltage has a significant role on gate capacitances. The switching time τ of the OPFET device is computed for dark and illumination conditions. The switching time τ is greatly reduced by optical illumination and is also a function of device active layer thickness and corresponding impurity flux density Q_{Diff}. Thus it is shown that the diffusion process shows great potential for improvement of optoelectronic devices in quantum efficiency and other performance areas.**

Index Terms—**OPFET, MESFET, diffusion, analytical model**

NOTATIONS

k Boltzmann constant,
T Absolute temperature at 300K.
N_C Effective density of states in the conduction band at 300K
N_V Effective density of states in the valence band at 300K
ϵ Permittivity of semiconductor
q Electronic charge
Z Device width
L Channel length
μ_n Electron mobility
μ_p Hole mobility
τ_L Minority carrier lifetime in the illuminated condition
N(y,t) Impurity doping concentration of diffused active layer
N_A Substrate doping concentration

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N_{Davg}	Average channel doping concentration
y_{dg}	Distance from surface to edge of gate depletion region in the channel
y_{ds}	Distance from surface to edge of substrate depletion region in the channel
Y_{SG}	depletion layer width of Schottky contact at the source-end of the gate and
Y_{DG}	depletion layer width of Schottky contact at the drain-end of the gate.
a	active layer thickness
Q_{Diff}	Impurity flux density during diffusion process
Q_{ion}	Ion Implantation dose
D_1	Diffusion constant for diffusion process
D_2	Diffusion constant for post-implanted annealing process
t_1	Diffusion time
t_2	Annealing time
R_P	Implant range parameter
σ_1	Straggle parameters
Φ_{Bn}	Indium tin oxide Schottky barrier height
Δ	Depth of Fermi level below the conduction band
V_{bi}	Built-in voltage
V_{bs}	Substrate-to-source voltage
V_{gs}	Gate-source voltage
V_T	Threshold voltage
V_P	Pinch off voltage
V_{DS}	Drain-source voltage
V_{op}	Photo induced voltage
α	Optical absorption coefficient
Φ	Photon flux density
τ_n	Lifetime of electrons
G	Optical carrier generation rate
V_S	Saturation velocity
R	Surface recombination rate
η	Ideality factor
J_S	Current density

I. INTRODUCTION

In the last few years, optically controlled MESFETs also referred to as OPFETs have received considerable attention due to inherent advantages in high-speed optical switching and high frequency optical modulation/ demodulation applications [1-4]. The radiation of an optical signal from GaAlAs injection laser on GaAs MESFET has demonstrated capabilities of gigabit signal rate modulation [5]. In comparison with other photo detectors such as Avalanche Photo Diodes (APDs), the OPFET device promises to be superior for dispersion measurement on optical fibers with low dispersion and very high speed [6]. Theoretical and experimental observations have shown that the variations of the DC and dynamic properties in MESFETs when a light beam strikes the transistor gate can be accounted for by an appropriate change in the gate junction equivalent to the built-in voltage [7]. In order to establish the OPFET device characteristics, a number of theoretical and experimental observations have been continuously reported [8-14] exploring the illumination effect on the static and dynamic characteristics of MESFET devices for various biases, optical responses of the MESFET both at DC and microwave frequencies and large-signal characteristics of the MESFET under He-Ne illumination source.

In recent years, there has been considerable work done on the development of silicon based optoelectronic integrated circuits (OEIC's) [15-16]. Mature silicon processing technology, including micromachining techniques, can be used to fabricate complex optical structures such as micro-optical devices and hybrid optoelectronics. The silicon based OPFET promises excellent compatibility with current silicon IC technology requiring the same or similar low-cost and reliable manufacturing techniques of monolithic silicon-based OEIC's.

The ion implantation induced defects in a silicon substrate have been characterized by measuring the bulk generation lifetime of MOS capacitor and experiments have been conducted to study the dependence of substrate dopant species (phosphorous and boron) on defect formations [17]. I-V characteristics of ion implanted solar cell devices at optical illumination have shown the efficiency in the range of 0.01%. Phosphorous ion implantation not only results in the transition of the crystalline fullerenes to amorphous material phase, but also produces a significant defect level [18]. An effective loss of photo-generated carriers due to the ion implantation process induced defects in the active channel region of OPFET is a major issue of degradation of quantum efficiency, sensitivity, etc. The channel current obtained from the diffusion and ion implanted OPFET devices are studied and both currents under dark and optical illumination conditions are compared to realize the process-induced defects as major problem for optoelectronics device. This model has adopted the silicon based OPFET device to show the significant impact of process induced

defects (diffusion and ion implantation processes) on device performance. The purpose of this research article is to distill the practical parameters for fabrication by diffusion process. as well as to establish if the diffusion process in substitution of the ion implantation fabrication process can be expected to improve the OPFET device performance, or not. We are in the process of fabricating a practical OPFET device using Synopsys TCAD modeling software to develop optical demodulator in the range of 5-10 gigabit signal rates from a laser source.

II. THEORY ON THE MODEL

A schematic structure of OPFET device is shown in Fig. 1. The transparent gate is made of indium tin oxide (ITO) material to form a Schottky rectifying contact with proper antireflection coating and all optical and electrical parameters of this model are assumed to be the ideal case.

Under optically illuminated condition a one-dimensional Poisson's equation can be expressed in the following form [19]:

$$\frac{d^2\psi(y)}{dy^2} = -\frac{q}{\varepsilon}\left[N(y,t) - G\tau_n\right] \quad (1)$$

The photogenerated carrier at the steady state derived by the following equation [20]:

$$G\tau_n = \alpha\phi\tau_n \exp(-\alpha y) \quad (2)$$

The impurity distribution in the channel is expressed as [21]:

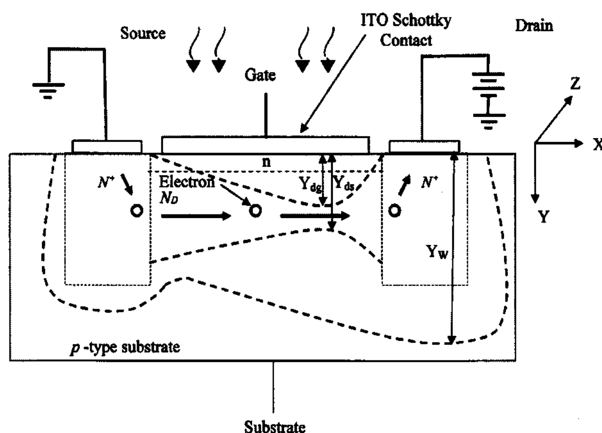

Fig. 1. Cross-sectional view of an OPFET.

$$N(y,t) = \frac{Q_{Diff}}{\sqrt{\pi D_1 t_1}}\exp\left[-\left(\frac{y}{2\sqrt{D_1 t_1}}\right)^2\right] - N_A. \quad (3)$$

The electrical field is determined by integrating equation (1) using the appropriate boundary condition for the electric field at the edge of the depletion width [19].

$$\frac{d\psi(y)}{dy} = \frac{qQ_{Diff}}{\varepsilon}\left\{erf\left(\frac{y_{dg}}{2\sqrt{D_1 t_1}}\right) - erf\left(\frac{y}{2\sqrt{D_1 t_1}}\right)\right\} + \frac{q\phi\tau_n}{\varepsilon}\left\{\exp(-\alpha y_{dg}) - \exp(-\alpha y)\right\} \quad (4)$$

Using the 2nd boundary condition [6], the channel potential at any point between source and drain is obtained by the second integration of the equation (4) as follows:

$$\psi(y) = \frac{qQ_{Diff}\, y}{\varepsilon}\left\{erf\left(\frac{y_{dg}}{2\sqrt{D_1 t_1}}\right) - erf\left(\frac{y}{2\sqrt{D_1 t_1}}\right)\right\} + \frac{2qQ_{Diff}\sqrt{D_1 t_1}}{\varepsilon\sqrt{\pi}}\left\{\exp\left[-\left(\frac{y_{dg}}{2\sqrt{D_1 t_1}}\right)^2\right] - \exp\left[-\left(\frac{y}{2\sqrt{D_1 t_1}}\right)^2\right]\right\} + \frac{q\phi\tau_n}{\varepsilon\alpha}\left\{\exp(-\alpha y) - \exp(-\alpha y_{dg})\right\} + \frac{q\phi\tau_n}{\varepsilon}\exp(-\alpha y_{dg})\left[y - y_{dg}\right] + V(x) - \Delta \quad (5)$$

The above channel potential can be substituted using the 3rd boundary condition for surface potential [6], as follows.

$$V(x) - (V_{GS} - \phi_{Bn} + V_{op}) = \frac{2qQ_{Diff}\sqrt{D_1 t_1}}{\varepsilon\sqrt{\pi}}\left\{1 - \exp\left[-\left(\frac{y_{dg}}{2\sqrt{D_1 t_1}}\right)^2\right]\right\} + \Delta - \frac{qN_A y_{dg}^2}{2\varepsilon} + \frac{q\phi\tau_n}{\varepsilon\alpha}\exp(-\alpha y_{dg}) + \frac{q\phi\tau_n y_{dg}}{\varepsilon}\exp(-\alpha y_{dg}) \quad (6)$$

The indium tin oxide (ITO) Schottky barrier height (Φ_{Bn}) is found to be 0.6 V [22].

When the channel is pinched-off at the drain under certain drain-source biasing conditions, the channel potential relation (6) at the drain under pinch-off condition [19] may be expressed as:

$$V_P - (V_{GS} - \phi_B + V_{op}) = \frac{2qQ_{Diff}\sqrt{D_1 t_1}}{\varepsilon\sqrt{\pi}}\left\{1 - \exp\left[-\left(\frac{y_P}{2\sqrt{D_1 t_1}}\right)^2\right]\right\} + \frac{q\phi\tau_n}{\varepsilon\alpha}\left\{\exp(-\alpha y_P) - 1\right\} + \frac{q\phi\tau_n}{\varepsilon}\exp(-\alpha y_P) y_P + \Delta \quad (7)$$

Using (6) and (7), the following equation is developed for evaluating the channel current in section 2.2.3.

$$V(x)-V_P=\frac{2qQ_{Diff}\sqrt{D_1t_1}}{\varepsilon\sqrt{\pi}}\left\{\exp\left[-\left(\frac{y_P}{2\sqrt{D_1t_1}}\right)^2\right]-\exp\left[-\left(\frac{y_{dg}}{2\sqrt{D_1t_1}}\right)^2\right]\right\}$$
$$+\frac{q\phi\tau_n}{\varepsilon\alpha}\left\{\exp(-\alpha y_{dg})-\exp(-\alpha y_P)\right\}$$
$$+\frac{q\phi\tau_n}{\varepsilon}\left\{\exp(-\alpha y_{dg})y_{dg}-\exp(-\alpha y_P)y_P\right\} \quad (8)$$

1. Threshold Voltage

Using equations (6) or (7) with proper boundary conditions, the threshold voltage is obtained in a similar manner as in [24] and is given by:

$$V_T=\phi_{Bn}-V_{op}-\frac{2qQ_{Diff}\sqrt{D_1t_1}}{\varepsilon\sqrt{\pi}}\left\{1-\exp\left[-\left(\frac{y_{PM}}{2\sqrt{D_1t_1}}\right)^2\right]\right\}$$
$$-\frac{q\phi\tau_n}{\varepsilon\alpha}\left\{\exp(-\alpha y_{PM})-1\right\}-\frac{q\phi\tau_n}{\varepsilon}\exp(-\alpha y_{PM})y_{PM}-\Delta \quad (9)$$

Applying the standard formulae for transformation of exponential function to error function [19] and substituting the error function term given in (32) of Appendix I into (9), the threshold voltage may be derived as:

$$V_T=\phi_{Bn}-V_{op}-\Delta-\frac{2qQ_{Diff}\sqrt{D_1t_1}}{\varepsilon\sqrt{\pi}}\left[1+\frac{2\varepsilon N_A}{qQ_{Diff}^2}(V_{bi}-V_{BS})-2\frac{N_A}{Q_{Dif}}\sqrt{\frac{2\varepsilon}{qN_A}(V_{bi}-V_{BS})}\right]$$
$$-\frac{q\phi\tau_n}{\varepsilon\alpha}\exp\left[-\alpha\left\{1-\frac{N_A}{Q_{Diff}}\sqrt{\frac{2\varepsilon}{qN_A}(V_{bi}-V_{BS})}\right\}-\frac{q\phi\tau_n}{\varepsilon}\left[1-\frac{N_A}{Q_{Diff}}\sqrt{\frac{2\varepsilon}{qN_A}(V_{bi}-V_{BS})}\right]\right]$$
$$\exp\left[-\alpha\left\{1-\frac{N_A}{Q_{Diff}}\sqrt{\frac{2\varepsilon}{qN_A}(V_{bi}-V_{BS})}\right\}\right] \quad (10)$$

The threshold voltage for dark and illumination condition is obtained using above equation and valid for enhancement and depletion FET. The average channel concentration N_{DAvg} obtained from impurity flux density Q_{Diff} and substrate concentration N_A are important fabrication parameters to select the threshold voltage for enhancement and depletion OPFET devices. The average impurity concentration N_{Davg} has been computed by iterative method and incorporated in this model.

The photo-induced voltage developed at the Schottky contact due to the photo-generated carriers can be determined by considering the recombination and process induced defects effect on minority carriers' lifetime [23] as:

$$V_{op}=\frac{\eta kT}{q}\ln\left[\frac{qG\sqrt{\frac{kT\mu_p\tau_L}{q}}-Rq}{J_s}\right] \quad (11)$$

2. I-V Characteristics

Three I-V characteristics under dark and illumination conditions have been computed in this model to study (i) the drain source current (I_{DS}) versus V_{DS} at different V_{GS} to establish the I-V Characteristics of OPFET, (ii) I_{DS} versus V_{DS} for the diffusion and ion implanted OPFET devices at constant V_{GS} to study the effects of ion implantation and diffusion process induced defects/ damages and (iii) I_{DS} versus V_{DS} for different V_P and Q_{Diff} to optimize the active channel depth and doping impurity concentration. The drain-source current is determined by integrating the channel charge between the source and drain [24] as:

$$I_{DS}=\frac{q\mu_nZ}{L}\int_0^{V_{DS}}Q_n(V)dV \quad (12)$$

Where $Qn(V)$ is the total mobile charge carrier in channel.

The channel charge carrier density may be expressed by considering total charge carrier density under optical illumination [13]:

$$Q_n(V)=Q_{Diff}\left[erf\left(\frac{y_{ds}}{2\sqrt{D_1t_1}}\right)-erf\left(\frac{y_{dg}}{2\sqrt{D_1t_1}}\right)\right]$$
$$+\phi\tau_n\left[1-\exp(-\alpha y_{dg})\right] \quad (13)$$

2.1 I-V characteristics for gate-source biasing using ion implantation process

The error function terms given in (29) and (33) of Appendix I are substituted into (13) and integrating (12), the drain-source current for various gate biasing is obtained as follows:

$$I_{DS}=\frac{qu_nZQ_{Diff}}{L}\left\{V_{DS}-\frac{2}{3Q_{Diff}}\sqrt{\frac{2N_A\varepsilon}{q}}\left\{\left[V_{DS}+V_{bi}-V_{BS}\right]^{\frac{3}{2}}-\left[V_{bi}-V_{BS}\right]^{\frac{3}{2}}\right\}\right.$$
$$\left.-\frac{2}{3\sqrt{A}}\left\{\left[V_{DS}+\phi_B-V_{GS}-\Delta-V_{op}\right]^{\frac{3}{2}}-\left[\phi_B-V_{GS}-\Delta-V_{op}\right]^{\frac{3}{2}}\right\}\right\}$$
$$+\frac{qu_nZQ_{Diff}}{L}\phi\tau_n\left[1-\exp(-\alpha y_{dg})\right]\times V_{DS} \quad (14)$$

The above equation expresses the ideal I-V characteristics of an OPFET device under dark and illuminated condition for different gate biasing and supports both enhancement and depletion mode devices.

2.2 I-V characteristics for gate-source biasing using ion implantation process

A derivation of I-V characteristics for ion implanted OPFET devices considering the annealing effects and other related process parameters [25] is determined by again integrating (12) using charge carrier density and the drain-source current of an ion implanted OPFET device is obtained as:

$$I_{DS}=\frac{qQ_{ion}\mu Z}{L}\left[\begin{array}{l} V_{DS}(1+\alpha)-\frac{2qN_A^2}{3Q_{ion}\varepsilon}\left[\left(\frac{2\varepsilon}{qN_A}\right)(V_{bi}-V_{BS}+V_{DS})\right]^{3/2}+\frac{2qN_A^2}{3Q_{ion}\varepsilon}\left[\left(\frac{2\varepsilon}{qN_A}\right)(V_{bi}-V_{BS})\right]^{3/2} \\ -\frac{qQ_{ion}\sigma}{3\varepsilon}\sqrt{\frac{2}{\pi}}\left[\alpha^2-2\alpha C_1+C_1^2+R(V_{DS}-V_{GS}+\phi_B-\Delta-V_{op})\right]^{3/2} \\ +\frac{qQ_{ion}\sigma}{3\varepsilon}\sqrt{\frac{2}{\pi}}\left[\alpha^2-2\alpha C_1+C_1^2+R(V_{GS}+\phi_B-\Delta-V_{op})\right]^{3/2} \end{array}\right] \tag{15}$$

Where

$\sigma=\sqrt{(\sigma_i^2+2D_2t_2)}$, $R_P^*=R_P+K\Delta Y_j$, $\alpha=\frac{R_P^*}{2\sigma}\sqrt{\frac{\pi}{2}}$, $R=\frac{\varepsilon\sqrt{2\pi}}{qQ_{ion}\sigma}$,

$C_1=erf\left(\frac{R_P^*}{\sigma\sqrt{2}}\right)$, and $C_2=V-V_{GS}+\phi_B-\Delta-V_{op}$, ΔY_j = Change in the junction depth due to post-implantation annealing and K≈ 0.5 [26].

2.3 I-V characteristics for various pinch-off voltage using diffusion process

The drain-source current for different pinch-off voltages are computed under dark condition by substituting the error function terms given in (29) and (33) in Appendix I into (13) as:

$$\begin{aligned} I_{DS}=\frac{q\mu_n ZQ_{Diff}}{L}&\left\{V_{DS}-\frac{2}{3}\sqrt{\frac{2\varepsilon}{qN_A}}\left\{[V_{DS}+V_{bi}-V_{BS}]^{\frac{3}{2}}-[V_{bi}-V_{BS}]^{\frac{3}{2}}\right\}\right. \\ &-\frac{1}{3}\sqrt{(V_{DS}-D)C^2-2\sqrt{(V_{DS}-D)}C+B+AV_{DS}+1} \\ &\left(-\frac{\sqrt{(V_{DS}-D)}C}{C^2+A}+\frac{2DA^2+2(DC^2+B+1)A+(2B-1)C^2}{(C^2+A)^2}+2(V_{DS}-D)\right) \\ &+\frac{1}{(C^2+A)^{5/2}}(C(DA^2+(DC^2+B+1)A+BC^2)\log(\frac{1}{\sqrt{(C^2+A)}}(2(\sqrt{(V_{DS}-D)}C^2 \\ &\left.-C+A\sqrt{V_{DS}-D}+\sqrt{C^2+A}\times\sqrt{(V_{DS}-D)C^2-2\sqrt{(V_{DS}-D)}C+B+AV_{DS}+1}))))\right\} \end{aligned} \tag{16}$$

Where:

$A=\frac{4q^2Q^2_{Diff}D_1t_1}{\varepsilon^2\pi}$, $B=-\frac{V_p\varepsilon\sqrt{\pi}}{2qQ_{Diff}\sqrt{D_1t_1}}$, $C=\frac{N_A}{Q_{Diff}}\sqrt{\frac{2\varepsilon}{qN_A}}$, and $D=V_{BS}-V_{bi}$

The above equation reflects the various diffusion process parameters to optimize OPFET pinch off voltage, which is evident from the following equation [27]

$$Q_{Diff}=\frac{2V_P\varepsilon}{q}\sqrt{\frac{\pi}{D_1t_1}} \tag{17}$$

3. Internal Gate Capacitance before Pinch-Off Region

The space charge distribution in the gate depletion region in an OPFET is calculated based on charge distribution shown in Fig. 2. In order to show the optical illumination effects on gate capacitance, the space charge in the gate depletion of the OPFET is divided by three defined sections I, II and III carrying the charges Q_1, Q_2 and Q_3 respectively. The simulation process of gate capacitance based on three charges for different gate regions before pinch-off condition agrees well with two-dimensional analyses for short channel MESFETs [28]. The gate charge Q_1 confined in region I of the gate can be expressed by the following equation [29]:

$$Q_1=qZL\int_0^{Y_{DG}}[N(y)-G\tau_n]dy-\frac{qZL}{Y_{DG}-Y_{SG}}\int_{Y_{SG}}^{Y_{DG}}[N(y)-G\tau_n](y-Y_{SG})dy \tag{18}$$

The charge Q_2 in section II is expressed by:

$$Q_2=\frac{\pi}{2}\varepsilon Z(V_{bi}-V_G+V_S) \tag{19}$$

The charge Q3 in section III can be evaluated as:

$$Q_3=\frac{\pi}{2}\varepsilon Z(V_{bi}-V_G+V_D) \tag{20}$$

The total gate-source capacitance expressed by the following equation is obtained by substituting (2) and (3) into (18) and adding the side-wall capacitance from (19) and (20):

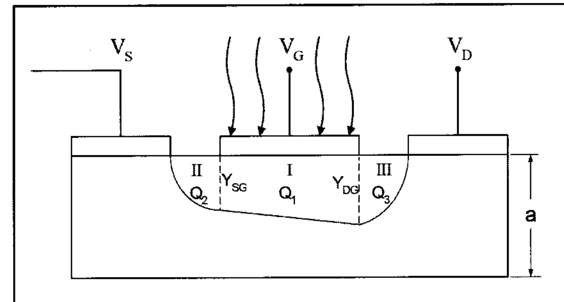

Fig. 2. Internal space charge distribution before pinch off region.

$$C_{GS}=\frac{qZLQ_{Diff}}{2\sqrt{A}}\left[\frac{V_2/\sqrt{V_1}-2\sqrt{V_2}+\sqrt{V_1}}{\left(\sqrt{V_2}-\sqrt{V_1}\right)^2}\right]+\frac{qZLQ_{Diff}S\sqrt{D_1t_1}}{2A\sqrt{\pi}}\left[\frac{V_{DS}/\sqrt{V_1}}{\left(\sqrt{V_2}-\sqrt{V_1}\right)^2}\right]-\frac{qZL\,\tau_n\phi S}{2\alpha}\left[\frac{\left(\left\{e^{-\frac{\alpha}{S}\sqrt{V_2}}+e^{-\frac{\alpha}{S}\sqrt{V_1}}\right\}/\sqrt{V_1}\right)+\frac{\alpha}{S\sqrt{V_1}}e^{-\frac{\alpha}{S}\sqrt{V_1}}\left(\sqrt{V_2}-\sqrt{V_1}\right)}{\left(\sqrt{V_2}-\sqrt{V_1}\right)^2}\right]+\frac{\pi\varepsilon Z}{2} \tag{21}$$

Similarly, we can also derive the following equation for total gate-drain capacitance:

$$C_{GD}=\frac{qZLQ_{Diff}}{2\sqrt{A}}\left[1/\sqrt{V_2}\right]+\frac{qZLQ_{Diff}S\sqrt{D_1t_1}}{2A\sqrt{\pi}}\left[\frac{2\sqrt{V_1}-\sqrt{V_2}-V_1/\sqrt{V_2}}{\left(\sqrt{V_2}-\sqrt{V_1}\right)^2}\right]-\frac{qZL\,\tau_n\phi S}{2\alpha}\left[\frac{2\sqrt{V_2}e^{-\frac{\alpha}{S}\sqrt{V_2}}+\frac{\alpha}{S}e^{-\frac{\alpha}{S}\sqrt{V_2}}\left(\sqrt{V_2}-\sqrt{V_1}\right)+\left(\left\{e^{-\frac{\alpha}{S}\sqrt{V_2}}-e^{-\frac{\alpha}{S}\sqrt{V_1}}\right\}/\sqrt{V_2}\right)}{\left(\sqrt{V_2}-\sqrt{V_1}\right)^2}\right]+\frac{\pi\varepsilon Z}{2} \tag{22}$$

Where $S=\sqrt{\frac{qN_{Davg}}{2\varepsilon}}$, $V_1=\phi_B+V_{GS}-\Delta-V_{op}$ and $V_2=\phi_B+V_{DS}-V_{GS}-\Delta-V_{op}$

4. Switching Characteristics

The switching time of an OPFET depends on the active channel thickness and corresponding impurity flux density of the diffusion process. The switching time τ is computed for different active layer thickness expressed by the following equation [30]:

$$\tau=\frac{L(\phi_{Bn}-V_{OP}-V_{GS})^{1/2}}{V_S\left[\left(\frac{qN_{DAVG}a^2}{2\varepsilon}\right)^{1/2}-(\phi_{Bn}-V_{OP}-V_{GS})^{1/2}\right]} \tag{23}$$

Finally, the switching time τ as a function of impurity flux density Q_{Diff} can be expressed by following equation:

$$\tau=\frac{L(\phi_{Bn}-V_{op}-V_{GS})^{1/2}}{V_S\left[\left(\frac{Q_{Diff}q\sqrt{D_1t_1}}{2\varepsilon\sqrt{\pi}}\right)^{1/2}-(\phi_{Bn}-V_{OP}-V_{GS})^{1/2}\right]} \tag{24}$$

Reflected in the above equations is the key to understanding the switching response of the OPFET device in relation to various active channel thicknesses formed via selective impurity flux density by diffusion process.

III. Numerical Calculations, Results and Discussions

The results based on numerical calculations are presented here to evaluate the characteristics of threshold voltage, drain-source currents, gate-capacitances and switching response of a diffusion process based OPFET device under dark and illumination conditions in order to study the optical demodulation characteristics. I-V characteristics of diffusion and ion implanted OPFET devices are intensively studied to justify better fabrication processes to enhance the optoelectronic device performance.

Equation (10) is derived to compute the threshold voltage V_T under dark and illuminated conditions illustrated in Fig. 3. The plot shows the threshold voltage as a function of impurity flux density Q_{Diff} for substrate concentrations $N_A = 10^{12}/cm^2$ under dark and optical illumination with photon flux densities of $\Phi = 10^{15}$ and $10^{17}/cm^2s$. The graph shows that the threshold voltage is linearly decreasing with respect to an increase in impurity flux density ($0.5x10^{12}$ – $2x10^{12}/cm^2$). As a result, the OPFET device can behave as an enhancement FET for certain low impurity flux densities and depletion FET for certain high impurity flux densities in the dark condition. The threshold voltage of the OPFET can be selectively adjusted by simply changing the impurity flux density during diffusion process. The threshold voltage V_T at dark condition shifts more negative due to the effect of optical illumination with photon flux densities of $\Phi = 10^{15}$ and $10^{17}/cm^2s$. The photo-generated carriers under optical illumination cause a significant threshold shift to larger negative values to make the device behave as a depletion FET device irrespective to doping concentration. The calculated value of photo-induced voltage V_{OP} is found to be approximately in the range of 0.29 V to 0.39 V for impurity flux densities of 10^{15} and 10^{17} $/cm^2$ respectively. In the present device modeling, the threshold voltage is chosen to be about -1.2V for impurity flux density $Q_{Diff} = 10^{12}/cm^2$ at

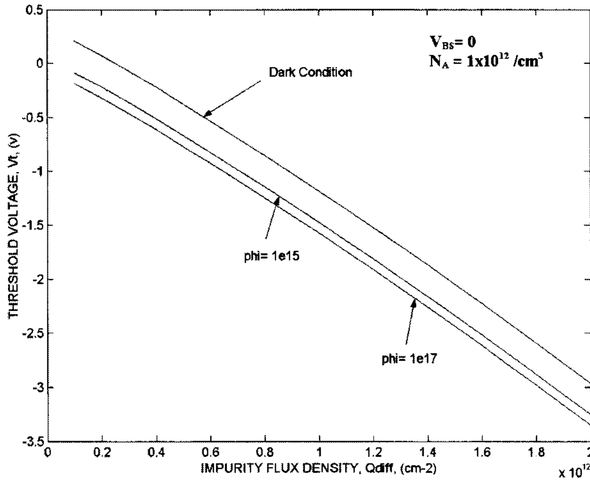

Fig. 3. Threshold Voltage V_T as a function of impurity flux density Q_{Diff} for dark and optical illumination conditions.

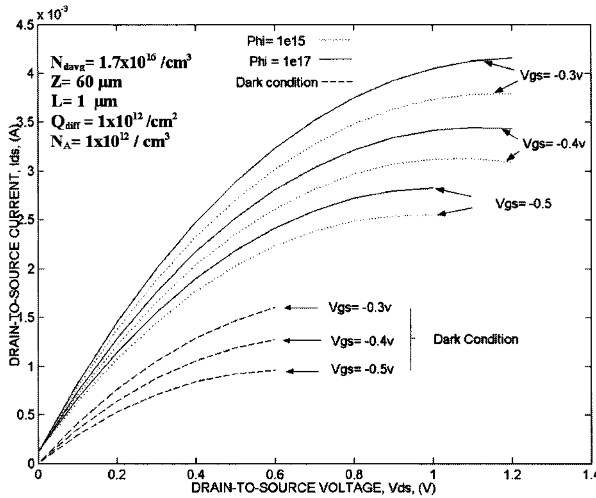

Fig. 4. Drain-source current I_{DS} versus drain-source voltage V_{DS} for different gate-source voltage V_{gs} under dark and optical illumination ($\Phi = 10^{15}$ and 10^{17}/cm^2.s) conditions.

dark condition, where the threshold voltages are shifted to about -1.49V and -1.51V at the optical illumination condition with photon flux densities of $\Phi = 10^{15}$ and 10^{17}/cm^{2}s respectively. The gate depletion width is changed significantly by the optical signal due the photo-induced voltage, which in turn changes the threshold voltage of OPFET efficiently working as optical demodulator.

Equation (14) is derived to show the ideal I-V characteristics of the OPFET for different gate-source voltage under dark and illumination conditions and is illustrated in Fig. 4. The three drain-source currents for V_{GS} = -0.3, -0.4 and -0.5 V are found to follow the I-V characteristics of the OPFET under dark condition with the saturation current limits in the approximate range of 1.6, 1.3 and 0.9 mA, respectively. The drain-source currents under optical illumination with photon flux densities of $\Phi = 1\text{x}10^{17}$ and $1\text{x}10^{15}$/cm^{2}s significantly increase and saturate at approximately 4.2, 3.4 and 2.8 mA and 3.8, 3.1 and 2.6 mA respectively for the same set of gate-source voltages. It is evident from the plot that the drain-source current under optical illumination condition is increased by more than 150% compared to the drain-source current under dark condition. The optical radiation on the gate reduces the gate depletion region evident from the threshold voltage reduction, which in turn significantly increases the pinch off voltage to enhance the channel cross section area. As a result, the drain-source current of the OPFET will increase and this property of the OPFET will behave as an effective optical demodulator.

Ion implantation damage models explicitly show the damage production, damage de-channeling, defect diffusion and reactions and crystal amorphization [31]. The post-implant annealing process is critical and produces the well known effect of extended defect formations, which affect the photo-generated carriers as an additional charge in the active region trapped by the defect centers resulting in quantum efficiency loss and stability degradation for optoelectronic devices. A realistic value of ion implantation process induced defect density obtained elsewhere is considered in the calculation of photo-induced voltage in equation (15). Using the equations (14) and (15), Fig. 5 shows a plot of drain-source current I_{DS} versus drain-source voltage V_{DS} for different gate-source voltages V_{GS} of both diffusion and ion implanted OPFET devices. The saturated drain-source current I_{DS} of diffusion and ion implanted OPFET devices under dark condition are intentionally kept nearly the same in order to better contrast to I-V characteristics under illumination condition. Both devices saturate at about 1.6mA by considering the same physical device dimensions, substrate concentration, channel concentration of ion implanted device $N_{Davg(ion)} = 1.9\times10^{16}$/cm^3 for ion dose $Q_{ion} = 1.37\times10^{12}$/cm^2 and channel concentration of diffusion processed device $N_{Davg(Diff)} = 1.7\times10^{16}$/cm^3 for impurity flux density $Q_{Diff}=1\times10^{12}$/cm^2. At the illuminated condition with photon flux density of $\Phi = 1\times10^{17}$/cm^{2}s, the drain-source current I_{DS} of the diffusion and ion implanted OPFETs saturate at about 3.7mA and 2.3mA respectively. As a result, the current of a diffusion process based device is enhanced

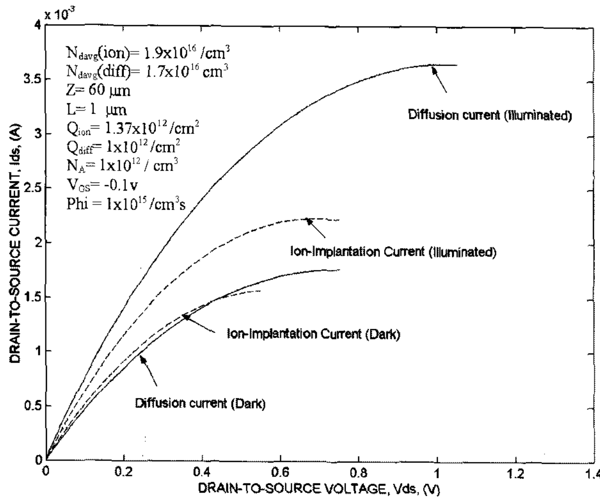

Fig. 5. Drain-source current I_{DS} versus drain-source voltage V_{DS} for diffusion and ion implantation process at constant gate-source voltage under dark and illumination conditions.

by more than 50% compared to an ion implanted OPFET device, which is evident of the loss of photo-generated carriers by the ion implantation process induced defects centers in the active channel region.

Fig. 6 depicts the I-V characteristics of an OPFET for various pinch-off voltages V_P and corresponding impurity flux densities (Q_{Diff}) under dark condition calculated from (16). The drain-source current saturates at about 0.25mA for the pinch-off voltage of about 0.35V. Estimation of the physical active layer thickness can be obtained from the average impurity concentration N_{Davg} of the channel region using the corresponding impurity flux density Q_{Diff}=9.06 × 10^{11}/cm^2. Similarly, other drain-source currents are found to be saturating at approximately 1.5 and 5.4mA for pinch-off voltages V_P = 0.8 and 1.5V respectively and the corresponding active channel thicknesses can be selectively formed by depositing impurity flux densities of Q_{Diff} = 2.07×10^{12} and 3.9×10^{12}/cm^2 respectively by diffusion process. With respect to the relationships between pinch-off voltage, active layer thickness and optical signal penetration depth, the plot gives valuable information to be used for: (i) optimization of physical active layer thickness, (ii) estimation of impurity diffusion flux density and (iii) optimization of diffusion times and temperatures of the diffusion process.

The calculated result for gate-source capacitance obtained from (21) is illustrated in Fig. 7, which shows the characteristics of gate-source capacitance C_{GS} as a function of various gate-source voltages V_{GS} for dark condition

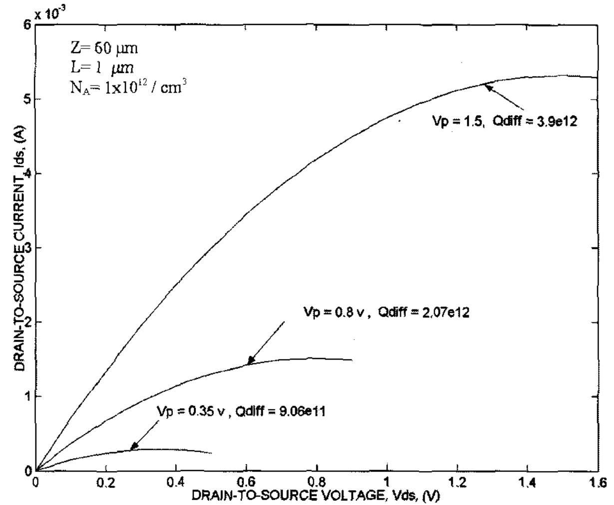

Fig. 6. Drain-source current I_{DS} versus drain-source voltage V_{DS} for pinch off voltage V_p and corresponding impurity flux densities Q_{Diff}.

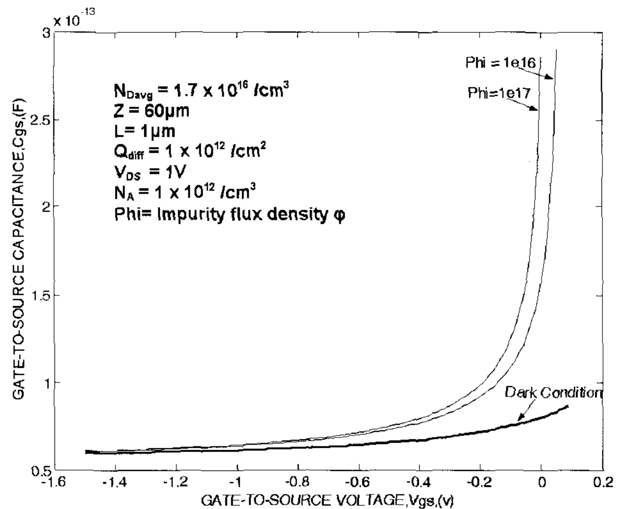

Fig. 7. Gate-to-source capacitance versus gate-to-source voltage for dark and optical illumination conditions.

and for optical illuminations with photon flux densities of Φ = 1×10^{16} and 1x10^{17}/cm^{2}s at constant drain-source voltage V_{DS} = 1V. The variation of the gate-source capacitance C_{GS} with respect to gate-source biasing V_{GS} in dark and illuminated conditions reveals that the gate-source capacitance increases with respect to a positive increase in negatively biased gate-source voltage V_{GS}. Under optical illumination conditions, the gate-source capacitance C_{GS} is initially increasing with low slope for V_{GS} = -1.5 to -0.2V and rises very sharply up to approximately 2.8×10^{-13}F as V_{GS} approaches 0V, where as the gate-source capacitance C_{GS} under dark condition also increases very slowly up to approximately 0.8×10-

^{13} F between the gate-source voltage V_{GS} = -1.5 to 0V. It is evident from the plot that the gate-source capacitance C_{GS} under optical illuminated condition at 0V is suddenly increased due to the additional charges from the optically generated carriers.

Fig. 8 is the computed result of gate-drain capacitance C_{GD} versus drain-source voltages V_{DS} for constant gate-source voltages V_{GS} = -0.5V under dark and illuminated conditions obtained from (22). The plot shows that the gate-drain capacitances C_{GD} under both dark and illumination conditions decreases with respect to an increase in drain-source voltage V_{DS}.

At drain-source voltage V_{DS} = 0V, the gate-drain capacitances C_{GD} is approximately 4.9×10^{-14} and 4.7×10^{-14} F under photon flux density of $\Phi = 1\times10^{17}$ and 1×10^{16} /cm^2·s respectively, which is relatively large compared to values at dark condition. As the drain-source voltage approaches V_{DS} = 1.5V, both the gate-drain capacitances C_{GD} under the illuminated condition drop to approximately 2.97×10^{-14} – 2.95×10^{-14} F respectively, whereas the gate-drain capacitances C_{GD} for dark condition drops up to approximately 2.8×10^{-14} F. However, the difference between the gate-drain capacitances C_{GD} for illumination and dark conditions at high drain-source biasing is effectively smaller compared to low drain-source voltage. The large difference in gate-drain capacitances C_{GD} between optical illumination and dark conditions at low V_{DS} occurs due to the additional charge developed by the photo-induced voltage V_{OP}, which is a major contributor to total charge carriers at low drain-source voltage.

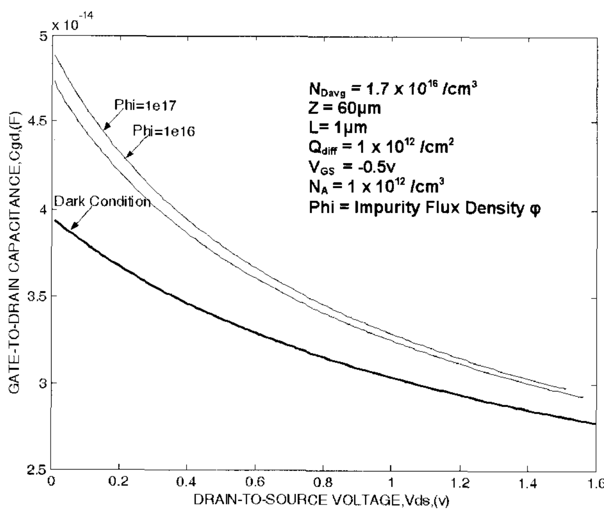

Fig. 8. Gate-to-drain capacitance versus drain-to-source voltage for dark and optical illumination conditions.

Equation (23) is used to compute the switching time τ as a function of the device active layer thickness *a* for dark and optical illumination conditions. The computed result illustrated in Fig. 9 shows that the switching time of 0.87×10^{-10} sec under dark condition abruptly decreases with respect to increasing device active layer thickness from about 0.25 to 0.4×10^{-4} cm. The switching time is also reduced under optical illumination condition, especially at device active layer thicknesses below 0.4×10^{-4}cm. The switching time τ for a device active layer thickness of 0.24×10^{-4}cm abruptly decreases from 0.88×10^{-10}s under dark condition to 0.10×10^{-10}s and 0.16×10^{-10}s for optical illumination with photon flux densities of $\Phi = 10^{15}$ and 10^{17}/cm^{2}s respectively, an increase in switching speed of over 600%. Therefore it is observed that the transition from dark to illuminated condition of the OPFET significantly changes the switching time for certain device active layer thicknesses. However, the results results represented by the plot match well with other author's computed results on switching time versus device active layer thickness [11].

The characteristics of switching time as a function of impurity flux density have been determined by using the equation (24) and the plot is illustrated in Figure 10. The switching time is shown to be abruptly decreasing for impurity flux densities less than and approaching about 1×10^{13}/cm^2, and still decreasing but less dramatically with respect to continued increase in impurity flux density. The plot indicates that the switching characteristics change

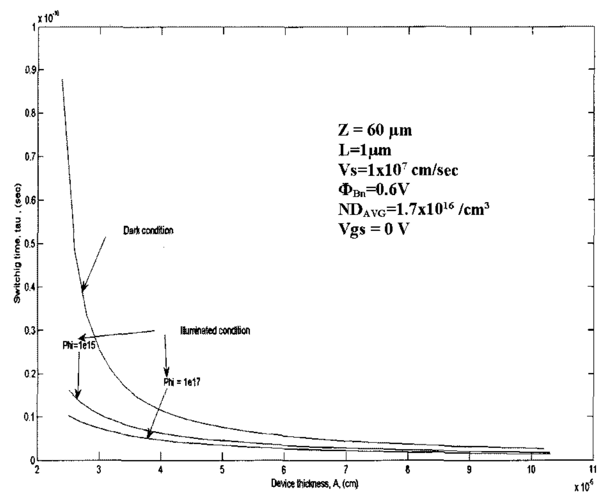

Fig. 9. Calculated switching time τ versus Active layer thickness for dark and optical illumination condition.

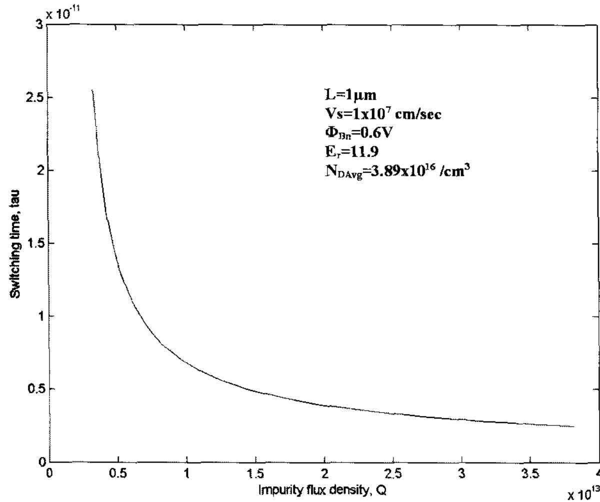

Fig. 10. Computed switching time τ versus impurity flux density Q_{diff}.

with low, moderate and high impurity deposition on the silicon during diffusion process. Most of the optically generated carriers should originate within the Schottky depletion region (gate depletion) for both high quantum efficiency and high switching speed, and in addition, the depletion region must not be so wide that the transit time of the carriers limits the frequency response. Therefore, it is essential to study the gate depletion and channel doping concentration through the active channel thickness, pinch-off voltage and impurity flux density associated with diffusion process fabrication. The plots on switching characteristics shown in Fig. 9 and 10 are very important when considering the fabrication process, estimation of physical active layer thickness, and optical signal penetration depth for improvement of optoelectronic device switching response.

IV. CONCLUSIONS

The analytical model of the OPFET presented here includes the effect of optical illumination on the threshold voltage, drain-source current, gate capacitance and switching time. The transition between dark and illuminated condition contributes to a major threshold voltage shift resulting in significant changes to device properties. The selective impurity flux density is very attractive process feature to fabricate enhancement and depletion OPFET devices. The drain-source current under optical illumination condition is significantly increased compared to the dark condition. The drain-source currents obtained from the diffusion and ion implanted OPFET device shows the influence of ion implanted process-induced defects on the photo-generated carriers causing channel current degradation. I-V characteristics of an OPFET device for different pinch-off voltages were found to be very useful to estimate the active channel layer thickness and to optimize the diffusion fabrication process parameters. The gate-source and gate-drain capacitances under illuminated condition increase significantly at low gate-source voltage due to the influence of photo-induced voltage. The switching time of the OPFET device with lower active channel thickness under dark condition is found to be improved compared to the optically illuminated condition. Low impurity flux densities in the diffusion process enhance the switching time of the OPFET device. An intensive study on different electrical parameters and resultant device performance shows that the OPFET device has a strong potential to demodulate gigabit signal rates from a laser source. The present analytical model offers an avenue of accurate optimum device and fabrication process design as well as establishment of the diffusion process as most suitable for optoelectronic devices fabrication.

APPENDIX I

Considering the fact that the electric field $E = 0$ at both sides of the junction formed by n-channel and p-substrate, which is equivalent to

$$\int_{y_{ds}}^{y_w} N(y)dy = 0 \tag{25}$$

Substitution (3) into (45) yields

$$erf(\frac{y_w}{2\sqrt{D_1 t_1}}) - erf(\frac{y_{ds}}{2\sqrt{D_1 t_1}}) = \frac{N_A}{Q_{Diff}}(y_w - y_{ds}) \tag{26}$$

The condition $y_w >> 2\sqrt{D_1 t_1}$ will be assumed to hold and so the error function approximation is derived as

$$erf\left(\frac{y_w}{2\sqrt{D_1 t_1}}\right) \cong 1 \tag{27}$$

From the abrupt junction relationship, we can write

the following equation as:

$$y_w - y_{ds} = \sqrt{\frac{2\varepsilon}{qN_A}(V(x) + V_{bi} - V_{BS})} \qquad (28)$$

Substitution of (47) and (48) into (46) yields

$$erf(\frac{y_{ds}}{2\sqrt{D_1 t_1}}) = 1 - \frac{N_A}{Q_{Diff}}\sqrt{\frac{2\varepsilon}{qN_A}(V(x) + V_{bi} - V_{BS})} \qquad (29)$$

Using pinch-off condition also yields:

$$erf(\frac{y_P}{2\sqrt{D_1 t_1}}) = 1 - \frac{N_A}{Q}\sqrt{\frac{2\varepsilon}{qN_A}(V_P + V_{bi} - V_{BS})} = 1 - a_P \qquad (30)$$

Where $a_P = \frac{N_A}{Q_{Diff}}\sqrt{\frac{2\varepsilon}{qN_A}(V_P + V_{bi} - V_{BS})}$ (31)

Using threshold condition (13b)

$$erf\left(\frac{y_{PM}}{2\sqrt{D_1 t_1}}\right) = 1 - \frac{N_A}{Q_{Diff}}\sqrt{\frac{2\varepsilon}{qN_A}(V_{bi} - V_{BS})} \qquad (32)$$

Neglecting the *optical term and bulk term in equation (9), $erf\left(\frac{y_{dg}}{2\sqrt{D_1 t_1}}\right)$ term can be estimated as:

$$erf\left(\frac{y_{dg}}{2\sqrt{D_1 t_1}}\right) = \frac{\varepsilon\sqrt{\pi}}{2qQ_{Diff}}\sqrt{\frac{V_{DS} + \phi_B - V_{GS} - \Delta - V_{op}}{D_1 t_1}} \qquad (33)$$

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REFERENCE

[1] J. J. Gauter, et.al., “optical effects on the static and dynamic characteristics of a GaAs MESFET,” *IEEE Trans. MTT*, vol.MTT-33, pp.819-822.

[2] C. Baak, et.al, “GaAs MESFET: A high speed optical detector,” *Electron Lett.*, vol.13, p.139, 1977.

[3] J. C. Gammel and J. M. Ballantyne, “The OPFET: A new high-speed optical detector,” *in Proc. IEDM*, pp.120-123, 1978.

[4] A. A. de Salles, “Optical control of GaAs MESFET’s,” *IEEE Trans. MTT*, vol. MTT-31, pp.812-820, 1983.

[5] J. M. Osterwaller and B. J. Rickett, “GaAs MESFET demodulates gigabit signal rates from GaAlAs injection laser,” *Proc. IEEE*, vol.67, pp.966-968, 1979.

[6] B. B. Pal, et.al, “Time dependent analysis of an ion implanted GaAs OPFET,” *IEEE Trans. ED*, Vol.42, No.4, pp.491-497, 1994.

[7] J. Graffeuil, P. Rossel and H. Marinot, Electron Lett., vol.15, p.439, 1979.

[8] J. L. Gautier, D. Pasquet and P. Pouvil, “Optical effects on the static and dynamic characteristics of a GaAs MESFET,” *IEEE Trans. MTT*, vol. Mtt-33, pp.819-822, 1985.

[9] H. Mizuno, “Microwave characteristics of an optically-controlled GaAs MESFET,” *IEEE MTT*, vol. MTT-31, pp.596-600, 1983

[10] R. N. Simons and K. B. Bhasin, “Analysis of optically controlled microwave/millimeter-wave device structure,” *IEEE Trans MTT*, vol. MTT-34, pp.1349-1355, 1986.

[11] R. N. Simons, “Microwave performance of an optically controlled AlGaAs high electron mobility transistor and GaAs MESFET,” *IEEE MTT*, vol. MTT-35, pp.1444-1455, 1987.

[12] R. B. Darling and J. P. Uyemura, “optical gain and large-signal characteristics of illuminated GaAs MESFETs,” *IEEE J. Quantum Electron*, vol. QE-23, pp.1160-1171, 1987.

[13] S. Mishra, V. K. Singh and B. B. Pal, “Effect of radiation and surface recombination on the characteristics of an ion implanted GaAs MESFETs,” *IEEE Trans. ED*, vol. 37, pp. 2-10, 1990.

[14] P. Chakrabarti, et.al, “An improved model of an ion implanted GaAs OPFET,” *IEEE Trans. Electron Devices.*, vol. 39, pp.2050-2059, 1992.

[15] Giovanni Breglio, et.al., “Two silicon optical modulators realizable with a fully compatible bipolar process,”

IEEE Journal of selected topics in Quantum Electronics, vol.4, pp. 1003-1010, 1998.

[16] C.L. Schow, et.al., "A 1-Gb/s monolithically integrated silicon NMOS optical receiver," *IEEE Journal of selected topics in Quantum Electronics*, vol.4, pp. 1035-1039, 1998.

[17] Kei Kanemoto, et. al., "Dependence of ion implantation : Induced defects on substrate doping," *J. Appl. Phys.* 89, pp.3156-3161, 2001.

[18] K. L. Narayanan and M. Yamaguchi, "Phosphorous ion implantation in C60 for the photovoltaic applications," *J. Appl. Phys.*, 89, pp.8331-8335, 2001.

[19] G. W. Taylor, H. M. Darley, R. C. Frye and P. K. Chatterjee, "A Device Model for an Ion-Implanted MESFET," *IEEE Transaction Electron Devices* Vol. ED-26, No.3, 1979.

[20] S. M. Sze, "Physics of Semiconductor Devices, 2nd ed. ," *John Wiley & Sons*, New York, 1981.

[21] S. K. Ghandhi, "VLSI fabrication principle of Si and GaAs," *John Wiley & Sons*, New York, 1983.

[22] Hojin Ryu, Jinmo Kang, et.al, "Indium-tin oxide/Si contacts with In- and Sn-diffusion barriers in polycrystalline Si thin-film transistor liquid-crystal displays," *Journal of Electronic Materials*, Vol.32, No.9, p.919, 2003.

[23] P. Chakraborti, S. K. Shrestha, et.al., "Switching characteristics of an optically controlled GaAs-MESFET," *IEEE Trans. Electron Devices*, Vol.42, No.3, pp.365-375, 1994.

[24] B. B. Pal and S. N. Chattopadhyay, "GaAs OPFET characteristics considering the effect of gate depletion with modulation due incident radiation," *IEEE Trans. Electron Devices*, Vol.39, No.5, p.1021-1027, 1992.

[25] S. N. Chattopadhyay and B. B. Pal, "Analytical modeling of an ion implanted silicon MESFET in post-anneal condition," *IEEE Trans. Electron Devices*, Vol.36, No.1, pp.81-87, 1989.

[26] M. S. Shur, "Analytical model of GaAS MESFET," *IEEE Trans. Electron Devices*, vol.25, pp.612-618, 1978.

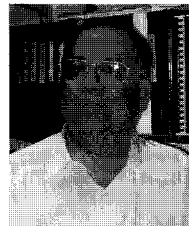
[27] Michael Shur, "GaAs devices and circuits," *Plenum Press*, New York, 1989

[28] T. Takada, K. Yokoyama, et.al., "A MESFET variable capacitance model for GAAs integrated circuit simulation," *IEEE Trans. Microwave Theory Tech.*, Vol.MTT-30, No.5, pp.719-724, 1982.

[29] S. N. Chattopadhyay and B. B. Pal, "The effects of annealing on the switching characteristics of an ion implanted silicon MESFET," *IEEE Trans. Electron Devices*, Vol.36, No.5, pp.920-929, 1988.

[30] M.S. Shur and L. F. Eastman, "Current-voltage characteristics, small-signal parameters, switching times and power–delay products of GaAs MESFETs," *in IEEE MTT-S Int. Microwave Symp. Dig.*, 1978, pp.150-152.

[31] Shiyang Tian, et.al. "A detailed physical model for ion implant induced damage in silicon," *IEEE Trans. Electron Devices*, vol.45, pp.1226-1238, 1998.



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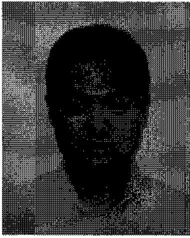

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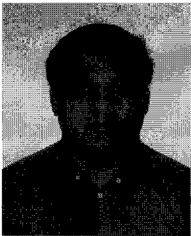

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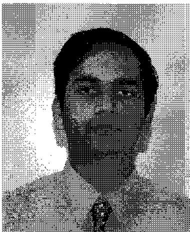

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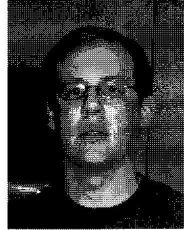

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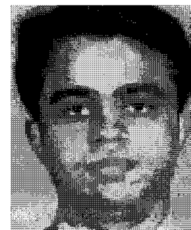

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