Compact Gate Capacitance Model with Polysilicon Depletion Effect for MOS Device

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***Abstract*—The MOS gate capacitance model presented here is determined by directly solving the coupled Poisson equations on the poly and silicon sides, and includes the polysilicon (poly) gate depletion effect. Our compact gate capacitance model exhibits an excellent fit with measured data and parameter values extracted from data are physically acceptable. The data are collected from 0.5, 0.35, 0.25 and 0.18μm CMOS technologies.**

***Index Terms*—Device modeling, gate capacitance, MOSFETs, polysilicon depletion effect.**

I. INTRODUCTION

The assumption in earlier MOS device modeling approaches is to treat the gate as a perfect conductor which would not deplete because the poly is heavily doped compared to the transistor channel. This assumption of a perfect conductor is no longer valid for current deep sub-micron processes. As the oxide thickness gets smaller, the silicon doping in the channel is increased to allow suitable channel control and these circumstances generate higher poly depletion at the gate, [1-4]. The performance degradations of the MOS device, reduced channel charge and gate capacitance result from an increase in channel doping and a decrease in the oxide thickness for a given poly doping [2-7].

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The numerical solutions of (1) indicate that the poly depletion mainly affects the electrostatic potential at the poly/silicon-oxide interface rather than the surface potential at the silicon/silicon-oxide interface. A complete numerical simulation result of (1) is shown in [11]. Our work here focuses on developing a computationally efficient compact physical model for circuit simulation and other applications. The compact model presented here neglects the poly depletion effect on the surface potential at the silicon/ silicon-oxide interface as a first order approximation.

II. MODEL EQUATIONS

Using the gradual channel approximation the coupled one-dimensional Poisson equations for the poly and silicon regions are written as

$$\frac{d^2V}{dX^2} = \frac{q}{\varepsilon_{si}}\begin{cases} n-p-N_d & X \le -T_{ox} \\ n-p+N_a & X \ge 0 \end{cases} \quad (1)$$

where $n = n_i e^{(V-\phi_n)/V_{th}}$ is electron density, $p = n_i e^{-(V-\phi_p)/V_{th}}$ is hole density, n_i intrinsic density, Tox is the silicon-oxide thickness, V(X) is the electrostatic potential; X is the perpendicular distance from the gate to silicon substrate N_d and N_a are the donor and accepter doping densities respectively, q represents electron charge, ε_{si} semiconductor permittivity, ϕ quasi-Fermi potential, $V_{th} = k_b T/q$, k_b Boltzmann constant and T temperature. Both the poly and the silicon doping are considered to be uniform and separated by a thin oxide layer. The assumption here is that the doping density $N_d >> N_a$ in the poly and $N_a >> N_d$ in the silicon.

In this work dimensional voltages and lengths are denoted by capital letters, and lower-case letters denote the same quantities non-dimensionalised. The voltage $V_{th}\ln\lambda$ is used as reference for voltages and potentials, the length value $L_d\sqrt{\ln\lambda/\lambda}$ is used as reference length, where $\lambda = N_a/n_i$ ranges from 10^5 to 10^8, and $L_d = \sqrt{\varepsilon_{si}V_{th}/qn_i}$ is the intrinsic Debye length. The gate oxide capacitance is scaled as $C_{ox} = c_{ox}\varepsilon_{si}/L_d = \varepsilon_{ox}/T_{ox}$. The boundary conditions consist of the continuity of electric potential V and electric displacement, εdV/dX, at the oxide interfaces X=0, -Tox. Moreover the electric displacements at the two interfaces are equal. The electric potential and electric field are also considered to be zero in the bulk. The electrostatic potential V away from the interface at the edge of depleted poly gate is the applied gate voltage (Vgs) minus the flat band voltage (Vfb). The flat band voltage represents the built-in potential or work function differences across the oxide interfaces, [8].

Using the scaling above, equation (1) becomes

$$\frac{d^2v}{dx^2} = \begin{cases} \frac{1}{\beta}e^{(v-v_g^*)\ln\lambda} - \beta e^{-(v+2-v_g^*)\ln\lambda} - 1/\beta & x \le -t_{ox} \\ e^{(v-2)\ln\lambda} - e^{-v\ln\lambda} + 1 & x \ge 0 \end{cases} \tag{2}$$

where $\beta = N_a/N_d$, v_g^* is the gate voltage minus the flat band voltage, and at thermal equilibrium the electron and hole quasi-Fermi potentials are equal. The quasi-Fermi potential is taken to be unity in the silicon substrate and it is $1+v_g^*-v_{bi}$ at the poly gate where $v_{bi} = 2-(\ln(\beta))/\ln\lambda$ is the built-in potential. Integration of (2) and application of the boundary conditions at the bulk and poly gate, give

$$\left.\frac{dv}{dx}\right|_{x=-t_{ox}} = \sqrt{\frac{2}{\beta\ln\lambda}(e^{(v_t-v_g^*)\ln\lambda}-1) + \frac{2\beta}{\ln\lambda}(e^{-(v_t+2-v_g^*)\ln\lambda}-\frac{1}{\lambda^2}) - \frac{2}{\beta}(v_t-v_g^*)} \tag{3a}$$

$$\left.\frac{dv}{dx}\right|_{x=0} = \sqrt{\frac{2}{\ln\lambda}(e^{(v_s-2)\ln\lambda} + e^{-v_s\ln\lambda} - \frac{1}{\lambda^2} - 1) + 2v_s} \tag{3b}$$

Boundary conditions at the oxide interfaces yield

$$\left.\frac{dv}{dx}\right|_{x=-t_{ox}} = \left.\frac{dv}{dx}\right|_{x=0} = c_{ox}\sqrt{\frac{\ln\lambda}{\lambda}}(v_s - v_t) \tag{4}$$

where vs=v(0) and vt=v(-tox)

Equations (3) and (4) give

$$q_g^2 = \frac{2}{\beta\ln\lambda}(e^{(v_t-v_g^*)\ln\lambda}-1) + \frac{2\beta}{\ln\lambda}(e^{-(v_t+2-v_g^*)\ln\lambda}-\frac{1}{\lambda^2}) - \frac{2}{\beta}(v_t-v_g^*) \tag{5}$$

where $q_g^2 = \frac{2}{\ln\lambda}(e^{(v_s-2)\ln\lambda} + e^{-v_s\ln\lambda} - \frac{1}{\lambda^2} - 1) + 2v_s$ is known by neglecting the poly depletion effect on vs as stated in the introduction. There are several methods to solve vs without the poly depletion effect [9, 10]. A solution for vs can be achieved in replacing vt by v_g^* in (4) and solving (3b).

The gate capacitance is defined as

$$C = \frac{dQ_g}{dV_{gs}} \tag{6}$$

where $Q_g = A\cdot(v_s - v_t)V_{th}\ln\lambda\cdot c_{ox}\varepsilon_{si}/L_d$ and A is the capacitance area. Both vs and vt depend on the gate voltage and a closed form of the capacitance can be determined from the derivatives with respect to the gate voltage.

The solution for vt is determined from the transcendental equation (5) using Newton's method, and convergence is achieved with a maximum of two iterations

$$v_t = v_1 - \frac{g(v_1)}{g'(v_1)} \tag{7}$$

Where

$$v_1 = v_0 - \frac{g(v_0)}{g'(v_0)},\quad v_0 = v_g^* - \frac{q_g^2\beta}{2},$$

$$g(v_t) = q_g^2 - \frac{2}{\beta\ln\lambda}(e^{(v_t-v_g^*)\ln\lambda}-1) - \frac{2\beta}{\ln\lambda}(e^{-(v_t+2-v_g^*)\ln\lambda}-\frac{1}{\lambda^2}) + \frac{2}{\beta}(v_t-v_g^*),$$

$$g'(v_t)=\frac{dq_g^{\,2}}{dv_s}\frac{dv_s}{dv_t}-\frac{2}{\beta}e^{(v_t-v_g^*)\ln\lambda}+$$
$$2\beta e^{-(v_t+2-v_g^*)\ln\lambda}+\frac{2}{\beta},$$
$$\frac{dq_g^{\,2}}{dv_s}=2e^{(v_s-v_g^*)\ln\lambda}-2\ln\lambda e^{-v_s\ln\lambda}+2,$$
$$\frac{dv_s}{dv_t}=1+\frac{\frac{\sqrt{\lambda}}{c_{ox}}\left(\frac{1}{\beta}e^{(v_t-v_g^*)\ln\lambda}-\beta e^{-(v_t+2-v_g^*)\ln\lambda}-\frac{1}{\beta}\right)}{\sqrt{\frac{2}{\beta}\left(e^{(v_t-v_g^*)\ln\lambda}-1\right)+2\beta\left(e^{-(v_t+2-v_g^*)\ln\lambda}-\frac{1}{\lambda^2}\right)-\frac{2\ln\lambda}{\beta}(v_t-v_g^*)}}$$

Equation (7) is valid for all device operational regions: accumulation, depletion and inversion. In accumulation, holes are at the device channel surface to provide a net positive charge, at depletion the bulk charge dominates, and electrons provide a net negative charge in the inversion case.

III. RESULTS

The gate capacitance model in (6) gives accurate results for the poly depletion effect (see Table. 1 and comparison with measured data in Figure 1).

Table 1. Model parameters extracted from different technology data.

Tech (μm)	Na (m-3)×10^{23}	Nd (m-3)×10^{26}	Tox (nm)	Vfb (V)
0.18	1.41316	1.40342	3.8870	-0.94
0.25	1.29405	14.0368	5.6094	-0.97
0.35	0.521136	8.4875	7.6198	-0.76
0.5	0.068964	11.2137	14.050	-0.46

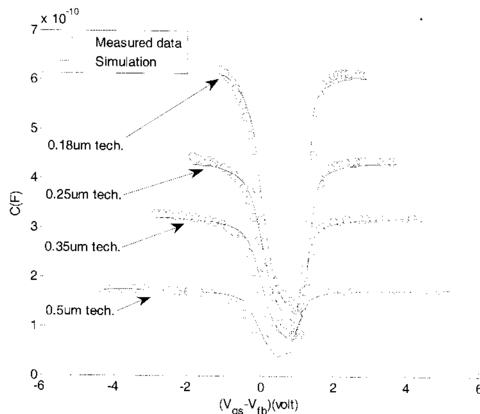

Fig. 1. MOS gate capacitance versus relative gate voltage.

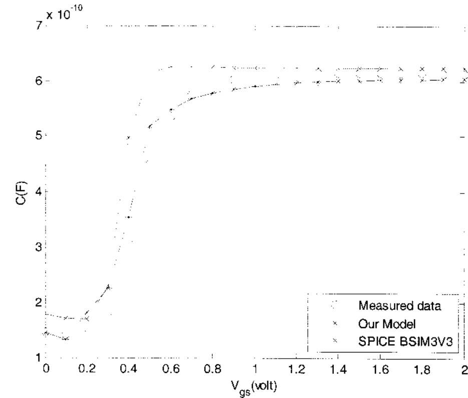

Fig. 2. MOS gate capacitance versus applied gate voltage comparison of the 0.18um tech.

In Figure 2 we compared our model with the industry standard SPICE BSIM3v3 model extracted from the same wafer lot of the 0.18um technology C-V measured data and our model simulation gives improved results. This new information may be used to improve circuit simulations in advanced VLSI since the gate depletion effect is significant in the current MOS devices.

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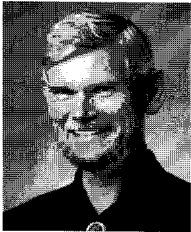

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