

# A Novel Prototype of Duty Cycle Controlled Soft-Switching Half-Bridge DC-DC Converter with Input DC Rail Active Quasi Resonant Snubbers Assisted by High Frequency Planar Transformer

Khairy Fathy\*, Keiki Morimoto\*\*, Ki-Young Suh\*\*\*, Soon-Kurl Kwon<sup>†</sup> and Mutsuo Nakaoka\*\*\*\*

**Abstract** - This paper presents a new circuit topology of active edge resonant snubbers assisted half-bridge soft switching PWM inverter type DC-DC high power converter for DC bus feeding power plants. The proposed DC-DC power converter is composed of a typical voltage source-fed half-bridge high frequency PWM inverter with a high frequency planar transformer link in addition to input DC busline side power semiconductor switching devices for PWM control scheme and parallel capacitive lossless snubbers. The operating principle of the new DC-DC converter treated here is described by using switching mode equivalent circuits, together with its unique features. All the active power switches in the half-bridge arms and input DC buslines can achieve ZCS turn-on and ZVS turn-off commutation transitions. The total turn-off switching losses of the power switches can be significantly reduced. As a result, a high switching frequency IGBTs can be actually selected in the frequency range of 60 kHz under the principle of soft switching. The performance evaluations of the experimental setup are illustrated practically. The effectiveness of this new converter topology is proved for such low voltage and large current DC-DC power supplies as DC bus feeding from a practical point of view.

**Keywords:** Arc welding machine, DC-DC power converter, DC rail active quasi-resonant snubbers, Divided voltage source type, High frequency transformer link, Soft switching PWM

## 1. Introduction

### 1.1 Research Background

Recently, a saturable inductor assisted ZVS-PWM full-bridge high-frequency inverter link DC-DC power converter [1], and lossless capacitors and transformer parasitic inductive components assisted soft switching DC-DC power converter with phase-shifted modulation control scheme in secondary-side of high frequency transformer [2-4] have been developed and evaluated. These power converter circuit topologies are suitable for handling high output power of more than about several kW, especially for high voltage and low current applications as new energy related power supplies. However, secondary magnetic switches or transformer secondary side semiconductor switching devices in these converter circuit topologies may cause large conduction loss when these

power circuit topologies are adopted for low voltage and large current applications such as arc welding power supplies. Therefore, for the low voltage and large current application required for arc welding power supplies, a soft switching DC-DC power converter with active switches in the primary side of the high frequency transformer is considered to be more suitable and acceptable. As a circuit topology to meet this requirement for the arc welder, the authors developed the novel circuit topology of voltage source full-bridge type soft switching PWM inverter in which all the active switches can actively achieve ZCS turn-on and ZVS turn-off commutation operation [6-7].

### 1.2 Research Objectives

This paper presents a novel circuit topology of the voltage source half-bridge type soft switching PWM inverter. Under the newly-proposed high frequency inverter link DC-DC power circuit, all the active switches in the half-bridge arm and dc bus lines can actively achieve ZCS turn-on and ZVS turn-off commutation operation.

The steady state operating principle of the proposed soft switching PWM DC-DC power converter is described with its remarkable features. The experimental operation results of this new type of soft switching PWM DC-DC power converter using IGBT power modules are illustrated including power loss analysis as compared with that of the

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hard switching PWM DC-DC power converter. The practical effectiveness of the proposed high frequency transformer link DC-DC power converter acceptable and suitable for high power applications that is designed for low voltage and large current output is actually proved on the basis of experimental data.

## 2. New Soft Switching DC-DC Converter Topology

Fig. 1 shows the proposed soft switching PWM DC-DC converter circuit using a novel type half-bridge soft switching PWM inverter with high frequency transformer link. The proposed converter is composed of a typical voltage source half-bridge inverter with an active PWM switch  $Q_3(S_3/D_3)$  in the positive dc bus line, an active PWM switch  $Q_4(S_4/D_4)$  in the negative dc bus line, two lossless snubbing capacitors  $C_1, C_2$  and two diodes  $D_5, D_6$ . Two centre points of two capacitors  $C_1, C_2$  and two diodes  $D_5, D_6$  are connected to a mid point of two voltage sources  $E_1, E_2$  and one of the primary winding terminals of the high frequency transformer. The voltage of the two voltage sources  $E_1, E_2$  and capacitance of capacitors  $C_1, C_2$  are designed so as to be equal ( $E_1=E_2=E, C_1=C_2=C$ ). The main active switches  $Q_1(S_1/D_1)$  or  $Q_2(S_2/D_2)$  can be turned on and turned off in accordance with the modified PWM control circuit similar to the conventional half-bridge type hard switching PWM inverter.

Under the proposed soft switching DC-DC converter, the switches in the half-bridge type inverter can perform ZVS turn-off transition due to the presence of the active PWM switches  $Q_3$  or  $Q_4$ , which are turned off and the snubbing capacitors  $C_1$  or  $C_2$ , which are completely discharged before the active switches  $Q_1$  or  $Q_2$ . In the case of half-bridge type inverter, arms are turned off. In addition, the inverter switches can also perform ZCS at a turn-on transition with the aid of inductance  $L_s$ , as a parasitic leakage inductance of the high frequency transformer.

As for the active PWM switches  $Q_3$  or  $Q_4$  in series with the dc bus line side, the PWM controlled switches can achieve ZVS at turn-off mode transition due to the lossless snubbing capacitors  $C_1$  or  $C_2$ . These active PWM switches  $Q_3$  or  $Q_4$  can also achieve ZVS/ZCS at turn-on mode transition due to the lossless snubbing capacitors  $C_1$  or  $C_2$ , which have been charged up to the same voltage as the half voltage  $E_1$  or  $E_2$  of dc power bus line voltage source by the energy storage in the leakage inductance  $L_s$  after the half-bridge type inverter switches are turned off completely.

Although the conduction power loss of the additional switches may increase the total power loss a little, the total turn-off switching loss of the half-bridge type PWM inverter can be significantly decreased with the optimum aid of dc bus line series switches  $Q_3$  or  $Q_4$  and the lossless snubbing

capacitors  $C_1$  or  $C_2$ .

## 3. Principle of Operation

### 3.1 Gate Voltage Pulse Timing Sequences

Fig. 2 shows timing pattern sequences of switching gate driving pulses. The gate voltage pulse signals for the inverter switches  $Q_1$  or  $Q_2$  in voltage source half-bridge inverter arms are the same as PWM signal sequences of the conventional half-bridge inverter. Regarding the turn-on gate voltage pulse signals to the dc bus line side series switches  $Q_3$  or  $Q_4$ , the signals are applied to  $Q_3$  or  $Q_4$  at the same timing as the turn-on signals to  $Q_1$  or  $Q_2$ , respectively. As for the turn-off signals to  $Q_3$  or  $Q_4$ , the signals are delivered to  $Q_3$  or  $Q_4$  before the predetermined length of time  $t_d$  on the basis of the time when the turn-off signals are applied to  $Q_1$  or  $Q_2$ . In other words, the turn-off pulse signals are applied to  $Q_1$  or  $Q_2$  after the turn-off gate signals are supplied to  $Q_3$  or  $Q_4$  by a time  $t_d$ .

### 3.2 Switching operation modes and equivalent circuits

Figure 3 illustrates the relevant operating waveforms during a complete switching period for the pattern of gate drive pulse timing sequences shown in Fig. 2. The switching operation modes of this DC-DC power converter are divided into twelve operation modes from mode 1 to mode 12 in accordance with operating timing sequences, from  $t_1$  to  $t_{12}$ . The operation principle is described in the following paragraph. The equivalent circuits corresponding to respective operation mode are shown in Fig. 4.

- 1) Mode 1 ( $\sim t_1$ ): Before time  $t_0$ , the switches  $Q_1$  and  $Q_3$  are turned on. At this time,  $i_{l1}$  flows through the primary winding of high frequency transformer HF-T.  $i_{s1}$  flows through  $Q_1$  and  $i_{s3}$  flows through  $Q_3$ . In this period, all currents  $i_{l1}$ ,  $i_{s1}$  and  $i_{s3}$  are equal and the voltage  $v_{C1}$  across  $C_1$  is the same as the DC busline voltage  $E_1$ .
- 2) Mode 2 ( $t_1 \sim t_2$ ): At time  $t_0$ , the turn-off pulse signal is applied to  $Q_3$ . At this time, the high side series switch  $Q_3$  in the DC busline can be turned off with ZVS because the current  $i_{s3}$  through  $Q_3$  is immediately cut off due to the lossless snubbing capacitor  $C_1$ . After time  $t_1$ , the voltage  $v_{C1}$  across the capacitor  $C_1$  discharges constantly toward zero voltage from  $E_1=E$ . At this time, the voltage  $v_{C1}$  across the lossless snubber capacitor  $C_1$  is estimated by,

$$v_{C1}(t) = E - (i_{l2}/C)t \quad (1)$$

where,  $i_{l1}$  is a primary current of the high frequency transformer. From Eq. (1), until this voltage  $v_{C1}$  becomes zero, the discharging time  $t_x$  of the capacitor  $C_1$  is given by;

$$t_x = CE / i_{l1} \quad (2)$$

From Eq. (2), the larger the current  $i_{l1}$  though the primary winding of high frequency transformer HF-T, the shorter the discharging time for capacitor  $C_1$ . On the other hand, the smaller the current  $i_{l1}$ , the longer the discharging time  $t_x$ . Under this newly-developed DC-DC power converter circuit (see Fig. 1(a)), the delay time  $t_d$  indicated in Fig. 2 is designed so as to be longer than the time calculated from Eq. (2) under the condition of the maximum  $i_{l1}$  or the maximum output current. In this case, the switches  $Q_1$  or  $Q_2$  can achieve ZVS turn-off transition completely. To enlarge the complete ZVS operation range at the turn-off commutation for the switches  $Q_1$  or  $Q_2$ , the delay time  $t_d$  should be varied according to the value of current  $i_{l1}$ .

- 3) Mode 3( $t_2 \sim t_3$ ): At time  $t_1$ , the voltage  $v_{C1}$  becomes zero. In the interval from  $t_1$  to  $t_2$ , the diodes  $D_5$  is turned on and the current  $i_{l1}$  through high frequency transformer primary winding flows through the circulation loop;  $L_S \rightarrow D_5 \rightarrow S_1 \rightarrow L_S$ .
- 4) Mode 4( $t_3 \sim t_4$ ): At time  $t_2$ , the turn-off gate pulse signal (see Fig. 2) is applied to  $Q_1$ . At this time, the switch  $Q_1$  can be turned off with ZVS because the voltage  $v_{C2}$  across  $C_2$  was already zero during the next half operation cycle and the diodes  $D_2$  of  $Q_2$  are immediately turned on. After that, the capacitor  $C_2$  is charged up to the same voltage as dc busline voltage  $E_2$ .

At this mode, the condition in which the capacitor  $C_2$  is charged up to the same voltage as DC bus line voltage  $E_2$  can be estimated by Eq. (3).

$$(1/2)CE^2 = (1/2)L_S i_{l1}^2 \quad (3)$$

where  $CI=C2=C$

However, as described later in mode 6, circuit parameters should be designed to meet the condition of;

$$(1/2)CE^2 \leq (1/2)L_S i_{l1}^2 \quad (4)$$

in order to achieve ZVS, a turn-on transition of  $Q_4$ .

5) Mode 5( $t_4 \sim t_5$ ): Under a condition of Equation (4), after the voltage  $v_{C2}$  reaches the DC busline voltage  $E_2$ , the voltage  $v_{C2}$  across the snubber capacitor  $C_2$  is clamped to dc bus line voltage  $E_2$  because the diode  $D_4$  of  $Q_4$  is turned on

and the energy stored into the inductor with leakage inductance  $L_S$  is back to DC busline voltage source  $E_2$ .

6) Mode 6( $t_5 \sim t_6$ ): In this mode, all operations are stopped in the primary circuit of the high frequency transformer.

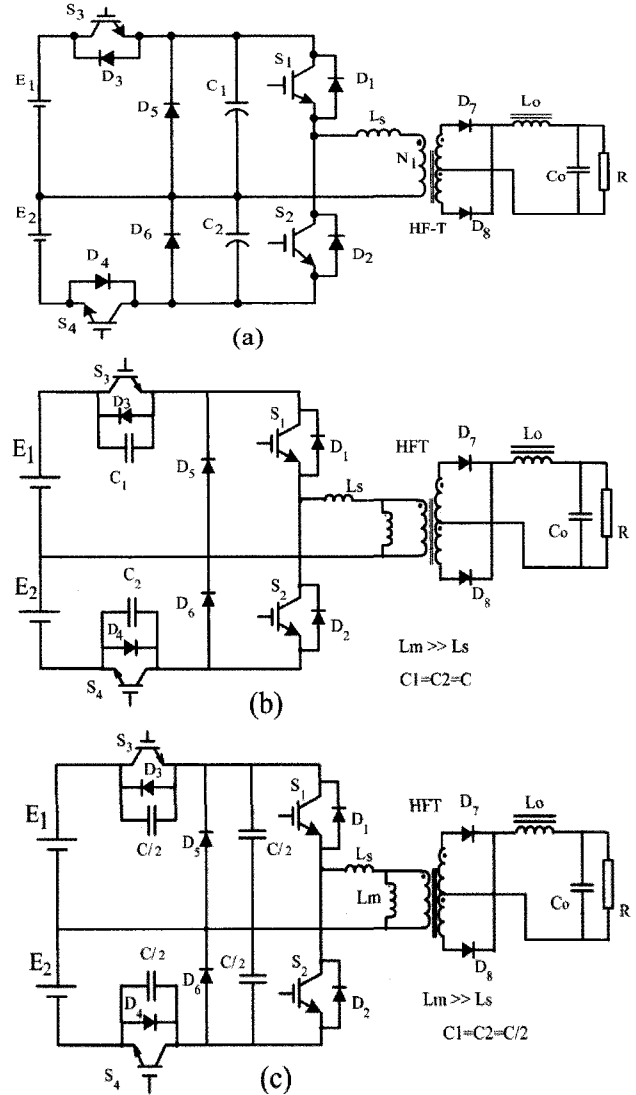


Fig. 1. A novel type half-bridge soft-switching PWM DC-DC power converter.

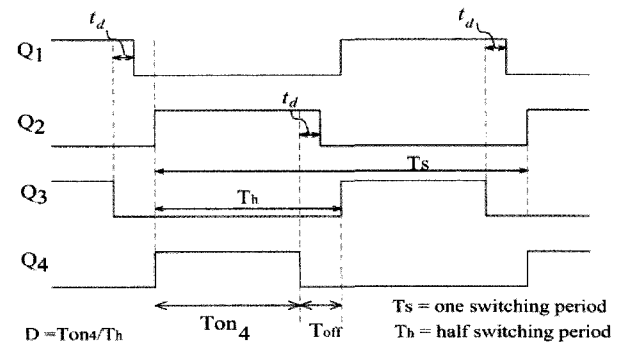


Fig. 2. Timing Pattern sequences of switching gate driving pulses.

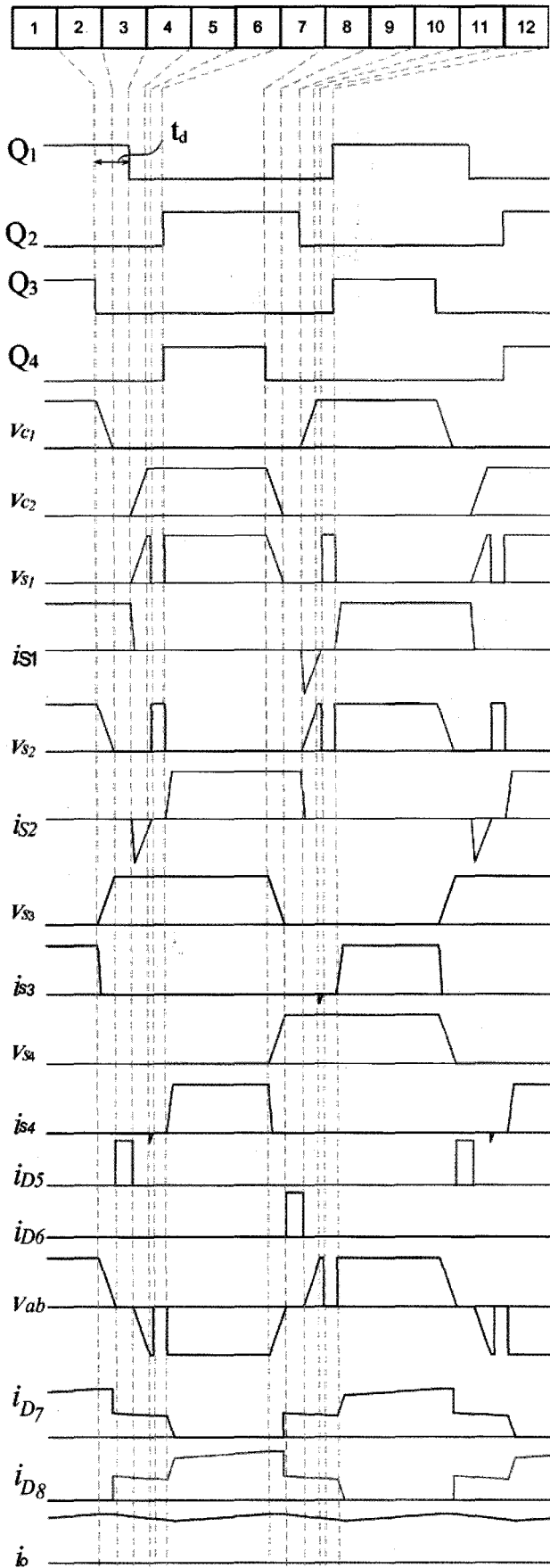
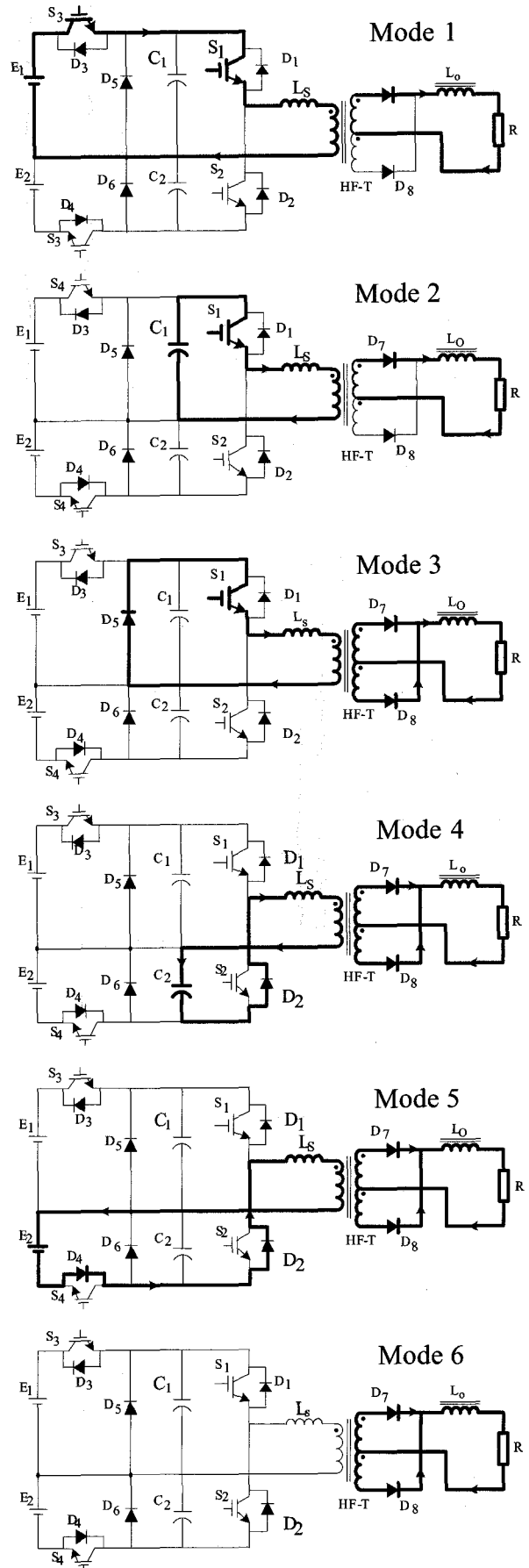


Fig. 3. Operating waveforms during one switching period.



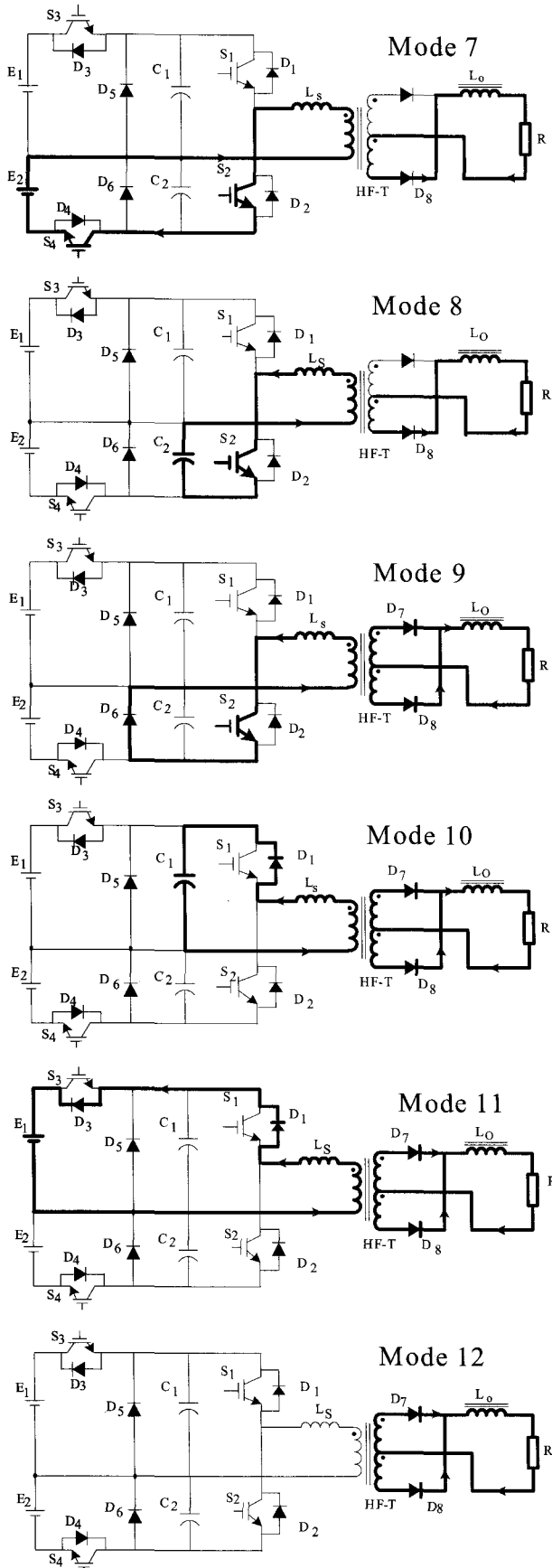


Fig. 4. Equivalent circuits and operational modes for one switching cycle.

- 7) Mode 7( $t_6 \sim t_7$ ): At time  $t_5$ , the turn-on gate pulse signals are applied to the switches  $Q_2$  and  $Q_4$ . At this time, the switch  $Q_2$  can be turned on with ZCS due to the primary-side lumped parasitic inductance  $L_S$  of the high frequency transformer. Furthermore, the series switch  $Q_4$  in the bus line achieves a complete soft-switching ZVS/ZCS at turn-on transition because the voltage  $v_{C2}$  is the same voltage as DC busline voltage  $E_2$ .
- 8) Mode 8( $t_7 \sim t_8$ ): The turn-off signal is applied to  $Q_4$ . At this time, the series switch  $Q_4$  in dc the busline can be turned off with ZVS because the current  $i_{s4}$  through  $Q_4$  is immediately cut off due to the lossless snubbing capacitor  $C_2$ . The voltage  $v_{C2}$  across the capacitor  $C_2$  discharges constantly toward zero.
- 9) Mode 9( $t_8 \sim t_9$ ): The voltage  $v_{C2}$  becomes zero, the diodes  $D_6$  are turned on and the current  $i_{l1}$  through transformer primary winding flows through the loop;  $L_S \rightarrow S_2 \rightarrow D_6 \rightarrow L_S$ .
- 10) Mode 10( $t_9 \sim t_{10}$ ): The turn-off gate pulse signal is applied to  $Q_2$ . At this time, the switch  $Q_2$  can be turned off with ZVS because the voltage  $v_{C2}$  was already zero during the last half operation cycle and the diodes  $D_1$  of  $Q_1$  are immediately turned on. After that, the capacitor  $C_1$  is charged up to the same voltage as dc busline voltage  $E_1$ .
- 11) Mode 11( $t_{10} \sim t_{11}$ ): After the voltage  $v_{C1}$  across the snubber capacitor  $C_1$  reaches the dc busline voltage  $E_1$ , it is clamped to dc busline voltage  $E_1$  because the diode  $D_3$  of  $Q_3$  is turned on and the energy stored into leakage inductance  $L_S$  is back to dc busline voltage source  $E_1$ .
- 12) Mode 12( $t_{11} \sim t_{12}$ ): At this mode, all operations are stopped in the primary circuit.

Thereafter, the operation processes for  $Q_1$ ,  $Q_3$  and  $Q_2$ ,  $Q_4$  will be repeated in sequence continuously from mode 1 to mode 12 as in Fig. 4.

## 4. Experimental Results and Discussions

### 4.1. Total System Implementations

The experimental DC-DC converter circuit setup treated here is shown in Figure 5. In the DC-DC converter setup implementation, the maximum output voltage and current are designed for 36V, 400A, respectively. The design specifications and circuit parameters are described in Table 1.

The complete appearance of experimental setup using low voltage large current arc welding power supply is presented in Figure 6. The maximum DC output power of this experimental power supply setup is designed for 14.4

kW. Figure 7 represents the assembled component appearance on the printed circuit board (PCB) in the primary main circuit. Figure 8 shows the exterior appearance of the high frequency transformer in the proposed soft switching PWM DC-DC converter. The IGBT power modules are mounted on the heat sink and connected by the printed circuit board in which the capacitors  $C_1$  and  $C_2$  are mounted on the PCB and the capacitors  $C_3$  and  $C_4$  are directly connected to the output of the three phase rectifier. Connecting IGBTs and capacitor  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$  by the printed circuit board enables minimization of the stray line inductance with optimum connections among IGBTs,  $C_1$ ,  $C_2$ ,  $C_3$  and  $C_4$ . Actually, the minimum leakage inductance of the high frequency transformer is particularly important on this new soft-switching PWM DC-DC converter, because spike voltage across collector and emitter of IGBTs easily appears at a turn off transition if there is wiring stray inductance between snubbing capacitors and the IGBT switches.

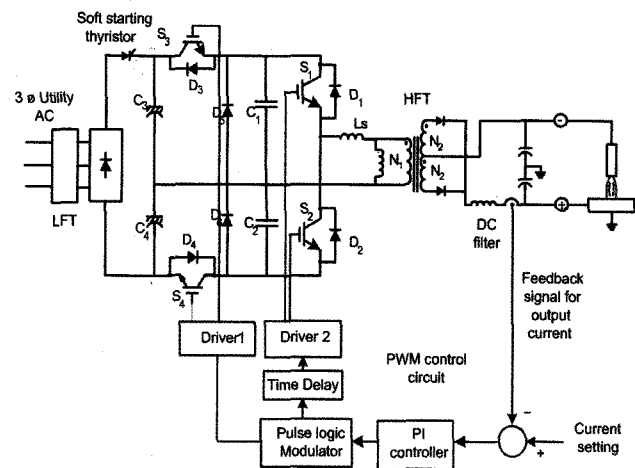


Fig. 5. Experimental setup circuit implementation.

Table 1. Design specifications and circuit parameters.

Item	Symbol	Value
Utility AC Input Voltage		AC400[V]
Inverter Switching Frequency	$f_s$	40 [kHz]
Switching Period	$T_s$	25 [ $\mu$ s]
Primary Side Lumped Leakage Inductance of High Frequency Transformer	$L_s$	2 [ $\mu$ H]
Capacitance of Quasi Resonant Capacitors	$C_1, C_2$	0.235[ $\mu$ F]
Capacitance of DC Smoothing Filter Capacitor	$C_3, C_4$	2200[ $\mu$ F]
Inductance of DC Reactor in Load Side	$L_o$	60[ $\mu$ H]
Equivalent Load Resistance (Stable Arc Welding Load)	$R$	0.09 [ $\Omega$ ]
Maximum Load Current	$I_o$	400 [A]
Turns Ratio of HFT	$N_1:N_2:N_3$	4:1:1
Remarks; $L_m \gg L_s$		

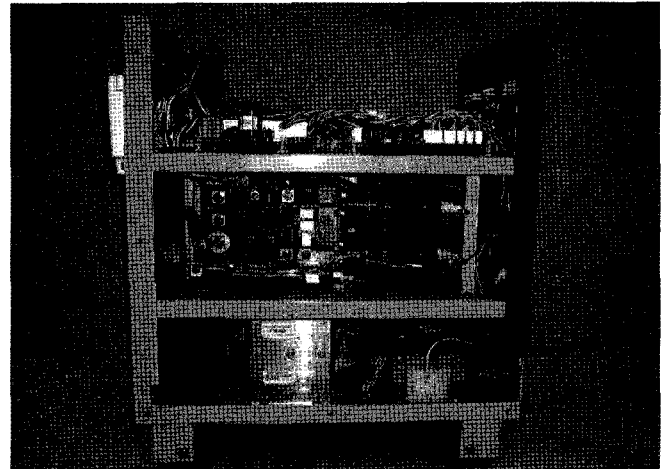


Fig. 6. Complete appearance of stick arc welding power supply using newly-developed soft switching DC-DC converter.

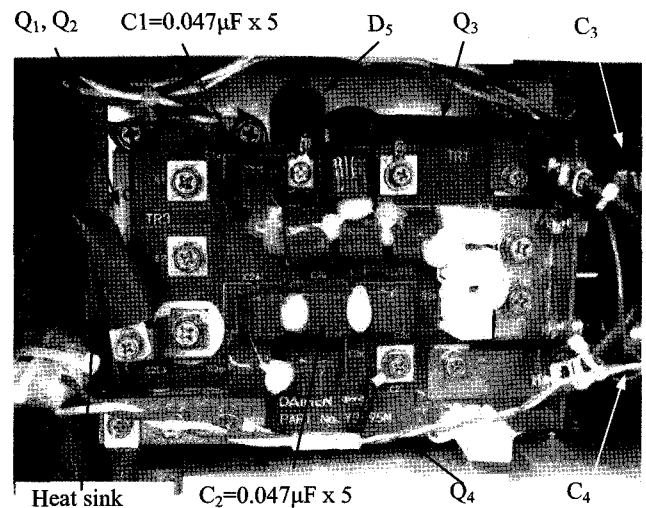


Fig. 7. Assembled component appearance in high frequency transformer primary side circuit.

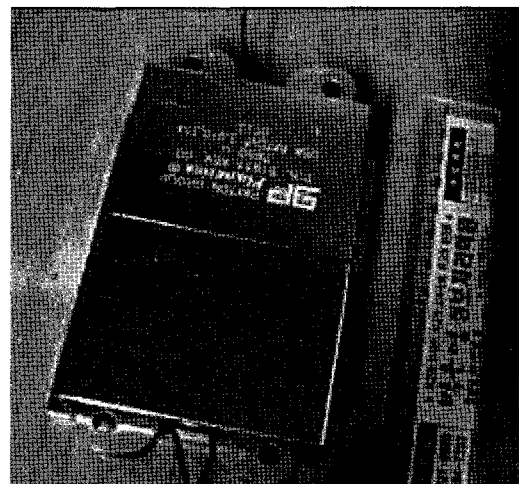
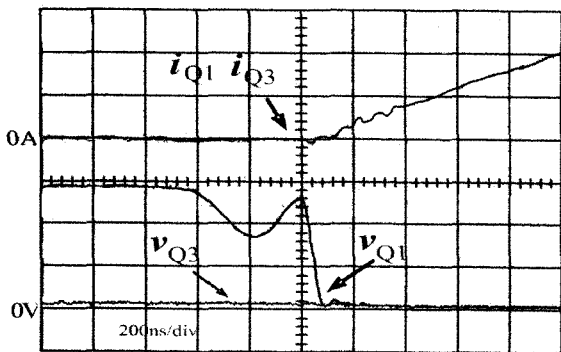


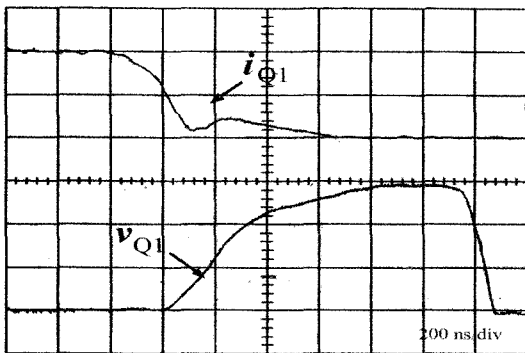
Fig. 8. Exterior appearance of high frequency transformer in the proposed soft switching PWM DC-DC converter.

### 4.2. Measured Voltage and Current Switching Waveforms

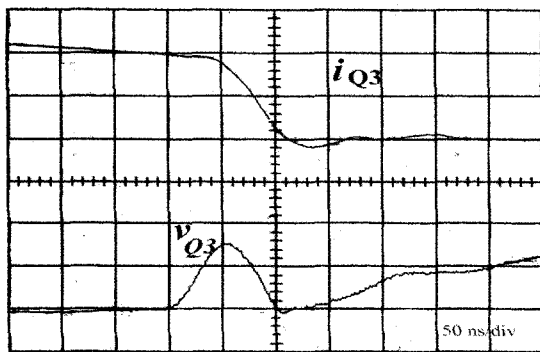
The switching operating waveforms for voltage and current when the switch  $Q_1$  is turned on and turned off are shown in Fig. 9 (a) and (b). Observing these operating waveforms, the switch  $Q_1$  is turned on with ZCS and also turned off with ZVS. The switching waveforms for voltage and current when the switch  $Q_3$  is turned on and turned off are shown respectively in Fig 9 (a) and (c). Observing the operating waveforms, the switch  $Q_3$  is turned on with ZVS/ZCS and is turned off with ZVS. However, at the turn-off transition for  $Q_1$  and  $Q_3$ , only a few switching power losses still exist due to the inherent tail current characteristic of IGBTs.



(a) Turn on switching waveforms for  $Q_1, Q_3$



(b) Turn off switching waveforms for the switch  $Q_1$



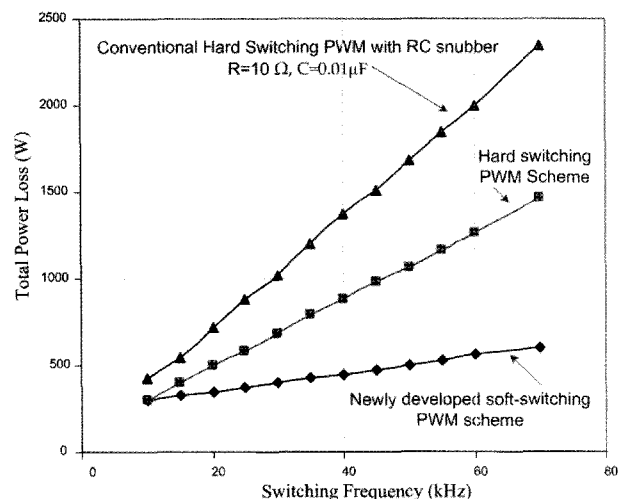
(c) Turn off switching waveforms for the switch  $Q_3$

**Fig. 9.** Measured switching waveforms for active power switches  $Q_1$  and  $Q_3$

### 4.3. Comparative Results of Power Loss Analysis

In the power loss analysis and evaluations presented in Fig. 9, the total power loss of all the switches including  $Q_3$  and  $Q_4$  in the newly-developed DC-DC power converter circuit is compared with that of all the switches in the conventional hard switching PWM inverter type. When the switching frequency is 10 kHz, the total power losses for both inverter type DC-DC power converter circuits are almost equal to each other. Furthermore, the switching frequency of the high frequency inverter power stage using IGBTs is designed for more than about 10 kHz. The more the switching frequency of the inverter increases, the more this newly-developed DC-DC power converter circuit has remarkable advantages relating to the power conversion efficiency and power density as compared with the conventional hard switching inverter type DC-DC power converter.

In case the switching frequency is designed for 40 kHz, the total power loss for the switches in newly-developed DC-DC power converter circuits is 445W and that of the conventional hard-switching PWM inverter is 865W. Furthermore, the snubber circuit is necessary for the conventional hard switching PWM DC-DC power converter circuit. Therefore, the total power loss for the conventional hard switching converter circuit including the power loss of the snubber circuit is estimated to be about 1370W. This loss is three times more than the total power loss of the newly-developed converter circuit.



**Fig. 10.** Comparative power loss analysis between newly developed and conventional hard switching converters.

### 5. Conclusions

In this paper, the novel circuit topology of the voltage

source modified half-bridge soft switching PWM DC-DC power converter with a high frequency planar transformer link was presented. The operating principle, switching pattern and control strategy of the half-bridge soft switching PWM DC-DC power converter designed for inverter switching frequency 40 kHz, 36V and 400A output specifications were illustrated and discussed for low voltage and large current output applications such as telecommunication and automotive applications as well as arc welding power supply applications. The power loss analysis of the proposed soft switching DC-DC power converter was discussed and evaluated as compared with the hard switching PWM DC-DC power converter with a high frequency transformer link. The practical effectiveness of the proposed DC-DC power converter operation under a soft switching PWM scheme was actually proved from a practical point of view and the high efficiency and power density of this converter could be achieved on the basis of experimental results for low voltage and large current power supplies.

Under the simple circuit, which has two additional power semiconductor switching devices and two passive circuit components compared to the typical half-bridge inverter circuit, all the active switching devices incorporated into half bridge inverter arms and DC busline input achieve ZVS turn-off and ZCS turn-on commutation. When the switching frequency of the high frequency inverter using IGBTs is selected more than about 10 kHz, the more the switching frequency of inverter increases, the more this proposed PWM DC-DC power converter has remarkable advantage in relation to the power conversion efficiency and power density as compared with the conventional hard switching inverter type DC-DC power converter.

The downsizing and light-weighted power supply using this newly-developed soft switching DC-DC power converter circuit was developed and put into the practical market in industry.

In the future, in order to improve the power conversion efficiency and reduce the electromagnetic noise, SiC-SBD or GaN-SBD as the passive power switches and SiC-JFET/SIT as the active power switches should be introduced and evaluated for the proposed soft switching DC-DC converter with high frequency transformer link.

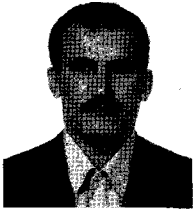
### Acknowledgment

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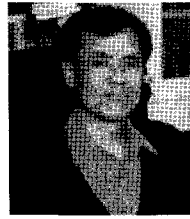
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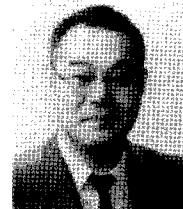
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