A Study on Improvement of a-Si:H TFT Operating Speed

Chang Wu Hur, *Member, KIMICS*

Abstract—The a-Si:H TFTs decreasing parasitic capacitance of source-drain is fabricated on glass. The structure of a-Si:H TFTs is inverted staggered. The gate electrode is formed by patterning with length of 8 μm~16 μm and width of 80~200 μm after depositing with gate electrode (Cr) 1500 Å under corning 7059 glass substrate. We have fabricated a-SiN:H, conductor, etch-stopper and photoresistor on gate electrode in sequence, respectively. The thickness of these thin films is formed with a-SiN:H (2000 μm), a-Si:H(2000 μm) and n^+a-Si:H (500 μm). We have deposited n^+a-Si:H , NPR(Negative Photo Resister) layer after forming pattern of Cr gate electrode by etch-stopper pattern. The NPR layer by inverting pattern of upper gate electrode is patterned and the n^+a-Si:H layer is etched by the NPR pattern. The NPR layer is removed. After Cr layer is deposited and patterned, the source-drain electrode is formed. The a-Si:H TFTs decreasing parasitic capacitance of source-drain show drain current of 8 μA at 20 gate voltages, I_{on}/I_{off} ratio of ~10^8 and V_{th} of 4 volts .

Index Terms—parasitic capacitance of source-drain, inverting pattern of upper gate electrode, etch-stopper.

I. INTRODUCTION

Today, amorphous silicon is widely used in optical to electrical conversion device and wide area film device. Especially, a-Si:H is used such as a switching device for active matrix LCD, contact image sensor for a-Si:H TFT and Fax, and a-Si:H solar cell. In all these applications the transistor acts as a switch.

Hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) can be important circuit elements in large-area imaging sensors because of their advantageous material and optical properties.

If TFT-LCD becomes large size and high definition, the RC time constant of TFT gate line is increased and the degradation of image quality occurs. So, the resistance of gate line and the electrical capacitance has to be decreased.

To improve TFT operating speed, there is a method decreasing parasitic capacitance of gate to source-drain. Many companies of advanced countries is studying a method decreasing parasitic capacitance of gate to source-drain by self-align method at present. In this paper, a method different from the conventional method is used. This method simplifies fabrication process and makes to decrease parasitic capacitance of gate to source-drain.

II. FABRICATION AND CHARACERISTIC OF ETCH-STOPPER A-SI:H TFT

Amorphous silicon is deposited using plasma enhanced chemical vapor deposition (PECVD). At this time, electrical and optical characteristics of amorphous silicon such as conductivity, optical band gap and deposition rate are changed under deposition condition such as SiH_4, flux, chamber pressure, RF power and substrate temperature. The optical band gap of a-Si:H thin film shows 1.7 ~ 1.8eV, as a flux of SiH_4 is increased, it is deposited from 1.0 to 6.9 (Å/sec).

Generally, we can estimate the trade-off relation between conductivity and optical band gap according to a flux of SiH_4 and control the optical band gap by adjusting a flux of SiH_4. But, the change of conductivity and optical band gap is little according to chamber pressure condition. The deposition rate is ranged from 1.0 to 3.0 (Å/sec). Also, the change of electrical and optical characteristics is a little according to RF power. Figure 1 shows the IR spectrum result. It represents a relation between Si of a hydrogenated amorphous silicon film and bonding of H. Frequency of fundamental infrared absorption modes depends on a mass of oscillation dipole and amount of bond between elements including dipole. The a-Si:H film shows a type of vibration mode, it shows SiH_4 stretching mode at wave number 2000 cm^{-1}. Also, it represents a rocking mode at wave number 635 cm^{-1}. The bond represented at weaker bond range 800 ~ 900 cm^{-1} depends on the vibrational mode of SiH_2. Therefore, the fabricated a-SiH film in this experimental setup shows that Si-H bonding of stretching/rocking mode exists. The gate insulator layer and a-SiN:H film of passivation film are fabricated using PECVD by mixing SiH_4 gas and NH_3gas. Figure 3 shows optical bandgap of a-SiN:H. Etching rate of a-SiN:H increases and refraction diminishes as NH_3/SiH_4 increases. Also, their characteristics are not related with RF power. The E_{opt} value is around 2.4 eV.

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Chang Wu Hur is with the Mokwon University, Department of Information Electronics & Imaging Engineering (phone: 82-42-829-7655).

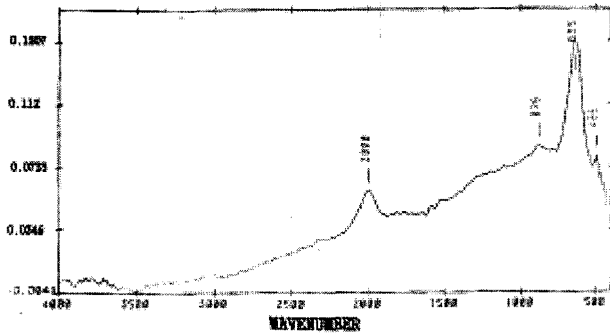

Fig. 1 FTIR characteristics of a-Si:H

Figure 2 shows a cross-section of thin film transistor fabricated in this experimental setup. The gate electrode is formed by patterning with length of 8 μm~16 μm and width of 80~200 μm after depositing with gate electrode (Cr) 1500 Å under corning 7059 glass substrate. We have fabricated a-SiN:H, a-Si:H and a-SiN:H on gate electrode in sequence. The thickness of these thin films is formed with a-SiN:H (2000 Å), a-Si:H(2000 Å) and a-SiN:H (2000 Å). After upper layer a-SiN:H of etch-stopper pattern is patterned by pattern of Cr gate electrode, we have deposited n^+a-Si:H(500Å) thin film and the NPR(Negative Photo Resister) layer. The NPR layer by inverting pattern of gate electrode is patterned and the n^+a-Si:H layer is etched by the NPR pattern. The NPR layer is removed. We have used a RIE (Reactive Ion Etching) method using CF + O_2 gas to etch n^+a-Si:H layer. RIE equipment is used RI mode of PECVD. a-Si:N:H is patterned by RIE and the used gas is used by mixing CHF_3 and O_3. To compensate damage by RIE process, the sample is annealed at temperature 200 °C in vacuum state. To form a source drain electrode, the film is patterned after deposit 4000 Å of Al by E-beam evaporator.

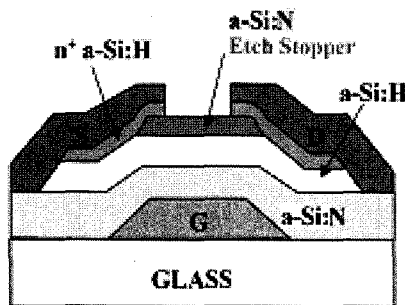

Fig. 2 Structure of a-Si:H TFT

To measure the electrical characteristics of the fabricated samples, we obtained characteristics of I-V, V_{th} and I_{on}/I_{off} by using probe station and 4145A parameter measurement equipment. As shown in figure 3, 4, 5, The saturation current at gate voltage 20 Volts is 8 μA, I_{on}/I_{off} is ~10^8 and V_{th} is 4 volts. We have estimated that the leakage current of the TFT is very small. That is to say, the V_{th} of the TFT using etch-stopper compared with conventional TFT shows a small value and has 4 volts. I_{on}/I_{off} has ~ 10^8 order value. From the results, we can estimate that this method simplifies fabrication process and makes to decrease parasitic capacitance of gate to source-drain. It enhanced a good electrical characteristic. Also, the leakage current can be diminished.

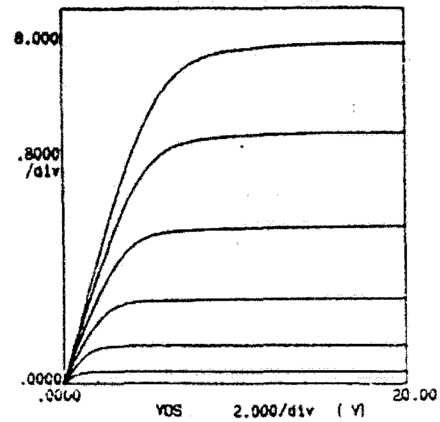

Fig. 3 I-V Characteristics of a-Si:H TFT

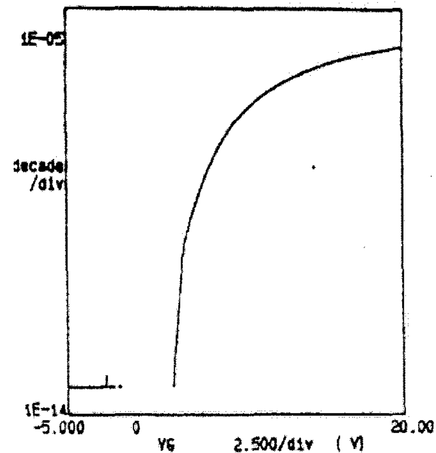

Fig. 4 I_{on}/I_{off} Characteristics of a-Si:H TFT

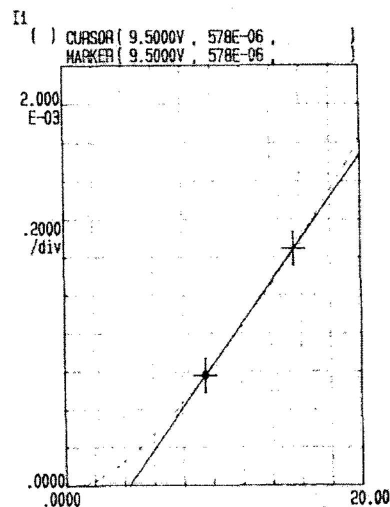

Fig. 5 V_{th} Characteristics of a-Si:H TFT

III. CONCLUSION

Hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) can be important circuit elements in large-area imaging sensors because of their advantageous material and optical properties. To improve TFT operating speed, there is a method decreasing parasitic capacitance of gate to source-drain. In this paper, a method different from the conventional method is used. This method simplifies fabrication process and makes to decrease parasitic capacitance of gate to source-drain. From the experimental results, the TFT of this paper has a higher value of I_{on}/I_{off} compared with conventional TFT. In the case of I_{off} current, leakage current between source and gate reduces. Also, this effect gives the increase of I_{on}/I_{off}. From the I-V curve, we can estimate that drain current of TFT at same gate voltage increases over 8μA. And, leakage current between gate and source is much smaller. From the results, we can estimate that this method simplifies fabrication process and makes to decrease parasitic capacitance of gate to source-drain. It enhanced a good electrical characteristic. Also, the leakage current can be diminished. These phenomena give a good result. This method can be applicable to device such as HDTV display.

IV. CONCLUSIONS

Hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) can be important circuit elements in large-area imaging sensors because of their advantageous material and optical properties. To improve TFT operating speed, there is a method decreasing parasitic capacitance of gate to source-drain. In this paper, a method different from the conventional method is used. this method simplifies fabrication process and makes to decrease parasitic capacitance of gate to source-drain. From the experimental results, the TFT of this paper has a higher value of I_{on}/I_{off} compared with conventional TFT. In the case of I_{off} current, leakage current between source and gate reduces. Also, this effect gives the increase of I_{on}/I_{off}. From the I-V curve, we can estimate that drain current of TFT at same gate voltage increases over 8μA. And, leakage current between gate and source is much smaller. From the results, we can estimate that this method simplifies fabrication process and makes to decrease parasitic capacitance of gate to source-drain. It enhanced a good electrical characteristic. Also, the leakage current can be diminished. These phenomena give good results. This method can be applicable to device such as HDTV display.

REFERENCES

[1] Michael Hack, "Physical models for amorphous-silicon TFT and their implementation in a circuit simulation program", IEEE ED., pp.2764-2769, Dec, 1989.

[2] K. Aflatooni, a-Si:H Schottky diode direct detection pixel for large area x-ray imaging, IEEE IEDM, December 7-10, Washington, D.C., 1997.

[3] Chang W. Hur, " Method of Making Thin Film Transistors", United States Patent, Patent No.5,306,653, Apr. 1994.

[4] R.V.R. Murthy, Mechanisms underlying leakage current in inverted staggered a-Si:H thin film transistors, Fourth Symp. on Thin Film Transistor Technologies, Boston, Nov. 1-6, 1998.

[5] A. Nathan, Correlation between leakage current and overlap capacitance in a-Si:H TFTs, IEEE Workshop on Charge-Coupled Devices and Advanced Image Sensor, Karuizawa, Japan, June 10-12, 1999.

Change-Wu Hur
received his B.S.degree in Electronic Engineering from Kwangwoon University in 1982 and M.S. and Ph.D. degrees in Electrical and Electronic Engineering from the Yonsei University in 1984 and 1991, respectively. From 1986 to 1994, he joined at LG Research Center, where he worked as Senior Member of Technical Staff. In 1994, he joined the department of Electronic and Information security Engineering, Mokwon University, Korea, where he is presently a professor. His research interest is in the area of VLSI and Display that includes ASIC design, Display technology and Wireless Communication design.