Analysis of Short Channel Effects Using Analytical Transport Model For Double Gate MOSFET

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Abstract — The analytical transport model in subthreshold regime for double gate MOSFET has been presented to analyze the short channel effects such as subthreshold swing, threshold voltage roll-off and drain induced barrier lowering. The present approach includes the quantum tunneling of carriers through the source-drain barrier. Poisson equation is used for modeling thermionic emission current, and Wentzel-Kramers-Brillouin approximations are applied for modeling quantum tunneling current. This model has been used to investigate the subthreshold operations of double gate MOSFET having the gate length of the nanometer range with ultra thin gate oxide and channel thickness under sub-20nm. Compared with results of two dimensional numerical simulations, the results in this study show good agreements with those for subthreshold swing and threshold voltage roll-off. Note the short channel effects degrade due to quantum tunneling, especially in the gate length of below 10nm, and DGMOSFETs have to be very strictly designed in the regime of below 10nm gate length since quantum tunneling becomes the main transport mechanism in the subthreshold region.

Index Terms—Double gate MOSFET, Short Channel Effects, Subthreshold Swing, Threshold roll-off, Drain Induced Barrier Lowering.

I. INTRODUCTION

THE double-gate MOSFET (DGMOSFET) is a particularly promising candidate for ultimate CMOS scaling due to its better control of short channel effects(SCEs) such as near-ideal subthreshold slope and mobility enhancement.[1][2] The DGMOSFET is also very promising for achieving ballistic transport due to its low doped channel and double gate feature, in addition to the superior control of short channel effects. The two gates control roughly twice as much current as a single gate, resulting in stronger switching signals. The double gate design provides inherent electrostatic and hot-carrier coupling in the channel. This intimate coupling between the gates and channel makes DGMOSFET technology the most scalable of all FET designs. The DGMOSFET is electrostatically stronger than a single-gate MOSFET because two gates are used to control the channel from both sides, thus allowing for additional gate length scaling by at least a factor of two. The addition of a second gate electrode not only halves the effective channel thickness of the device, but also eliminates penetration of the drain electric field through the buried oxide, which improves gate control of the channel. The challenge lies in obtaining suitable threshold voltages for high-speed logic devices, while controlling extrinsic resistance. However, for sub-20nm DGMOSFET, the SCEs such as threshold roll-off and drain induced barrier lowering(DIBL) and degradation of subthreshold swing become very important features that cannot be neglected. Thus we need the simple and analytical models with physical meaning to apply eventually to circuit simulation and IC design. Consequently, the aim of this work is to model subthreshold operations for DGMOSFET into the simple and analytical equations. In this work, we propose a analytical model of subthreshold current transport including both thermionic emission and quantum tunneling of carriers for analyzing the subthreshold operations of DGMOSFET structure with ultra thin and short channel. We present new analytical model for potential in channel not to use approximation of $\exp(-L_g / \lambda_j)$ since this term is not negligible in the case of devices with gate length of below 20nm. The quantum tunneling rate has been derived from the reasonable Wentzel-Kramers-Brillouin(WKB) approximations, and the gate length- and voltage-dependent quantum tunneling current are obtained to analyze SCEs such as SS , ΔV_{th} and $DIBL$ for sub-20nm DGMOSFET.

This analytical model with quantum tunneling and the simulated devices is described in section II. In section III some key simulation results have been presented in the case of SCEs for DGMOSFET operations, focusing on the influence of tunneling in the subthreshold regime and the limitation of scaling in DGMOSFET. Section IV summarizes the results and emphasizes the main conclusions of this work.

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II. DEVICE STRUCTURE AND MODEL

This symmetric structure is characterized by two

identical polysilicon gates with no overlap with the source/drain extensions, as shown in Fig. 1. A very thin lightly p-type doped silicon channel with thickness t_{Si}, thin gate oxide of thickness t_{ox}, and channel length L_g are the geometric parameters. The doping level of the p-type silicon channel is $N_A = 10^{16} cm^{-3}$. The n-type source and drain regions are uniformly doped at the level of $10^{20} cm^{-3}$. The poly-gate is uniformly doped p-type with doping concentration of $10^{20} cm^{-3}$.

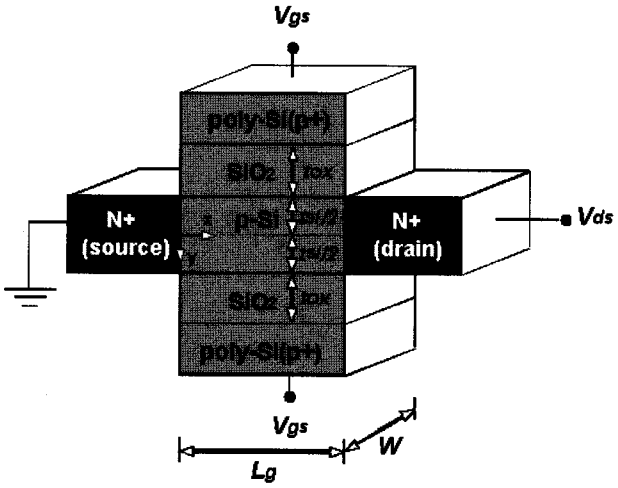

Fig. 1 Schematic structure of the symmetrical double gate MOSFET

For DGMOSFETs with channel lengths in the 10nm region, it can be assumed that the thermionic emission and tunneling currents dominate. Since the two current mechanisms are independent, the two current models are developed separately. For either current, an equation for the channel potential in the channel is necessary. The channel potential in the subthreshold region can be obtained from the 2D Poisson equation under the condition of full depletion and the potential can be expressed as[3]

$$\Psi(x,y) = V_{gs} - \phi_{MS} + U_{1D}(y) + \phi_{2D}(x,y) \qquad (1)$$

where V_{gs} is the gate voltage, ϕ_{MS} is the gate-to-channel work function difference, and $U_{1D}(y)$ is the 1D potential in the direction of thickness.

The term $\phi_{2D}(x,y)$ is the solution of the 2D Laplace equation, describing the influence of the source/drain.

The thermionic current is determined by the number of electrons that overcome the barrier height between the source and drain per unit time. Based on the Maxwell-Boltzmann statistics, the concentration of electrons in the source at energy levels higher than the barrier peak is $n_m = (n_i^2 / N_A) e^{q\phi_{\min}/kT}$, where n_i is the intrinsic carrier concentration. The minimum channel potential $\phi_{\min}$, corresponding to the current path, can be found from the condition $\partial\Psi(x,y)/\partial x = 0$. Given that these electrons move randomly with the average thermal velocity v_{th}, about 1/6 of these electrons move toward the drain and the number of electrons that hit the cross-sectional area $t_{Si}W$ per unit time is $n_m v_{th} t_{Si} W/6$. Therefore, the thermionic current is

$$\begin{aligned} I_{ther} &= q n_m(y) v_{th} t_{Si} W/6 \\ &\approx q n_m(d_{eff}) v_{th} t_{Si} W/6 \end{aligned} \qquad (2)$$

The parameter, d_{eff}, represents the effective current path[3].

Quantum-mechanical tunneling was not included in the analysis published by Qiang et al.[3], which focused on modeling SCE effects due to thermionic emission (but not including an equation for the thermionic current itself). However, the tunneling current is no longer negligible when channel lengths decrease to the 10-nm range. In this paper, the WKB approximation is used to determine the tunneling probability. The WKB approximation is relatively simple and reasonably accurate for channel lengths down to a few nanometers. The differences between the results derived from the WKB approximation and full quantum treatment are insignificant, according to recent report by Stadele[4].

Assuming that the concentration of electrons in the source is equal to the doping level N_D and that 1/6 of these electrons move toward the drain with the average thermal velocity v_{th}, the number of electrons that hit the barrier per unit time is $N_D v_{th} t_{Si} W/6$. This number has to be multiplied by the tunneling probability to obtain the tunneling current. Given that 2/3 of the electrons appear with the transversal and 1/3 with the longitudinal effective mass, the following equation for the tunneling current is obtained:

$$I_{tunn} = (qN_D t_{Si} W/6)(2T_t v_{th_t}/3 + T_l v_{th}/3) \qquad (3)$$

where T_t and v_{th_t} are the tunneling probability and the thermal velocity for electrons with the transversal effective mass, T_l and v_{th_l} are the tunneling probability and the thermal velocity for the electrons with the longitudinal effective mass. Analogously to the discussion related to the net thermionic current, the tunneling from the drain toward the source can be neglected at sufficiently high V_{ds} voltages. Adding the thermionic and the tunneling currents, the total subthreshold current

I_{tot} is obtained.

The general subthreshold-swing model for subthreshold current consisting of two components (thermionic and tunneling) can be expressed as

$$SS = \left[\frac{\partial I_{ther} / \partial V_{gs} + \partial I_{tunn} / \partial V_{gs}}{\ln 10 \bullet I_{tot}} \right] \quad (4)$$

III. VERIFICATION OF THE MODEL

3.1 Subthreshold Swing

To verify this new model for DGMOSFET in the subthreshold region, the subthreshold swings obtained by this model are compared to 2D simulation results.[5]

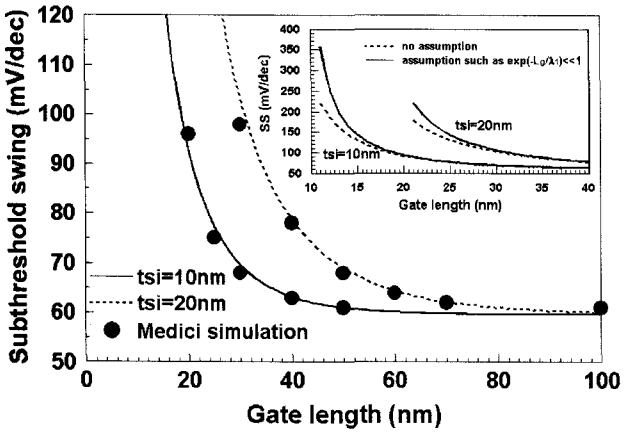

Fig. 2 Comparison of subthreshold swings for Medici simulation[5] and this model

Figure 2 shows the variation of subthreshold swing as a function of gate length. It can be seen that the results from the proposed model in this paper agree well with Medici numerical simulation including drift-diffusion current. Note that drift-diffusion current is negligible in subthreshold regime as shown in analysis published by Qiang et al. For shorter channels, the subthreshold-swing degradation is larger because the quantum tunneling is more pronounced.

3.2 Subthreshold current

The thermionic current dominates for channel lengths above 10nm, whereas the tunneling current dominates for channel length below 10nm[6]. Given that the dependence of tunneling current on gate voltage is weak, the subthreshold swing increases significantly in the sub-10nm region, degrading the performance gains achieved by the thin body and the double gate. Reasonable values of subthreshold swing (60-80mV/decade) can only be obtained with above 20-nm gate lengths when the current is mostly due to thermionic emission. The relative contribution of the tunneling current can be reduced by an increase in channel thickness, but this method is not good since the subthreshold swing is then incresaed by the thermionic current.

Figure 3 shows the subthreshold transfer characteristics I_{ds} versus V_{gs} at $V_{ds} = 0.1V$ for channel lengths from 5nm to 10nm. The slopes of the characteristics are reduced when the tunneling current is added to the thermionic current, which is the effect of subthreshold swing increase discussed earlier. In addition to this, the current increase itself is very significant, which means the off current becomes unnacceptably high. At $L_g = 5nm$, the off current with quantum tunneling is more than three orders of magnitude higher than the thermionic current.

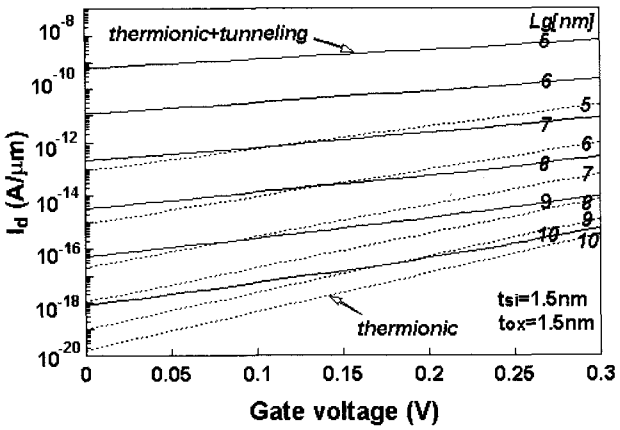

Fig. 3 Drain current in the subthreshold regime at $V_{ds} = 0.1V$ for different channel lengths, illustrating the contribution of quantum tunneling to the total current.

3.3 Threshold voltage roll off

To validate the variation of threshold voltage with gate length, obtained from the proposed model, the results of our model are compared to the results of 2D numerical simulation avaliable in the literature[5].

Figure 4 shows that there is a good agreement between this model and the numerical simulation. Thus, it can be concluded that the proposed model takes into account the electrostatic effects very well and that it is suited for calculations of the threshold voltage of small-geometry DGMOSGETs. Figure 4 also shows that the SCE is increased by the quantum tunneling. These results clearly show the importance of the tunneling current in the nano-scaled DGMOSFET for analysis of SCEs such as the threshold voltage roll off. Again, the effects of tunneling become pronounced for DGMOSFETs with gates shorter than 10nm.

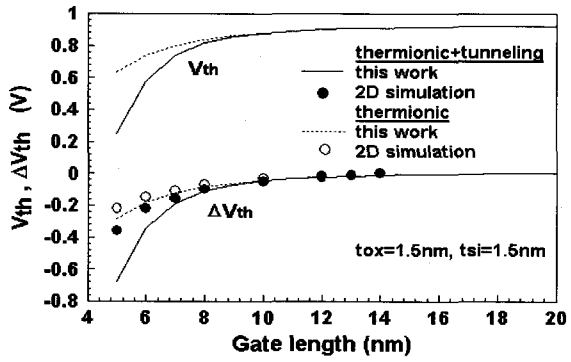

Fig. 4 Threshold voltage roll off as a function of the gate length in DGMOSFET with channel thickness of $t_{Si}=1.5nm$ and gate oxide thickness of $t_{ox}=1.5nm$. The results of the proposed model are verified by 2D numerical simulation.

3.4 Drain induced barrier lowering ; DIBL

The threshold voltage dependence on drain bias is important for digital applications. DIBL causes the threshold voltage to be a function of the operating voltages. Positive drain voltage corresponds to a reverse bias of the pn junction between the channel and the drain, increasing the width of the depletion region. A smaller gate voltage is therefore able to cause strong inversion, causing leakage and even punch through in some cases. DGMOSFETs have to be designed for minimum DIBL. Using the proposed model, DIBL is calculated and ploted as a function of gate length in Fig. 5. We can see that the DIBL is increasing due to quantum tunneling for gate lengths below 12nm. Usually, DIBL is proportional to the channel thickness and the gate oxide thickness, and inversely proportional to the gate length.

The slope is approximately -3, which is related to the fact that the punch through voltage has an L_g^3 dependence. However these relationships no longer hold for the case of thinner gate oxides such as $t_{ox}=0.5nm$ and especially gate lengths of over 10nm. Note that the DGMOSFET having the gate length of below 10nm influences on dependence L_g^3 due to quantum tunneling. Note DIBL is very sensitive to gate length in the regime of lower gate oxide thickness.[6]

IV. CONCLUSIONS

The model for analyzing SCEs such as subthreshold swing, threshold voltage roll off, and DIBL of nanoscale DGMOSFETs has been proposed in this paper. The results of this model have been compared to 2D numerical simulation to verify the

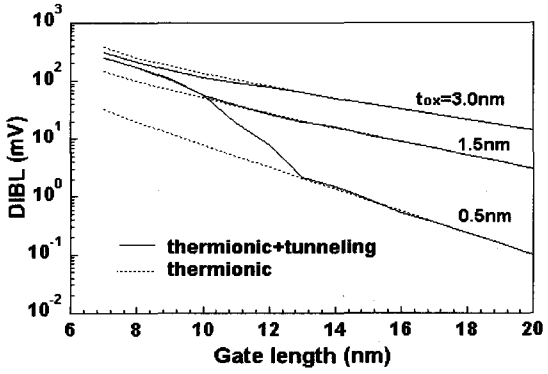

Fig. 5 DIBL as a function of gate length

model. Various calculations have been performed to investigate whether our approach can properly model the quantum tunneling between the source and drain in DGMOSFETs in the subthreshold region. A variety of DGMOSFETs with gate lengths ranging from 5nm to 20nm have been studied.

We have firstly analyzed the off current in the subthreshold region using the proposed model, in which the subthreshold current consisted of thremionic emission and quantum tunneling components. The thermionic emission has been found as the main mechanism of carrier transport for channel lengths above 10nm. On the other hand, quantum tunneling is dominant in DGMSOFETs with gate lengths below 10nm, and it significantly influences the device scaling, especially in the sub-10nm region. The degradation of SCEs due to quantum tunneling has been analyzed using the proposed model. To analyze SCEs, we have calculated subthreshold swing, threshold voltage roll off, and DIBL. We have observed that as the gate length is reduced, there is a corresponding degradation of SCEs, which becomes very significant in the sub-10nm region when the quantum tunneling becomes dominant.

As shown by the results, design rules have to be very strict in DGMOSFETs having gate lengths below 10nm since smaller channel thicknesses and gate oxide thicknesses are necessary. The results demonstrate that scaling limit due to quantum tunneling should be about 10nm for channel thicknesses below 1.5nm.

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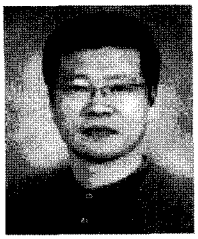

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