The Characterizing Analysis of a Buried-Channel MOSFET based on the 3-D Numerical Simulation

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Abstract - A depletion-mode MOSFET has been analyzed to evaluate its electrical behavior using a novel 3-D numerical simulation package. The characterizing analysis of the BC MOSFET was performed through short-channel narrow-channel and small-geometry effects that are investigated, in detail, in terms of the threshold voltage. The DIBL effect becomes significant for a short-channel device with a channel length of < 3(μm). For narrow-channel devices the variation of the threshold voltage was sharp for <4(μm) due to the strong narrow-channel effect. In the case of small-geometry devices, the shift of the threshold voltage was less sensitive due to the combination of the DIBL and substrate bias effects, as compared with that observed from the short-channel and narrow-channel devices. The characterizing analysis of the narrow-channel and small-geometry devices, especially with channel width of < 4(μm) and channel area of < 4×4(μm^2) respectively, can be accurately performed only from a 3-D numerical simulation due to their sharp variations in threshold voltages.

Keywords: Buried-channel MOSFET, Deep Depletion MOSFET, Narrow Channel Effect, Short Channel Effect, Small-Geometry Effect

1. Introduction

At present, a two-dimensional (2-D) device simulation is commonly used to analyze CCD characteristics. Due to the advancement of ULSI technology, the device is now much more miniaturized for higher packing chip densities than before, and thus the physical effects characterizing them are also more complicated. Such a trend requires a three dimensional (3-D) simulation approach to be able to solve insufficiently established physical phenomena such as the channel narrowing effect, drain-induced barrier lowering (DIBL) and small geometry effect.

As the channel length and/or width of the device becomes shorter and/or narrower, the physical mechanisms associated with the geometry effects become more complicated. The geometric-induced effects are usually interpreted by an analytical model with a number of assumptions for a simple calculation, which may result in an inaccurate prediction. The channel width is then always assumed to be infinite to perform a 2-D analysis. The potentials and electric fields generated near the surface and/or bulk channel play a very important role for characterizing the channel current and thus determining the output characteristics of the device. They are strongly dependent on the variations of both channel length and width.

Many efforts have been made to assess the short-channel effect through the variation of the threshold voltage due to a DIBL. The effect occurs in surface- and buried-channel devices when the channel length becomes significantly decreased and the depletion regions surrounding the source/drain diffusions is then much closer to each other, even for a very low drain voltage, resulting in a shift of the threshold voltage.

Extensive studies for this effect have been performed to find a relationship between the threshold voltage shift and the channel-length reduction by analyzing the subthreshold current as a function of channel length [1-4]. Van der Tol [4] has demonstrated that the DIBL effect is more sensitive to the threshold voltage shift for depletion-made devices than for surface-channel devices. This effect becomes more prominent as the channel length enters a sub-micron dimension [5, 6]. This is because the distance between the source and drain regions becomes much shorter, thus resulting in a significant reduction of the threshold voltage.

For channel-narrowing effect a few researches have been performed to assess the threshold voltage shift as a function of channel width for BC MOSFETs [5, 7-10]. Ballay et al. [5] have extensively studied the short channel and narrow channel effects, in which they demonstrated that the former effect allows the decrease of the threshold

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voltage due to an increased channel charge, while the latter effect results in its increase because of the reduced channel charge. Burkey et al. [7] and Fichtner et al. [11] demonstrated that for depletion-mode MOSFETs the narrowing channel effect becomes more pronounced when a channel width is reduced to less than 2 (μm).

An effective channel area should be considered carefully to provide an accurate analysis for device characteristics. Such work is often required for small-geometry devices as well as CCDs. For CCDs, the short channel and/or narrow channel effects may hinder an optimized design since a charge handling capability is strongly dependent on the device geometry and thus the channel area [12, 13]. A determination of the effective channel length may be obtained by a charge pumping technique [14]. The effective channel width is determined by a plot of the channel conductance versus design mask width for several gate voltages [7].

In this paper, a 3-D numerical simulation of the depletion-mode devices is performed to observe the substrate bias effect through a shift in the inversion threshold voltages and threshold voltage as a function of the channel implant dose and to determine its doping profile. For an analysis of the effects of short-channel, narrow-channel, and small-geometry, a number of devices with different geometry structures are simulated. The effects are demonstrated, in detail, through a variety of pictures and graphic representations in terms of the threshold voltage. The physical models used (such as recombination and mobility) are described in reference [15]. For our simulation, the "EVEREST" finite-element simulation package [16] was chosen since it contains an advanced adaptive algorithm.

2. Description of the Device

A buried-channel MOSFET originates from a test structure of an EEV CCD02 device. The test transistor consists of a mask design length of 8(μm) and a mask width of 64(μm) as a channel dimension. An implanted dose of 1.27E12 (cm^{-2}) reaches the silicon through a gate oxide resulting in a peak doping concentration of 3.2E16 (cm^{-3}) at the surface. The implantation was performed at 1100°C for 30 min. The source/drain regions are formed using LDD (Lightly-Doped Drain) technology. The implanted dose reached in the silicon is 7E13 (cm^{-2}) producing a peak doping near the surface. This is achieved by a phosphorus implant at 120 (leV) through an oxide layer under a nitride layer with an annealing condition at 950°C for 30 min. As a result, an effective channel length of 7.6 (μm) is obtained due to the use of a standard deviation of 0.07 (μm). For our efficient simulation the channel width of the device is reduced to 16 (μm). The resulting narrow-channel effect due to the channel-width reduction is negligible since the channel potential difference between the simulation results with 16 (μm) and 64 (μm) showed about 0.1(V).

3. 3-D Simulation and Results of Deep Depletion Mosfets

3.1 The Numerical Simulation of the Device

A device structure of the BC MOSFET used in the simulation is shown in "Fig. 1". The geometrical structure consists of a gate length, L, and gate width, W, corresponding to 8 and 16 (μm), respectively, and a substrate thickness of 5.5 (μm). The source/drain regions are located on opposing sides of the gate area. A channel stop region is placed at the rear of the structure (along y = 0(μm)). In the structure, x, y and z indicate channel-length direction, channel-width direction and substrate-direction, respectively. It should be noted that the simulated device includes one-half of the analysis domain due to the symmetric structure with respect to the channel width.

During the simulation work a variety of BC MOSFETs with different geometry structures have been used to observe the geometric-induced physical mechanisms; the channel length varies from 1 to 8 (μm) and channel width varies from 1 to 16 (μm). For our simulation a p+ field-implant layer was formed by a boron doping implantation of 1.5E13 (cm^{-2}) under a field oxide thickness of 0.63 (μm). This results in a peak doping of 3E16 (cm^{-3}) near the surface. The implanted doping profile was the same as that used by Burkey et al [7].

A number of devices with different gate (or channel) lengths and gate widths have been simulated to observe a shift of the threshold voltage as a function of device geometry. This work is intended to provide a clear insight

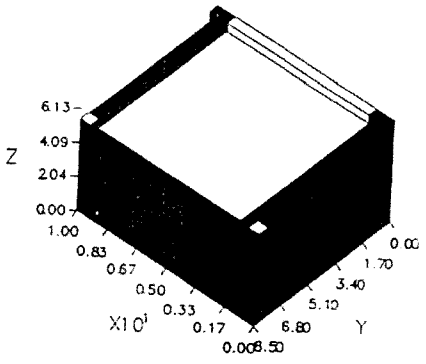

Fig. 1. A simulated structure of a BC MOSFET with a geometry: x = 10 μm channel length direction), y = 8.5 μm channel width direction) and z = 5.5 μm (thickness of substrate layer).

for short-channel and narrow-channel effects as well as to demonstrate that for small-geometry devices the short-channel and narrow-channel effects cannot be separately analyzed. The latter means that an accurate interpretation on the physical mechanisms in the small-geometry devices can be given only by 3-D analysis.

In this subsection we first discuss a short-channel effect and then a narrow-channel effect in terms of variation of the threshold voltage. After that, a combined geometry effect of the short-channel and narrow-channel effects is observed for small-geometry devices. Here, the flat band voltage is assumed to be zero in our simulation.

3.2 Simulation Results

3.2.1 Short-Channel Effect

The DIBL effect becomes significant due to the reduced potential barrier as the channel length decreases. The depletions around the source and drain become merged together when the length is very short; this then leads to a significant carrier injection from the source into the channel. This effect causes the turn-off point of the device to drop down to more negative voltage.

We have investigated the influence of the threshold voltage on the variation of the channel length. Variations of the threshold voltage against the channel length as a function of the drain-to-source voltage, V_{ds} and substrate voltage, V_{BS}, are illustrated in "Fig. 2". It was observed from Fig. 2 that the DIBL effect was much stronger than the substrate bias effect for L < 3(μm). The substrate bias effect causes the potential voltage to increase and is almost constant independent of the channel-length reduction.

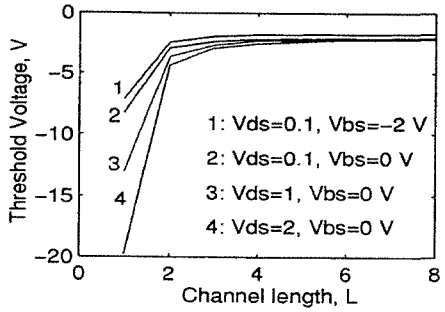

Fig. 2. Threshold voltage variation, describing the short-channel effect, for different channel lengths as a function of drain voltage or substrate voltage.

We have found subthreshold current characteristics and output characteristics to demonstrate the short-channel effect in terms of the drain current, which are illustrated in "Fig. 3". Fig. 3(a) shows a characteristic curve for Id versus Vg as a function of a channel length for V_{ds}=2(V), while output characteristics for Id versus Vd are illustrated in Fig. 3(b) where the gate voltage and source voltage are biased to –

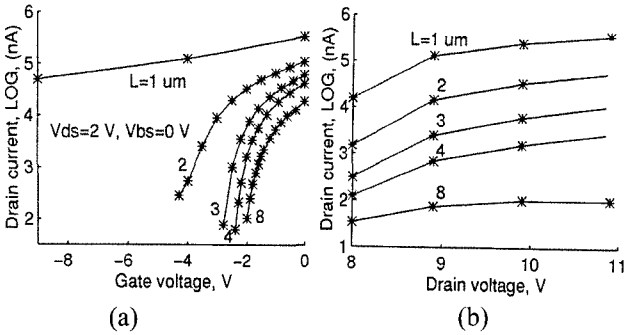

Fig. 3. Subthreshold currents (I_d versus V_g) (a) for different channel lengths of L=8, 4, 3, 2 and 1 μm and output characteristics (I_d versus V_d) (b) of the depletion-mode devices (V_{BS}=0, V_g=2.0 V and V_s=7.9 V).

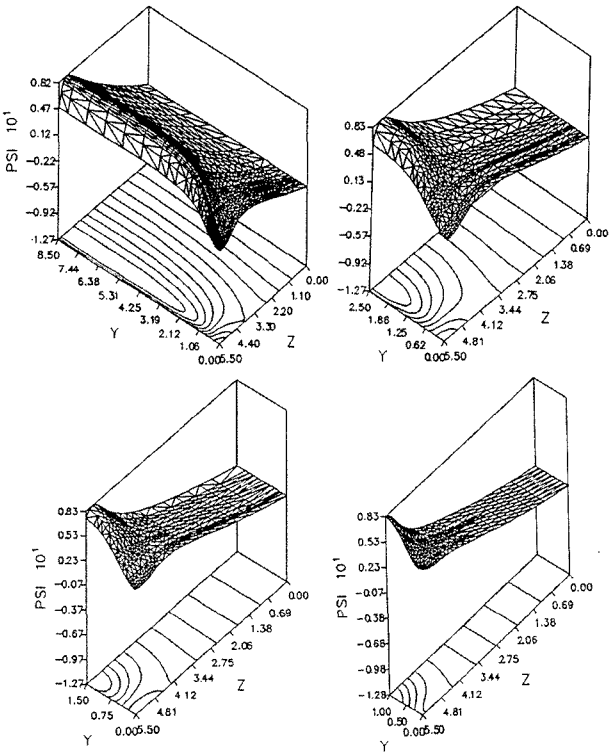

Fig. 4. 3-D isometric potential distributions, on the center of the channel effect: the surface potential is gradually decreased with decreasing the channel width. No surface potential barrier exists for W=1 μm. The devices are now operating at a pinch-off state. The gate voltages given as the threshold voltages for W=8, 4, 2 and 1 μm correspond to -1.72, 0.45, 4.12 and 9.12 V. The operating voltage conditions used here are: V_{ds}= 0.1 V (V_s=7.9 and V_d= 8 V) and V_{BS}= -2 V.

2(V) and 7.9(V), respectively. The substrate bias is then zero for the simulations. Both two characteristic curves confirm the short-channel effects discussed so far. It is clearly seen from Fig. 3(a) that the drain current curve for a device with L=1(μm) demonstrated a very low threshold

voltage (-19.8(V)) due to the significant short-channel effect. This is because a strong penetration of a drain field into the source resulted in a punch-through of the depletions near the source and drain regions even for V_{ds}=1(V).

3.2.2 Narrow-channel effect

Since the narrow-channel effect is usually ignored for a 2-D simulation an inaccurate estimation of a device performance occurs, especially for narrow-geometry devices. Thus, its thorough investigation using the 3-D simulation is required to achieve an optimal design of such practical devices. This effect is very important, especially in CCD applications, as it may bring a reduced charge handling capability. In addition, its careful consideration should be given, especially for CCDs with a reduced channel width, since during the parallel-to-serial charge transfer a parasite potential barrier may be produced due to the reduced width [17].

As the channel width becomes narrower the current path approaches the surface and a surface conduction may thus occur for a device with a very narrow channel width due to a reduction of the charge carriers in the channel. This narrow-channel effect leads to an increased threshold voltage. It is well known that the effective channel width is greatly dependent on the geometry, field-implanted dose, and operating voltage conditions (or operating modes of the device) [8, 18]. The effective channel width may be determined from a potential distribution extracted on the minimum point. Therefore, we will here demonstrate the narrow-channel effect in terms of the effective channel-width and threshold voltage variation.

For our purpose the channel width of the device, shown in Fig. 1, is varied from 1 to 16 (μm) to demonstrate the geometry effect clearly, while the channel length used for this analysis is fixed to be 8 (μm). "Fig. 4" illustrates isometric potential distributions, under the channel pinch-off state, for the different channel widths of W=16, 4, 2 and 1 (μm), which are produced on the center point of the channel length. For the simulations the drain-to-source voltage and substrate voltage were biased to 0.1 and –2(V), respectively, and the applied gate voltages were given as the threshold voltages.

The channel stop region is placed at the right-hand side ranging from 0 to 0.5(μm) (across the y-axis) where a densely refined mesh distribution is shown. It is clearly seen from Fig. 4 that a potential barrier between the potential minimum and the surface sharply decreases with decreasing the channel width. The channel potential and surface potential barrier are 8.18 and 3(V) for W=16 (μm), while for W=2 they are 8.28 and 0.8 (V), respectively. For W=1 (μm) no potential barrier exists, as shown in Fig. 4(d), resulting in a surface conduction.

The variation of the threshold voltage for different channel widths was observed as a function of V_{BS} and V_{ds}, which is demonstrated in "Fig. 5". It can be pointed out from Fig. 5 that the substrate bias effect is negligible for W < 4(μm) due to a close approach of the potential minimum towards the surface but becomes prominent for W> 4(μm). The drain field effect is insignificant for this analysis. The threshold voltage sharply increases for W< 4(μm).

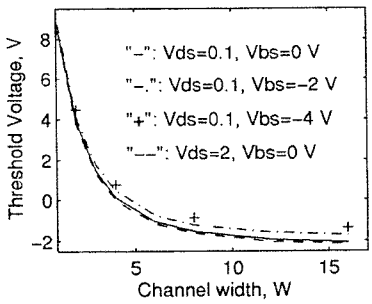

Fig. 5. The variation of the threshold voltage, describing the narrow-channel effect, for different channel widths as a function of a substrate voltage or drain voltage.

3.2.3 Small-geometry effect

Since small-geometry devices show a combined dependence of both short-channel and narrow-channel effects, it is much more difficult for one to understand the small geometry effect clearly. The 3-D isometric potential distributions on the potential minimum point are illustrated in "Fig. 6" where three different small-geometry devices of 8 (L) ×8 (W), 4×4 and 2×2 (μm^2) were simulated, which will, hereafter, be designated as A8, A4 and A2, respectively. The operating voltage conditions used for the simulation were given to operate the first device (A8) just below a pinch-off state. The drain-to-source voltage and substrate voltage are then biased to 2 and –2(V), respectively. The A4 and A2 are then operated at the subthreshold region. It can be demonstrated from the simulation that the channel potential becomes lower with decreasing channel area. The uniformity of the channel distribution becomes worse due to the reduction of the channel potential as the area decreases.

The potential reduction resulted from the combination of both short-channel and narrow-channel effects. However, for small-geometry devices the potential distribution along the channel-length direction follows that obtained from the narrow- channel devices. The only difference is that the channel potential is decreased with decreasing the channel area, compared with that observed from the narrow-channel device simulation. This is probably because the drain bias resulting in an increased potential barrier. Thus, the subthreshold current in the channel due to the DIBL effect is insignificant for a smaller-channel device.

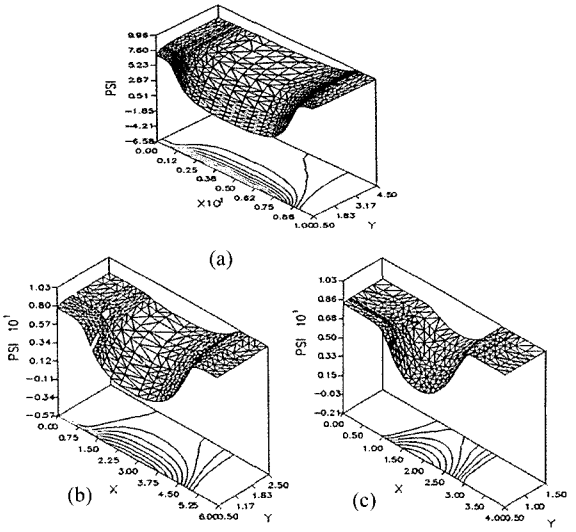

Fig. 6. 3-D isometric potential distributions on the potential minimum for (a) 8 (L) × 8 (W), (b) 4 × 4 and (c) 2 × 2 (μm^2) as A8, A4 and A2, respectively. A8 operates just below a pinch-off state, while A4 and A2 operate at subthreshold regions. The gate voltages used for A8, A4 and A2 are -1.25 V. The drain-to-source voltage and substrate voltage are then biased to 2 and -2 V, respectively.

It is of interest to observe the location of the potential minimum point from the corresponding current density distributions, which describes an operating mode of the device. The potential minima for A8, A4 and A2 are located at z=0.5, 0.38 and 0.32 (μm), respectively. The minima positions were comparable to those found from the narrow-channel devices. Thus, it can be clearly demonstrated from "Fig. 6" that as the area decreases the narrow-channel effect becomes the dominant factor and the operating mode of the small-geometry devices follows the narrow-channel devices. It was found from the simulated results that the potential barrier between the drain and source on the potential minimum point was 1.75(V) for A8, while for A4 and A2 it corresponded to 2 and 1.95(V), respectively. The DIBL effect is not so strong for >A1. This fact strongly supports that the narrow-channel effect plays a more important role for the small-geometry devices.

In "Fig. 7", the variation of the threshold voltage for different channel areas is shown as a function of V_{BS} or V_{ds}. It is pointed out from "Fig. 7" that its variation shows a stronger dependence on the drain bias effect than the substrate bias effect and is sharp for a channel area < A4.

Therefore, small-geometry effect including both short-channel and narrow-channel effects is significant for a channel area < A4. This means that the short-channel and narrow-channel effects should simultaneously be considered, otherwise the combined mechanism results in an unexpected characterizing analysis of the device.

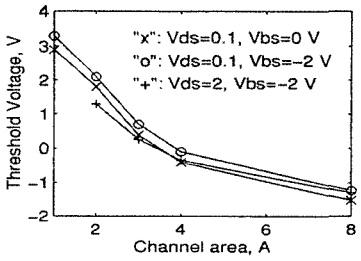

Fig. 7. Variation of the threshold voltage, describing small-channel effect, for different small devices of (a) 8 (L) × 8 (W), 4 × 4, 3 × 3, 2 × 2 and 1 × 1 (μm^2) as A8, A4, A2 and A1, respectively as a function of the substrate voltage and drain voltage.

4. Discussion

We have observed the short-channel effect, narrow-channel effect and small-geometry effect in terms of a variation of the threshold voltage. For a short-channel effect the threshold voltage was largely determined by the DIBL effect, which stimulates more carrier injection in the channel by reducing the potential barrier between the source and channel. The effect becomes more significant for a shorter-channel device. However, the potential, field and current density distributions in the channel along the transverse direction demonstrated a better uniformity for shorter-channel devices under the same voltage conditions. The uniformity of the current density distribution near the drain on the potential minimum point becomes worse with increasing the drain voltage due to the enhanced DIBL effect. This means that considerations for channel-width effect should be given due to the variation of the channel distributions for short-channel devices. For CCDs, which are always operated at a pinch-off state, the channel uniformity thus becomes significant since they often use a device structure with a channel length of > 4 (μm) and a very high drain (or diffusion) voltage. This mechanism can only be analyzed by a 3-D simulation. The subthreshold current characteristics and output characteristics confirmed the short-channel effect. The threshold voltage sharply varied for L <3 (μm). The device with L=1 (μm) indicated a punch-through of the depletions around the drain/source due to the strong penetration of the drain-induced field into the channel. Thus, DIBL effect is very significant for shorter-channel devices.

For narrow-channel devices, as the channel width becomes narrower the subthreshold current decreases due to the increase of the potential barrier between the source and channel resulting in the decreased charge carriers in the channel. This resulted in the increase of the threshold voltage. The location of the potential minimum gradually

approaches the surface due to the reduced surface potential barrier with the decreasing channel width. For W=1 μm the device operated as a surface-channel device due to no surface potential barrier. The effective channel width was much improved by reducing the p+-implanted dose. The widest effective channel width was achieved with zero implanted dose. Also, the use of the increased p+-implanted dose allowed an increase of the threshold voltage. It was demonstrated from the simulated results that the threshold voltage variation was sharp and the substrate bias effect was insignificant for W < 4 (μm). The DIBL effect was negligible for narrow-channel effect devices, as observed in "Fig. 5".

For small-geometry devices, the subthreshold current is negligibly lower due to the increased potential barrier, as observed in the case of the narrow-channel devices, as the channel area decreased. The DIBL effect was insignificant for a channel area of > A2 but becomes important for a channel area of <A2. The substrate bias effect becomes significant for a channel area of ≤A8. The uniformity of the channel along the transverse direction worsens and thus the effective channel width is narrower with decreasing the channel area. For Al it is operated under the punch-through of the depletions due to a strong short-channel effect, resulting in large current densities near the source/drain regions. The narrow-channel effect increased the threshold voltage due to the reduced channel carriers. The variation of the threshold voltage, describing the small-geometry effect, was very sensitive for a channel area of < A4.

5. Conclusion

A 3-D numerical simulation was performed to estimate the electrical behavior of the inverting depletion-mode devices used as a test transistor in the EEV CCD02 device. This simulation was done using a 3-D semiconductor device simulator "EVEREST", which leads us to perform a 3-D characterizing analysis of the device. The work was successfully performed because the simulator has a novel adaptive mesh technique and thus allowed a 3-D simulation of the large-geometry device. An accurate analysis was possible owing to sufficient local mesh refinement near the surface, the junction boundaries and high field regions, resulting in the reduction of the computation time and computer data storage requirements.

The 3-D simulation accurately analyzed the short-channel, narrow-channel and small- geometry effects in terms of a shift of the threshold voltage. The drain field effect is significant due to the DIBL effect with decreasing channel length, while the substrate bias becomes a dominant factor for narrow-channel devices. Both effects become important for small-geometry devices. It was strongly demonstrated from the simulated results that 2-D simulation cannot accurately perform the characterizing analysis of the narrow-channel and small-geometry devices, especially with W<4 (μm) and A<4×4 (μm^2), respectively. Also, for devices with a channel length of >4μm, 2-D simulation cannot trace a mechanism of the non-uniformity-induced threshold voltage shift (although it is not significant) when the device is operated at or above a pinch-off state.

Finally, a conclusion is drawn from the simulated results that the short-channel and narrow-channel effects cannot separately be considered and thus only 3-D simulation can estimate an accurate device performance. Thus, it can be demonstrated that the 3-D simulated results can also be used as an input data for a circuit simulation in CAD systems. And this simulator can be employed as a powerful tool for a new device development and for the characterizing analysis of sub-micron devices fabricated with ULSI technologies.

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