A 32nm and 0.9V CMOS Phase-Locked Loop with Leakage Current and Power Supply Noise Compensation

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Abstract—**This paper presents two novel compensation circuits for leakage current and power supply noise (PSN) in phase locked loop (PLL) using a nanometer CMOS technology. The leakage compensation circuit reduces the leakage current of the charge pump circuit which becomes more serious problem due to the thin gate oxide and small threshold voltage in nanometer CMOS technology and the PSN compensation circuit decreases the effect of power supply variation on the output frequency of VCO. The PLL design is based on a 32nm predictive CMOS technology and uses a 0.9V power supply voltage. The simulation results show that the proposed PLL achieves a 88% jitter reduction at 440MHz output frequency compared to the PLL without leakage compensator and its output frequency drift is little to 20% power supply voltage variations. The PLL has an output frequency range of 40M~725MHz with a multiplication range of 1-1023, and the RMS and peak-to-peak jitter are 5ps and 42.7ps, respectively.**

Index Terms—**Nanometer CMOS, Leakage Current, Power Supply Noise, Phase-Locked Loop (PLL)**

I. INTRODUCTION

The strong demand for low-power computing has been driven by a growing variety of portable and battery- operated electronic devices. These span a broad range of performance and functions with respect to throughput. Power consumption is a limiting factor in VLSI integration for portable applications. The resulting heat dissipation also limits the feasible packaging and performance of the VLSI chip. Since the dynamic power dissipation in synchronous digital integrated circuit is determined by CV^2f, reducing the supply voltage is an effective way to reduce power consumption of the modern electronic systems. As the supply voltage scales down with the technology, any power supply noise on power and ground level affects the analog circuit performance more than before. This power supply noise has a direct effect on the voltage controller oscillator (VCO) output frequency of PLL which is proportional to the control voltage from the charge pump. Therefore, this power supply noise is a critical issue to be resolved for better jitter performance of PLL [1][2].

In addition, due to the continued scaling of technology, the leakage power has become dominant in power dissipation of nanoscale CMOS digital circuits [3]. Since the analog electronics has to be on the same die as the digital core in contemporary mixed signal circuits, it has to cope with the nanoscale CMOS issues. Nanoscale CMOS technology has come to a point where new phenomena need to be taken into account for analog circuits.

As the nanoscale process advances, the gate-oxide thickness becomes thinner and the threshold voltage becomes lower. The leakage current in CMOS circuit design using nanoscale process has gradually become a

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significant issue [4][5]. In nanoscale CMOS process, the CMOS current is deeply affected by not only gate-source voltage (V_{gs}) but also drain-source voltage (V_{ds}) since the leakage current ($V_{gs}<V_T$, Cut-off MOS) is affected by drain-source voltage (V_{ds}). This makes the cascode current sink/source topology more desirable for the current mirror circuit in low power nanoscale circuit design. The leakage current increases with the transistor size of CMOS and the VCO output frequency is more sensitive to the leakage current and its control voltage (V_C) in high frequency operation. Therefore, for a large multiplication factor in PLL, the leakage current has a considerable effect on the control voltage (V_C) variation of the VCO after the large feedback cycle detection. Consequently, the leakage current is an important issue to be addressed for the PLL jitter performance [6].

The power supply noise (PSN) at the power/ground lines is another serious problem to be considered in the low power and high performance mixed mode systems since the on-chip power/ground voltage variation of the analog part increases due to the IR-drop and the *Ldi/dt* noise in digital part in spite of all the techniques to minimize them. This affects the functionality and performance of the analog circuit as well as the digital part, and may cause even circuit failure. The voltage drop also causes a smaller effective threshold voltage (resulting in an increased sensitivity to noise). Therefore, the power supply noise has a deep impact on the output frequency of PLL [7][8].

In this paper, a nanoscale CMOS PLL design using a 32nm CMOS technology is described, where low jitter performance is achieved using compensation circuits to reduce power supply noise effect on VCO output frequency and the leakage current in the charge pump. An MOS capacitor and an MIM capacitor are used for a big capacitance to save the chip area and a small capacitor in the passive second-order loop filter, respectively. To compensate the leakage current from the MOS capacitor a voltage feedback buffer is used in the loop filter, and a ring oscillator based VCO is used for a relatively small area and robustness over process and temperature variations.

The remainder of this paper is organized as follows. Section II illustrates the circuit diagram of the PLL, and Section III describes the proposed novel leakage compensation circuits. The proposed compensation circuit for power supply noise (PSN) is presented in Section IV followed by the results and comparison with other PLL in Section V, and the paper is concluded in Section VI.

II. Proposed PLL Circuit Design

Fig. 1 shows the proposed PLL with the compensation circuit blocks for leakage current and PSN. In addition to the conventional PLL blocks such as phase-frequency detector (PFD), charge pump (CP), loop filter (LF), voltage-controlled oscillator (VCO), and a frequency divider, the PLL in this paper includes the leakage compensator, the PSN compensator, and the voltage buffer block in the loop filter. The leakage compensation consists of two charge pump replicas and current mirrors. Using the UP/DN signals from the PFD and two bias voltages of charge pump, the leakage compensator senses the leakage current of the charge pump circuit and generates the same amount of current as the leakage current of the charge pump. However, the directions of the generated leakage current are opposite to those of the leakage current in the charge pump. That is how the leakage current of the charge pump is cancelled through the leakage compensator.

The PSN compensation circuit consists of n-stage inverters and current differential amplifiers. The inverters are used to monitor the propagation delay which is variable depending on PSN. The number of stage of the inverter chain is determined based on the power supply voltage noise range and the inverter delay.

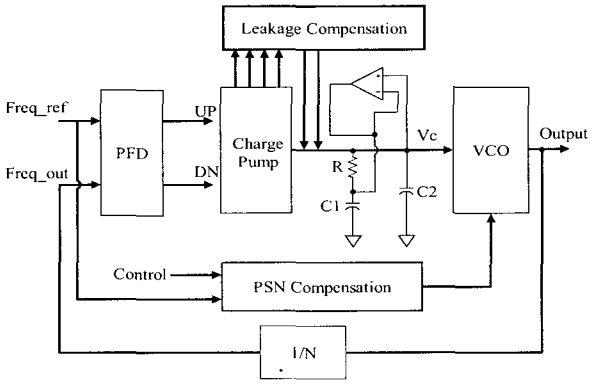


Fig. 1. Block diagram of the proposed PLL.

The current differential amplifiers convert the difference between the nominal propagation delay and the monitored actual propagation delay to current. The generated current is added to or subtracted from the current source in the VCO depending on the PSN polarity to adjust the VCO output frequency. The input signals of the PSN compensator are the control signal to enable the circuit and the reference clock, and the reference clock is propagated through the inverter chain.

1. Charge Pump

Fig. 2 shows the circuit schematic of the charge pump. The main charge pump is composed of MP6, MP7, MN6, and MN7. MP4,5(MP8,9). MN8,9(MN4,5) are the gain boosting stages to increase the output resistance of the charging and discharging current sources. In Fig. 2, the resistor, R_{bias}, MP1, and MN1 generate the bias current. When the UP (DN) signal is high, MP2 (MN2) turns on and MP6 (MN6) turns on. When the UP (DN) signal is low, MP3 (MN3) turns on and MP6 (MN6) will turn off. MP7 and MN7 are operated as current sources in the charge pump. UP1/UP_bias signal and DN1/DN_bias signal are used to replicate the leakage current of the charge pump in the leakage compensation circuit.

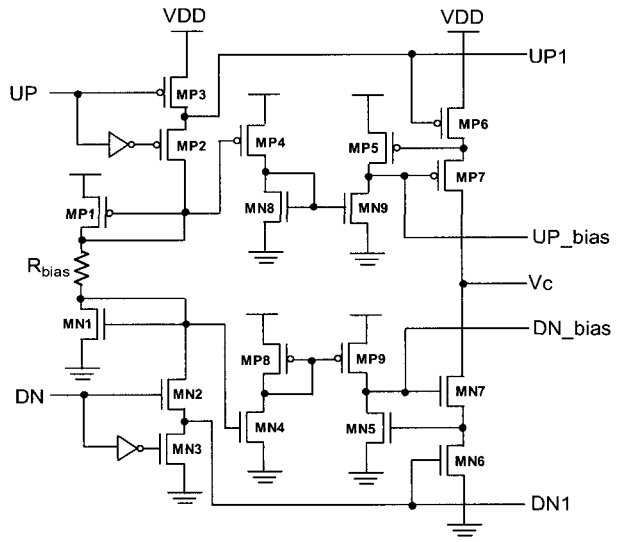


Fig. 2. Block diagram of Charge Pump.

2. Loop Filter and Frequency Divider

The PLL uses the low pass filter to filter out the high frequency component of phase error signal and noise. With the second-order loop filter, the PLL system is more stable and has less noise. The transfer function of the filter is given by,

$$H(s)=\frac{sC_1R+1}{s(SC_1C_2R+C_1C_2)} \quad (1)$$

To save the active area and reduce the leakage current, an MOS capacitor is used for the big capacitor (C1) in the loop filter and an MIM capacitor is used for the small capacitor C2. Since the leakage current from the MIM capacitor (C2) is much smaller, it can be neglected. However, the leakage current from the big MOS capacitor (C1) needs to be considered, and a voltage buffer is used to compensate the leakage. In Fig. 1, when the PLL is in the steady state, the voltages *Vc* and the charged voltage of C1 are almost equal to each other. Since this voltage buffer has to drive the big MOS capacitor C1, the dominant pole is moved to the output stage. The bandwidth of this voltage buffer is around 1/10 times that of the PLL. An integer-N frequency divider is used to change the input frequency range, to increase the signal integrity, or to multiply the input frequency [9].

3. VCO

The VCO is designed to operate at low supply voltage. As shown in Fig. 3, the VCO consists of a cascode self-biasing current source and a current starved ring oscillator with 11-stage of inverters

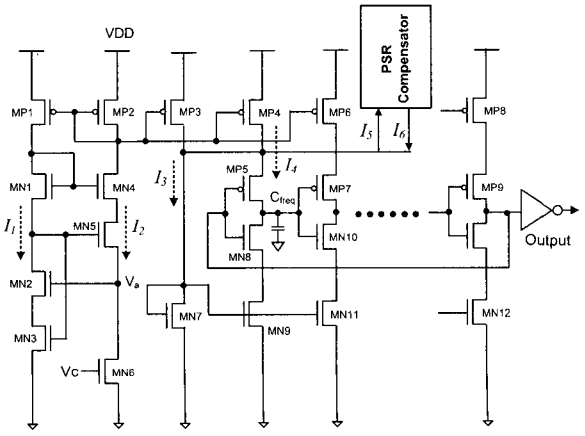


Fig. 3. Proposed VCO.

In the cascode self-biasing current source, V_a is determined by the gate-source voltage of MN3 and MN5. It is given by

$$V_a = Vgs_{(MN3)} - Vgs_{(MN5)} = \sqrt{\frac{2I_{(MN3)}}{\beta_{(MN3)}}} + V_{th(MN3)} - \left[\sqrt{\frac{2I_{(MN5)}}{\beta_{(MN5)}}} + V_{th(MN5)}\right] \quad (2)$$

where $V_{th(MN3)}$ is greater than $V_{th(MN5)}$ because the body bias of MN3 is connected to non-zero voltage(body effect), and $W/L_{(MN3)}$ is greater than $W/L_{(MN5)}$. Therefore, the first and last terms of the Equation (2) are much smaller than the third and second terms, respectively. Therefore, those two terms may be ignored and the Equation (2) can be rewritten as Equation (3).

$$V_a = V_{th(MN3)} - \sqrt{\frac{2I_{(MN5)}}{\beta_{(MN5)}}} \quad (3)$$

Equation (3) gives an insight about the V_a variation due to temperature. If $I_{(MN3)}$ and $I_{(MN5)}$ are equal and independent of temperature, the low temperature dependence of V_a is obtained to a certain extent since the negative temperature coefficient of the mobility and the negative temperature coefficient of the threshold voltage can reduce the temperature variation of V_a.

The current on MN6 is given by

$$I_{(MN6)} = I_1 = I_2 = \frac{V_a}{R_{(MN6)}} = V_a \times \left[\beta(V_c - V_{th(MN6)})\right] \quad (4)$$

where $R_{(MN6)}$ is the resistance of MN6 in the triode region.

Finally, a constant current I_4 is generated by the current source and applied to the VCO ring oscillator to control the VCO frequency. If any voltage variation is detected through the PSN compensator circuit described in Section IV, I_5 and I_6 are added or subtracted from I_4 and I_3 depending on the direction of the PSN polarity.

III. LEAKAGE COMPENSATION

The leakage current will increase drastically when migrating to the advanced nanoscale technologies. Many researchers have looked at the leakage effects on the digital circuit performance with the scaled gate oxides. However, few researchers looked at the effect of the gate leakage on analog circuit performance. As scaled CMOS is promising for system-on-chip applications, it is essential to look at the performance of the scaled CMOS technologies for analog applications by including the leakage constraints. Furthermore, longer channel length devices is often used for analog circuits to maintain the adequate output resistance, which increases the gate leakage current as it is proportional to the gate area.

1. Leakage Components in Nanoscale CMOS Circuits

In the off-state, the main components of leakage current are the subthreshold leakage (I_{Subth}), the gate induced drain leakage (I_{GIDL}), the gate tunneling leakage (I_{GATE}), and the band-to-band (BTBT) tunneling (I_{BTBT}) as shown in Fig. 4(a). In the on-state, the gate tunneling leakage (I_{GATE}) is the main component as shown in Fig. 4(b) [3]. The GIDL (Gate Induced Drain Leakage) is the current from drain to substrate caused by the high electric field between the gate and drain, and the thin gate oxide thickness and the high supply voltage increase the GIDL leakage. The gate tunneling leakage is a current flowing into the gate of transistor by tunneling effect, and the thin gate oxide thickness and the high supply voltage increase the gate tunneling leakage. The subthreshold leakage is a weak inversion conduction current that flows between the source and the drain of CMOS transistor when $V_{gs} < V_{th}$.

It increases exponentially due to the reduced threshold voltage, and it is the main leakage component in high forward body bias that is often used to reduce threshold voltage. Finally, the BTBT leakage is the current due to

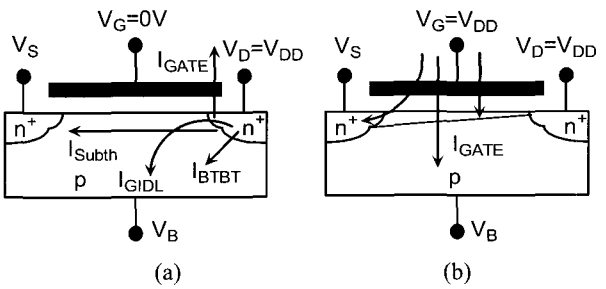


Fig. 4. Leakage current in nanoscale CMOS circuits: (a) OFF-state leakage components (b) ON-state leakage components.

electron tunneling across the reverse biased p-n junction between drain/source and substrate of CMOS transistor. Therefore, in the high reverse body bias, the BTBT leakage becomes a major contributor to the total leakage currents.

2. Leakage Compensation Circuit

The replica charge pump is composed of MP1, MP2, MN1, and MN2 as shown in Fig. 5. Fig. 5(a) presents the leakage generator circuit for the PMOSFETs of charge pump, and Fig. 5(b) is the leakage generator circuit for the NMOSFETs of charge pump (CP). For the PMOSFETs of the charge pump, the leakage current (I_1) is generated by "HIGH" UP1 signal, and its mirrored current I_2 flows through MN6 (ON state). The current I_2 which is exactly the same as the leakage current is subtracted from the node Vc to offset the PMOSFETs' leakage current of charge pump, resulting in the lower VCO control voltage Vc. The operation of Fig. 5(b) is the same as that of PMOSFETs.

The compensator uses the self-cascode current mirror for low voltage operation. The self-cascode structure (MN4 and MN5) provides a high output impedance with a larger voltage headroom than the conventional cascode scheme. The MN4 and MN5 can be treated as a single composite transistor. The composite structure has much larger effective channel length, and the effective output conductance is much lower. The lower transistor MN4 is equivalent to a resistor whose value is dependent on the bias voltage. For optimal operation, the W/L ratio of MN5 is kept larger than that of MN4, that is, $m > 1$

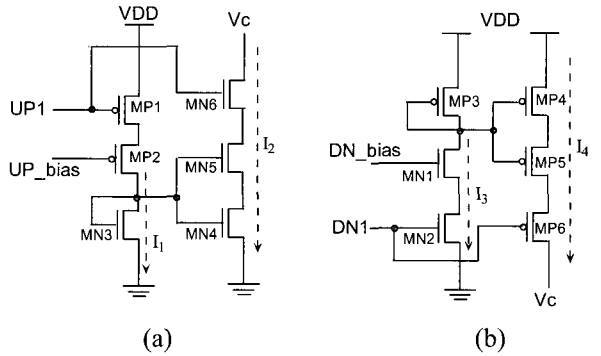


Fig. 5. Proposed Leakage compensator with CP replica: (a) Leakage compensator for PMOSFETs (b) Leakage compensator for NMOSFETs.

(m is the W/L ratio of the transistor MN5 to MN4). For the composite cascode structure, the effective transconduc tance($g_m(effective)$) will be g_{m5}/m, which is equivalent to the transconductance of MN4(g_{m4}). Then, the drain current (I_D) through MN4 and MN5 will be $\beta_{effective}\ (V_{in} - V_T)^2 / 2$, where $\beta_{effective}$ equals $\beta_4\beta_5 / (\beta_4 + \beta_5)$, which can be approximated by β_4 when m is large [10].

The voltage between source and drain of MN4 is small, and there is no appreciable difference between the V_{DSAT} of composite and simple transistors, and a self-cascode can be used in low voltage operation. For a self-cascode $V_{DSAT} = V_{DSATM4} + V_{DSATM5}$. The operating voltage of a regular cascode is much higher than that of a self-cascode. The self-cascode current mirror satisfies the requirements to compensate the small leakage current due to the advantages offered by the self-cascode structure offering high output impedance similar to that of the conventional cascode structure while the output voltage requirements are similar to those of a single transistor.

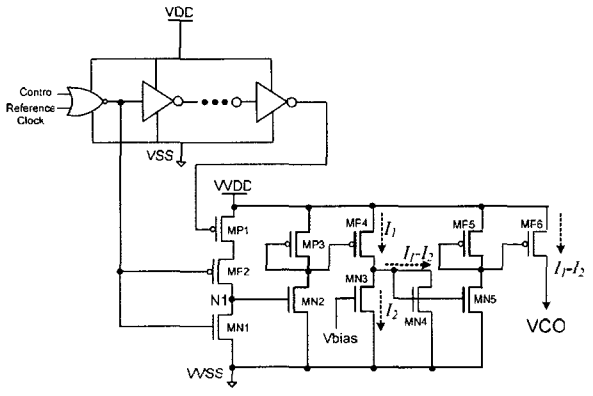
IV. PSN Compensation

Although the supply voltage has been reduced down to below 1.0 V, it is still possible to design most of the circuits. However, a further drop in supply voltage is expected to cause serious problems for circuits, especially analog circuits because the signal voltage becomes too small to design circuits with sufficient signal integrity at reasonable power consumption levels. This leaves much heavier burden to analog circuit design engineer since the voltage headroom becomes smaller and the reduced voltage headroom makes the circuit more sensitive to any power supply noise. Especially, in Very-Deep-Submicron (VDSM) high speed mixed mode circuit, the on-chip power-ground voltage variation is affected by the IR-drop and the Ldi/dt noise in digital part despite all the techniques to minimize them. This affects the performance of both analog and digital blocks due to the increased delay as a result of the lowered supply. The voltage drop also causes a smaller effective threshold voltage (resulting in an increased sensitivity to noise) [7][8].

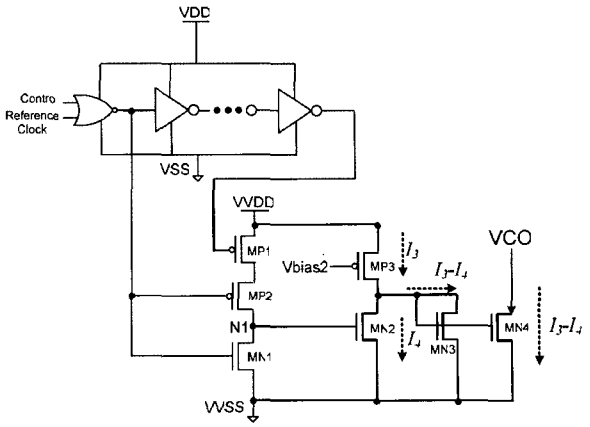
The main idea of the proposed PSN compensator is to monitor the power supply noise through its effect on the

propagation delay of the inverter chain to compensate the charge pump output voltage error caused by the PSN. Fig. 6 shows the circuit schematic of the proposed PSN compensator for the positive and negative variations of power supply. The n-stage inverter chain works as a delay line, whose delay depends on its effective supply voltage (in this research seven stage is used). In PLL circuit, the PSN compensator is triggered by the control signal and reference clock is used as the input to the inverter chain delay line. The NOR gate works as a control gate to operate the compensator when desired.

Transistors MP1 and MP2 work as switches connected in series between voltage *VVdd* and *N1*. *VVdd* comes from a local capacitor which is large enough to keep the constant voltage. When the reference clock is at "1" and the control signal is at "0", switch MP2 is open and MP1 is closed. The rising edge of the clock line closes switch MP2, and a current begins to flow to N1 node. This current charges the gate capacitor of M2 until the output signal of the inverter block changes, opening the switch MP1. Thus, the total charge supplied to N1 node is proportional to the propagation delay of the inverter block. As the propagation delay depends on the effective supply voltage seen by this block, the voltage of N1 at the end of the sampling period also depends on the supply voltage. As the power/ground bounce is produced just after the clock edge, the voltage of N1 will be dependent on the power/ ground bounce: the higher the supply voltage drop is, the longer the propagation delay and the higher the voltage of N1 and I_1 will be. If the effective supply voltage is higher due to the positive PSN noise, the voltage of N1 and I will be lower as the propagation delay becomes slower.



(a)



(b)

Fig. 6. Proposed PSN compensation circuit: (a) Negative variation (b) Positive variation.

The compensator samples the PSN during a time interval that is much shorter than the duration of the PSN. The sampling time of the compensator corresponds to the moment when a rising edge is produced in the reference clock. By introducing a programmable delay line from the control signal to the NOR input, the sampling moment can be changed and the samples of the voltage of N1 at different times are obtained to check the PSN in the whole clock cycle.

In addition, a current mirror and current differential amplifier are added to convert the voltage of N1 to current. In Fig. 6(a), I_1 is the current which is proportional to the voltage of N1, and I_2 is the reference current generated when the inverters have a normal power supply without PSN. If the power supply is reduced by PSN, the propagation delay of the inverter chain will increase, and the output frequency of PLL will decrease. Therefore, if I_1-I_2 in the current differential amplifier is added to the cascode self-biasing current source in the VCO block, and the VCO output frequency will increase in proportional to the current difference. The circuit to compensate positive PSN is shown in Fig. 6(b). In this case, the I_3-I_4 has to be subtracted from the cascode self-biasing current source in the VCO to decrease the output frequency of VCO.

V. EXPERIMENTAL RESULTS

The circuit is designed in a 32*nm* PTM BSIM4 technology [11]. Correct operation and performance of

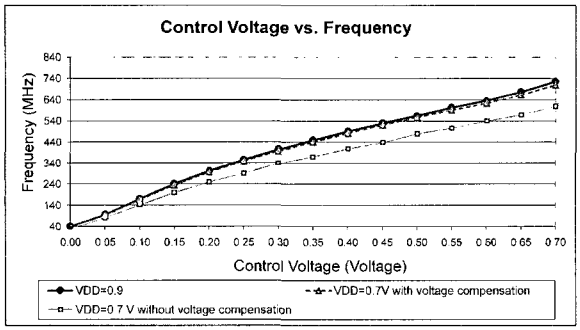


Fig. 7. Frequency vs. Control voltage of the proposed VCO.

the circuit design are verified through simulations. The proposed VCO operates from 40 MHz to 725 *MHz* at $0.9V$ supply voltage

When the temperature is changed from -25°C to 75°C, the VCO frequency variation is within 8%. The linear relationship between the frequency and control voltage is shown in Fig. 7. As the control voltage increases from $0V$ to $0.7V$, the current increases linearly. The VCO gain is $0.48MHz/1mV$, and the center frequency is $450MHz$. 10% supply voltage change causes only 9.3% frequency change ($\pm$ $21MHz$ from the center frequency).

In Fig. 7, the frequency vs. control voltage is shown for different power supply voltages. If *VDD* is changed from $0.9V$ to $0.7V$, the frequency decreases as expected. On the other hand, if the proposed PSN compensator is used in the same power supply voltage ($0.7V$), the frequency is almost the same as the case with $0.9V$ power supply voltage. Fig. 8 shows the frequency spectrum of the VCO with and without the PSN compensator. Two important phenomena are observed. First, the phase noise of the VCO output is significantly increased when the PSN compensator is not used. Secondly, the center frequency is shifted when power supply noise is induced affecting the accuracy of the PLL.

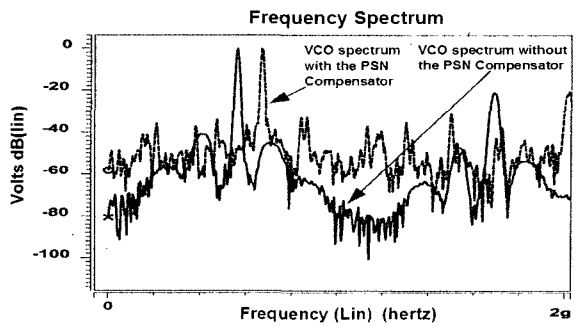


Fig. 8. Output spectrum of VCO with and without PSN compensator.

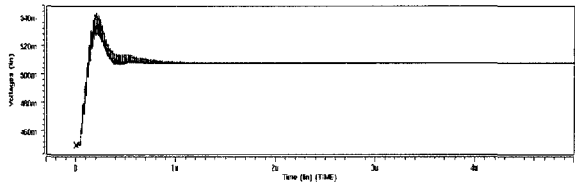


Fig. 9. Closed loop VCO input control voltage.

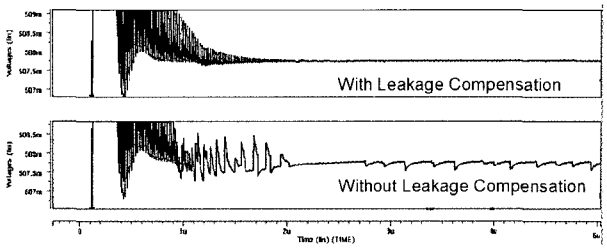


Fig. 10. VCO input control voltage of charge pump with and without leakage compensation.

Fig. 9 shows that the control voltage of the VCO reaches its locked state when the frequency of VCO is $725MHz$. Fig. 10 shows the control voltage of the PLL for both cases where the leakage compensation circuit is employed and the compensation circuit is not employed to compare the cases when the frequency of VCO is $725MHz$.

The proposed PLL performance is compared with a previously published PLL as shown in Table I. It is demonstrated that the new PLL reduces timing jitter significantly while providing other comparable PLL performance. The variation of the control voltage in the conventional PLL is about 1mV and the variation of the control voltage in the proposed PLL using leakage compensator is much less than $1mV$.

Table 1. Performance summary.

Performance Summary			
Reference		This Work	[6]
Process		32nm	0.13um
Supply Voltage		0.9V	1V
Reference Frequency Range		0.4M~10MHz	X
Output Frequency Range		40M~725MHz	10M~700MHz
RMS Jitter (peak-to-peak) at 440MHz	Charge Pump with Leakage Compensation	5ps (42.6ps)	24.3ps(155ps) at 360MHz
	Charge Pump without Leakage Compensation	40.9ps (242ps)	X

VI. CONCLUSIONS

The proposed compensation is designed in 32nm PTM (Predictable Technology Model) BSIM4 model. A novel leakage compensation circuit technique is presented to reduce the jitter caused by the transistor leakage current. The leakage compensator effectively improves the jitter performance of the conventional PLL in nanometer technology. To compensate the power supply noise effect on VCO, the effect of the noise is detected using an inverter chain and the power supply noise effect is compensated by the PSN compensator. The PSN compensator and leakage compensator provide the PLL with better performance and independence of power supply variation by reducing the jitter and increasing the output frequency range of the VCO. The proposed circuit techniques will be a good reference for the future mixed mode circuit design research in nanoscale CMOS integrated circuit design.

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