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저전압 고선형 바이폴라 OTA와 이를 이용한 IF 대역통과 필터

(Low-voltage high-linear bipolar OTA and its application to IF
bandpass Filter)

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요 약

GSM 셀룰러폰을 위한 저전압 고선형 바이폴라 OTA와 이를 이용한 IF bandpass filter(BPF)를 제안하였다. OTA는 저전압 선형 transconductor, translinear 전류이득 셀, 그리고 3개의 전류 미러로 구성 되어있다. BPF는 2개의 동일한 2차 BPF를 직렬 연결한 형태인데, 2차 BPF는 저항과 커패시터 그리고 2개의 OTA와 커패시터로 된 ground simulated inductor로 구성되어 있다. 8GHz bipolar transistor-array를 사용한 SPICE 시뮬레이션에서는 1mS의 transconductance의 OTA가 $\pm 2\%$ 이하의 선형 오차와 ± 2 V에서 ± 0.65 V이상의 선형범위를 가짐을 보여준다. transconductor의 온도계수는 $-90\text{ppm}/^\circ\text{C}$ 이하이다. BPF는 중심 주파수는 85MHz Q값은 80이 되도록 설계하였다. 중심주파수에서의 온도계수는 $-182\text{ppm}/^\circ\text{C}$ 이고, BPF의 소비전력은 128mW이다.

Abstract

A low-voltage high-linear bipolar OTA and its application to IF bandpass filter for GSM cellular telephone are presented. The OTA consists of a low-voltage linear transconductor, a translinear current gain cell, and three current mirrors. The bandpass filter is composed of two cascaded identical second-order bandpass filters, which consist of a resistor, a capacitor, and a grounded simulated inductor realized with two OTA's and a grounded capacitor. SPICE simulations using an 8 GHz bipolar transistor-array parameter show that the OTA with a transconductance of 1 mS exhibits a linearity error of less than $\pm 2\%$ over an input voltage range of ± 0.65 V at supply voltages of ± 2.0 V. Temperature coefficient of the transconductance is less than -90 ppm/ $^\circ\text{C}$. The bandpass filter has a center frequency of 85 MHz and Q -factor of 80. Temperature coefficient of the center frequency is less than -182 ppm/ $^\circ\text{C}$. The power dissipation of the filter is 128 mW.

Keywords: Linear operational transconductance amplifier; Simulated inductor; IF bandpass filter

I. Introduction

Operational transconductance amplifiers (OTA's) are essential elements in the design of electrically tunable amplifiers, filters, oscillators, and other current-mode signal processing. There are two

important limitations with the commercial OTA's like the LM3080 and CA3080: one is their severe harmonic distortion for larger input signal caused by the nonlinear characteristic of the emitter-coupled differential input pair^[1]; the other is their temperature dependency caused by temperature-sensitive transistor parameters^[2-3]. The simplest way of solving these problems is the use of the improved OTA's with on-chip diode linearization, like the LM13600 and CA3280^[1]. However, in order to achieve

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the improved performance with these devices, exactly matched resistors or elaborate trimming of a potentiometer is required.

In recent years, a bipolar linear OTA to overcome these problems has been reported^[4]. This linear OTA exhibits linear transfer characteristic over the entire bias current range and good temperature stability. In addition, its transconductance is linearly dependent on a bias current varying over four decades. A major disadvantage of the linear OTA is its relatively small linear input range caused by small common-mode input range. The larger device count and power dissipation is another factor which restricts its usefulness in low-voltage low-power applications.

This paper describes an improved bipolar linear OTA suitable for low-voltage low-power applications. It consists of a low-voltage linear transconductor, a translinear current gain cell, and three current mirrors. This improved OTA exhibits simpler configuration and higher linearity than the previous work. In order to test its applicability, the OTA is used to implement a fourth-order bandpass filter for the first IF receiver stage for GSM (global system for mobiles) cellular telephone.

II. Low-voltage bipolar linear transconductor

1. Limitation of the conventional bipolarlinear transconductor

The circuit configuration of a conventional bipolar linear transconductor reported in [4] is shown in Fig. 1. The operation principle of the circuit is to cancel out, by using local current feedback, the base-emitter junction voltages of the emitter-coupled pair with emitter degeneration. This makes the entire input voltage appear on the emitter-degeneration resistor R_E , and hence the circuit performs a linear voltage-to-current conversion given by

$$i_{OUT} = i_{C1} - i_{C2} = \frac{v_{IN}}{R_E} \quad (1)$$

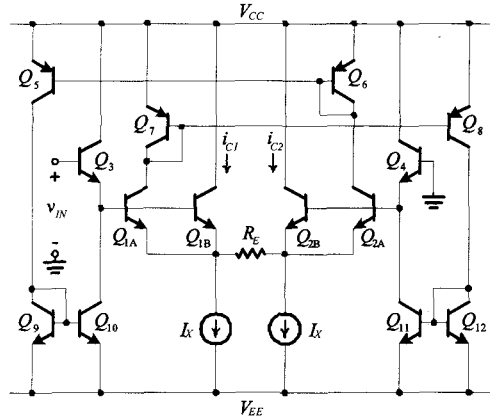


그림 1. (Chung *et al.* 1990a) 논문에 있는 기존의 바이폴라 선형 transconductor

Fig. 1. Conventional bipolar linear transconductor of (Chung *et al.* 1990a).

The input range of the circuit is limited by $|v_{IN}| \leq R_E I_X$ or the input common-mode range. The common-mode range of the differential input terminals is limited by the current sources I_X leaving active mode of operation.

Thus the voltages at both terminals should be smaller than $|V_{EE} + 2V_{CEsat}|$ for normal operation, where V_{CEsat} is the minimum voltage required for the current sources operating in active mode.

An important limitation with the transconductor is its small linear input range caused by small common-mode input range. The larger device count and power dissipation is another factor which restricts its usefulness in low-voltage low-power applications. In the next subsection, a simple bipolar linear transconductor with high linearity over large input range is presented.

2. Operation principle of a low-voltage bipolar linear transconductor

Fig. 2 shows the proposed bipolar linear transconductor. The basic principle of the circuit is to make an input voltage appear only across the degeneration resistor without dc voltage level shift. To achieve this operation, two external *pnp* transistors, Q_3 and Q_4 are added into the *npn* emitter-coupled pair with degeneration, and biased by

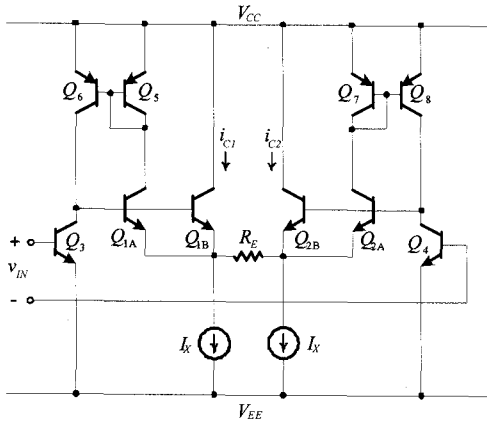


그림 2. 제안된 바이폴라 선형 transconductor
Fig. 2. Proposed bipolar linear transconductor.

the collector currents of Q_{1A} and Q_{2A} , respectively. To bias transistor Q_3 with the collector current of Q_{1A} , the collector current i_{C1} is reproduced at the emitter of Q_3 through a *pnp* current mirror formed by Q_5 and Q_6 . In the same manner, Q_4 is biased by the collector current i_{C2} which is reproduced at the emitter of Q_4 through a *pnp* current mirror formed by Q_7 and Q_8 . Assuming all the *npn* transistors and *pnp* transistors are identical, respectively, and summing the voltages around the loop consisting of the input voltage source, the four base-emitter junctions of $Q_1 \sim Q_4$, and the emitter degeneration resistor R_E , we obtain

$$\begin{aligned} v_{IN} = & -V_T \ln \left(\frac{\alpha_P k_P i_{C1}}{I_{SP}} \right) + V_T \ln \left(\frac{i_{C1}}{I_{SN}} \right) \\ & + \frac{R_E}{\alpha_N} (i_{C1} - i_{C2}) - V_T \ln \left(\frac{i_{C2}}{I_{SN}} \right) \quad (2) \\ & + V_T \ln \left(\frac{\alpha_P k_P i_{C2}}{I_{SP}} \right) \end{aligned}$$

where

V_T = thermal voltage

α_P = common-base current gain of the *pnp* transistors

$$k_P = \frac{\beta_P}{\beta_P + 2}$$

β_P = common-emitter current gain of the *pnp* transistors

I_{SP} = saturation current of the *pnp* transistors

I_{SN} = saturation current of the *npn* transistors

α_N = common-base current gain of the *npn* transistors

The sum of the terms including V_T is zero, and hence (2) reduces to

$$i_{C1} - i_{C2} = \frac{\alpha_N}{R_E} v_{IN} \quad (3)$$

Since the sum of i_{C1} and i_{C2} is $\alpha_N I_X$, i_{C1} and i_{C2} will be given by

$$i_{C1} = \frac{\alpha_N I_X}{2} + \frac{\alpha_N}{2R_E} v_{IN} \quad (4a)$$

$$i_{C2} = \frac{\alpha_N I_X}{2} - \frac{\alpha_N}{2R_E} v_{IN} \quad (4b)$$

The transconductance of the circuit is $G_m = \alpha_N / 2R_E$. The differential output currents i_{C1} , i_{C2} of the transconductor will drive the translinear current gain cell for implementing an OTA, which is described in Section 3.

The input range of the transconductor is limited by

$$|v_{IN}| \leq R_E I_X \quad (5)$$

or the input common-mode range. The common-mode range of the differential input terminals is limited by Q_6 leaving active mode of operation. Thus the voltages at both terminals should be smaller than $V_{CC} - V_{ECsat} - V_{EE}$, where V_{ECsat} is the minimum value of V_{EC} required for the *pnp* transistors operating in active mode. The common-mode range of this circuit is larger than that of the circuit shown in Fig. 1 by one $V_{BE} (\cong 0.6 \text{ V})$.

3. Low-voltage bipolar linear OTA

The low-voltage transconductor is used to design a low-voltage linear OTA. The resulting OTA is

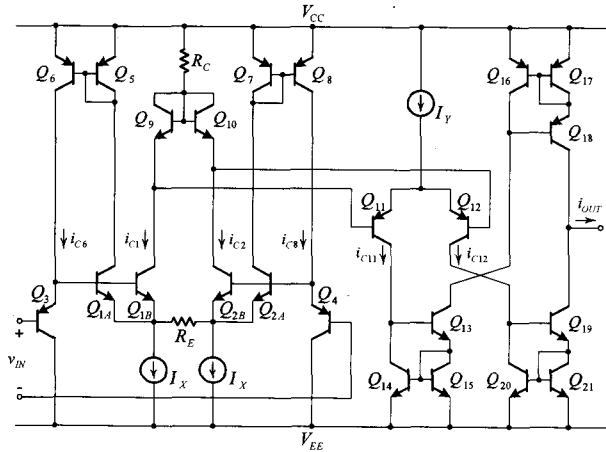


그림 3. 저전압 선형 바이폴라 OTA의 회로도
Fig. 3. Circuit diagram of a low-voltage linear bipolar OTA.

shown in Fig. 3. It consists of a low-voltage linear transconductor formed by transistors $Q_1 \sim Q_8$ and an emitter-degeneration resistor R_E , a translinear current gain cell $Q_9 \sim Q_{12}$, and three Wilson current mirrors $Q_{13} \sim Q_{21}$. The transconductor converts the differential input voltage v_{IN} into its corresponding differential output currents i_{C1} and i_{C2} whose expressions are given by (4a) and (4b), respectively.

The differential output currents i_{C1} , i_{C2} of the transconductor drive the diode-connected transistor pair Q_9 and Q_{10} of the translinear current gain cell formed by $Q_9 \sim Q_{12}$. The current gain cell makes the current partitioning of the transistor pair Q_9 and Q_{10} to be the mirror image of the current partitioning of the transistor pair Q_{11} and Q_{12} ^[5]. Therefore, we can write the following relation:

$$\frac{i_{C1}}{i_{C2}} = \frac{i_{C11}}{i_{C12}} \quad (6)$$

The output currents i_{C11} and i_{C12} of the current gain cell are differenced by three current mirrors formed by $Q_{13} \sim Q_{15}$, $Q_{16} \sim Q_{18}$, and $Q_{19} \sim Q_{21}$, respectively. Since the sum of i_{C11} and i_{C12} is I_Y and the difference is i_{OUT} , which denotes the single-ended output current of the OTA, currents i_{C11} and i_{C12} can be written as follows:

$$i_{C11} = \frac{I_Y}{2} + \frac{i_{OUT}}{2} \quad (7a)$$

$$i_{C12} = \frac{I_Y}{2} - \frac{i_{OUT}}{2} \quad (7b)$$

Combining (4a), (4b), (9), (7a), and (7b), one can obtain the transfer function of the OTA expressed as follows:

$$i_{OUT} = \frac{I_Y}{I_X} \frac{v_{IN}}{R_E} = G_m v_{IN} \quad (8)$$

The transconductance gain G_m is given by $(I_Y/I_X)(1/R_E)$. It is noticeable that in driving equation (8) no approximations have been made and there are no temperature-dependent terms. Also, note that the transconductance gain of the OTA is determined by the ratio of the dc bias currents I_Y and I_X .

III. Simulation results

The linear OTA shown in Fig. 3 was simulated using SPICE with an 8 GHz Tektronix SHPI bipolar transistor-array parameter^[6-7]. A product of R_E and I_X was chosen to make the input linear range 1 V: $R_E = 1\text{k}\Omega$ and $I_X = 1\text{mA}$. The value of the resistor R_C was chosen to be 200Ω for low voltage operation. The current sources I_X and I_Y were composed of a simple current-mirror and a resistor.

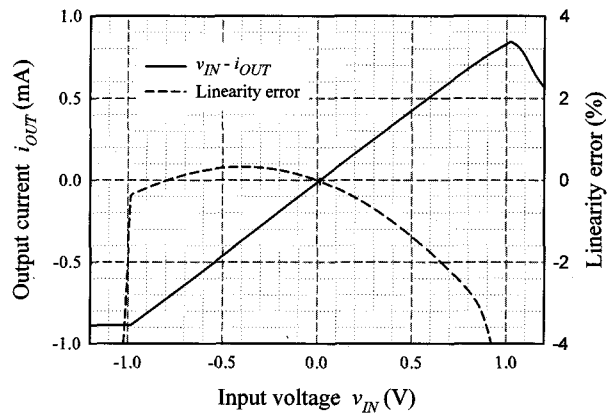


그림 4. OTA의 dc 전달 특성
Fig. 4. Dc transfer characteristic of the OTA.

All measurements were performed at supply voltages of ± 2.0 V.

The dc transfer characteristic of the simulated circuit for a fixed I_Y of 1 mA is plotted in Fig. 4 as the solid line. The linearity error relative to the ideal straight line of slope $G_m = 1$ mS is also plotted as the dashed line. The nonlinearity is seen to be less than 2% in the differential input voltage range from -1.0 V to +0.7 V. This nonlinearity is about two times lower than that of the conventional linear OTA in [4]. For comparison, the simulation result of the conventional linear OTA under the same operating conditions is shown in Fig. 5.

The dependency of the transconductance on temperature is shown in Fig. 6, which shows that the

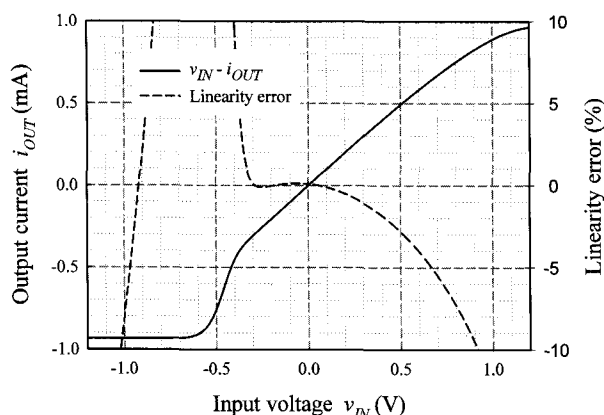


그림 5. 참고문헌 [5]에 제시된 기존 OTA의 dc 전달 특성

Fig. 5. Dc transfer characteristic of the conventional OTA in [5].

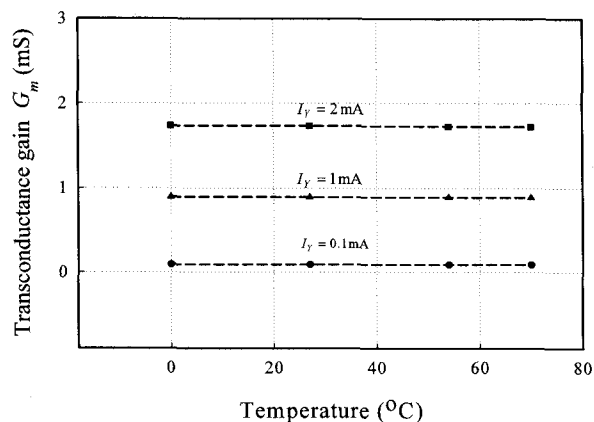


그림 6. OTA의 온도 특성

Fig. 6. Temperature characteristic of the OTA.

effect of temperature on the transconductance is almost negligible (less than -90 ppm/ $^{\circ}$ C).

The frequency response of the linear OTA is shown in Fig. 7, showing that the -3-dB frequency of the output current is more than 2.4 GHz for tuning bias current range of 0.1-1.2 mA. This frequency is

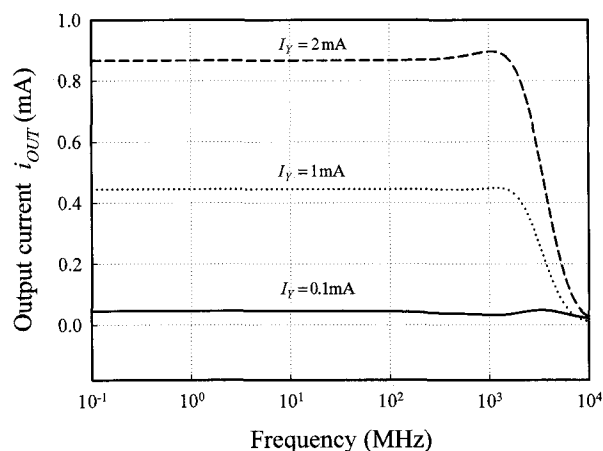


그림 7. OTA의 주파수 응답

Fig. 7. Frequency response of the OTA.

표 1. OTA의 성능 파라미터

Table 1. Performance parameters of the OTA's.

Parameter	Conditions	Proposed	Reported in [4]
Operating supply voltages		± 2 V	± 2 V
Input linear range	$\leq \pm 2$ %	± 0.7 V	± 0.35 V
TC of G_m	$0 \sim 70$ $^{\circ}$ C	$= 90$ ppm/ $^{\circ}$ C	$= 90$ ppm/ $^{\circ}$ C
Input resistance	1 MHz 80 MHz	110 k Ω 21 k Ω	1.3 M Ω 72 k Ω
Output resistance	1 MHz 80 MHz	470 k Ω 7 k Ω	450 k Ω 7k Ω
PSRR+ f_{3dB}		58 dB 627 kHz	66 dB 2.4 MHz
PSRR- f_{3dB}		85 dB 640 kHz	62 dB 480 kHz
-3dB bandwidth	$I_Y = 1$ mA	2.5 GHz	2.17 GHz
Power dissipation	$I_Y = 1$ mA	24 mW	28 mW

slightly higher than that of the conventional linear OTA (2.1 GHz). Other performance parameters of the proposed linear OTA are summarized in table 1, in which the simulation results of the conventional linear OTA in [4] are also presented for comparison.

IV. IF bandpass filter design

In order to test its applicability, the proposed OTA is used to implement a second-order bandpass filter for the first IF receiver stage for GSM (global system for mobiles) cellular telephone. Fig. 8 shows the circuit diagram of a second-order bandpass filter, in which two identical OTA's in conjunction with a grounded capacitor form a grounded inductor. The equivalent inductance of the inductor can be written as follows:

$$L_{eq} = CR_E^2 \left(\frac{I_X}{I_Y} \right)^2 \quad (9)$$

where R_E is the emitter degeneration resistance of the OTA. The transfer function of the bandpass filter is given by

$$T(s) = \frac{V_o(s)}{V_i(s)} = \frac{s \left(\frac{1}{C_1 R_1} \right)}{s^2 + s \left(\frac{1}{C_1 R_1} \right) + \left(\frac{I_Y^2}{C_1 C R_E^2 I_X^2} \right)} \quad (10)$$

The center frequency f_0 and the quality factor Q of the filter are given by

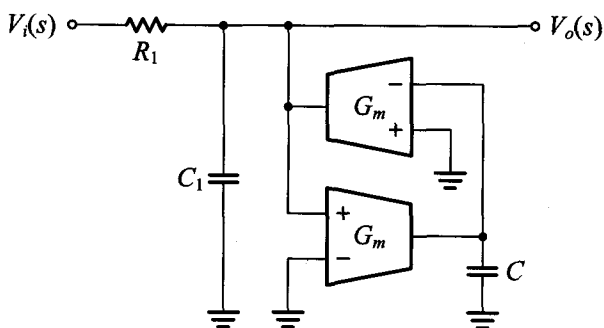


그림 8. 2차 bandpass filter의 회로도

Fig. 8. Circuit diagram of a second-order bandpass filter.

$$f_0 = \frac{I_Y}{2\pi \sqrt{C_1 C R_E I_X}} \quad (11)$$

$$Q = \sqrt{\frac{C_1}{C}} \frac{R_1 I_Y}{R_E I_X} \quad (12)$$

respectively. (11) shows that the center frequency can be tuned by adjusting the bias current I_Y , while (12) shows that Q -factor can be tuned by adjusting I_Y or R_1 .

The IF stage of a mobile communication requires a bandpass filter whose center frequency and Q -factor are 85 MHz and 75, respectively^[8]. The second-order bandpass filter shown in Fig. 8 can not provide this Q -factor. Therefore, to satisfy the required specifications of the filter, it is necessary to design the fourth-order bandpass filter which is cascaded with two identical second-order bandpass cells shown in Fig. 8.

Fig. 9 shows the transfer characteristics of the bandpass filters simulated with $R_1 = 10 \text{ k}\Omega$, $C_1 = 3 \text{ pF}$, $C = 3 \text{ pF}$, $R_E = 1 \text{ k}\Omega$, $I_X = 1 \text{ mA}$, and $I_Y = 2.1 \text{ mA}$. It can be seen that two filters have the same center frequency of 85 MHz, but Q -factors are different; the second order bandpass filter has Q -factor of 48 while the fourth-order one has 80. The effect of temperature on the center frequency of the fourth-order filters was also simulated. The result

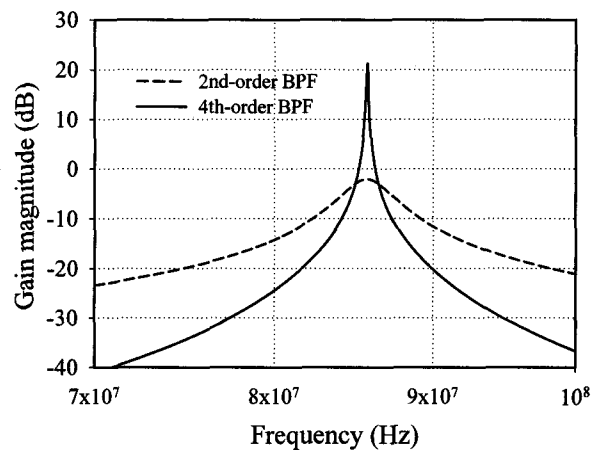


그림 9. IF bandpass filters의 전달 특성

Fig. 9. Transfer characteristics of the IF bandpass filters.

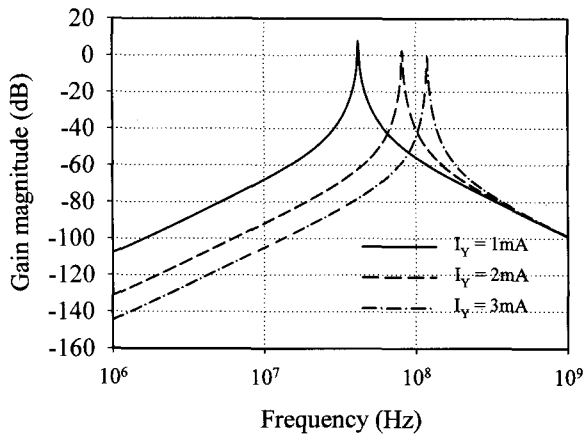


그림 10. 주파수 조정에 따른 4차 bandpass filter의 전달 특성

Fig. 10. Transfer characteristics of the fourth-order bandpass filter; frequency tuning.

was $-181.5 \text{ ppm}/^\circ\text{C}$, which is sufficiently low so that the filter can be used under temperature-varying environment conditions without temperature-compensation scheme. The power consumption of the fourth-order filter is 128 mW. The tuning of the center frequency f_0 with the bias current I_Y is shown in Fig. 10.

V. Conclusions

A low-voltage temperature-stable bipolar OTA with high-linearity has been described. It features simple configuration, large input linear range, and wide controllability of its transconductance gain. The OTA is used to design an IF bandpass filter for GSM cellular phone. SPICE simulations using the 8 GHz bipolar transistor-array parameter show that the OTA and the filter have fairly low sensitivities to temperature and power supply variations, which alleviate the demand on an automatic system for frequency tuning. One-chip implementations of the OTA and the filter are future works.

References

- [1] "Application Specific Analog Products", Databook (CA: National Semiconductor Corporation, Santa Clara, 1995).
- [2] Khan, I. A., and Ahmed, M. T., "Wide-range electronically tunable multifunction OTA-C filter for instrumentation applications", *IEEE Trans. Instrum. Meas.*, 36, 13-17, 1987.
- [3] Chung, W.-S., and Watanabe, K., "A temperature difference-to-frequency converter using resistance temperature detectors", *IEEE Trans. Instrum. Meas.*, 39, 676-677, 1990.
- [4] Chung, W.-S., Kim, K.-H., and Cha, H.-W., "A linear operational transconductance amplifier for instrumentation applications", *IEEE Trans. Instrum. Meas.*, 41, 441-443, 1992.
- [5] Gilbert, G., "A new wideband amplifier technique", *IEEE J. Solid-State Circuits*, 3, 353-365, 1968.
- [6] "QuickChip™ 6 Integrated Circuit Design Guide (Tektronix, Inc., Beaverton, Version 1)", 1989.
- [7] Wyszynski, A., Schaumann, R., Szczepanski, S., and Halen, P. V., "Design of 2.7GHz linear OTA and a 250-MHz elliptic filter in bipolar transistor-array technology", *IEEE Trans. Circuits & Systems II*, 40, 19-31, 1993.
- [8] Fabre, A., Saaid, O., and Boucheron, C., "Low power current-mode second-order bandpass IF filter", *IEEE Trans. Circuits & Systems II*, 44, 436-446, 1997.

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