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Overview of High Performance 3D-WLP

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Abstract Vertical interconnect technology called 3D stacking has been a major focus of the next generation of IC industries. 3D stacked devices in the vertical dimension give several important advantages over conventional two-dimensional scaling. The most eminent advantage is its performance improvement. Vertical device stacking enhances a performance such as inter-die bandwidth improvements, RC delay mitigation and geometrical routing and placement advantages. At present memory stacking options are of great interest to many industries and research institutes. However, these options are more focused on a form factor reduction rather than the high performance improvements. In order to improve a stacked device performance significantly vertical interconnect technology with wafer level stacking needs to be much more progressed with reduction in inter-wafer pitch and increases in the number of stacked layers. Even though 3D wafer level stacking technology offers many opportunities both in the short term and long term, the full performance benefits of 3D wafer level stacking require technological developments beyond simply the wafer stacking technology itself.

Key words Wafer Level packaging, 3D Packaging, Wafer Stacking.

1. Introduction

Vertical interconnect technologies called 3D stacking offer few major advantages including performance, cost, and form factors. First, it permits significant reductions of interconnect length distributions, which enables a significant increase in processor speed. A simple estimation of minimizing wire length has been done by MIT and with 2 stacked layers wire length will be reduced by~28% and with 5 stacked layers ~51%.[1] Second, it enables high density, low latency memory options, which provides a next generation transistor density with the current process generation. Third, it permits cost effective integration of very incompatible process flows can be processed independently and stacked at the wafer level prior to sort. Lastly, it has a great form factor, especially for mobile applications.

With the above advantages 3D stacking technologies becomes a major focus on IC and packaging interconnect technology. As shown in Fig. 1 3D stacking technologies have been real first in a packaging area as a part of SIP (system in packaging) and it will continuously be a technological trend for IC industries. There are many approaches of 3D stacking technologies and it is summarized in Fig. 2. First it is distinguished into a chip level and a wafer level. A chip level is considered as package solutions and in general these solutions have low performance, but higher yield. Currently it has 95% of market because of a cost advantage at present and mature technologies compared to wafer level solutions. Wafer level solutions however have much higher performance and for the future IC generations wafer level solutions will be the most attractive and perhaps only solutions. Among wafer level solutions

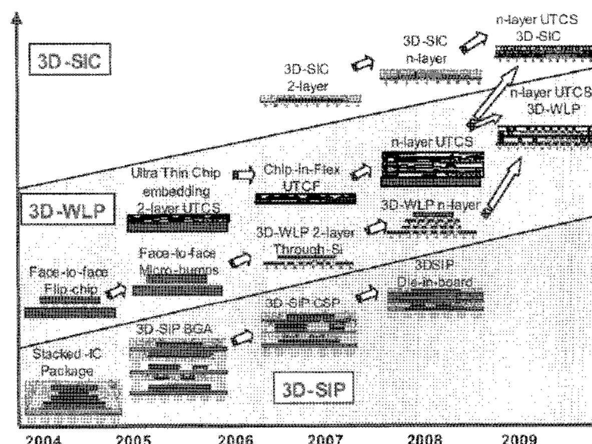

Fig. 1. IMEC's 3D Packaging and Interconnect Roadmap.[2]

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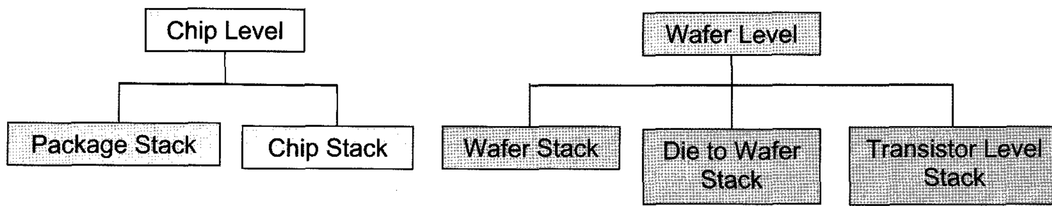

Fig. 2. 3D Technology Approaches.[3]

die-to-wafer stacks are more attractive at a moment because of higher yield with relatively medium cost and medium performance. But a wafer stacking will become the key technology in the future, especially for the high performance devices. 3D wafer level packaging will provides higher interconnect hierarchy to enable high density-high performance systems prior to 3D IC.

2. 3D Wafer Level Technologies

There are three wafer level based technologies such as dielectric (adhesives or SOI) bonding, metallic bonding and re-crystallization. All these approaches will be very low cost and high performance compared to package solutions or die solutions. Among these technologies, re-crystallization has the highest potential bandwidth, but the worst process capability and limitations in integrating divergent flows. Dielectric bonding has the lowest potential bandwidth and requires a high aspect ratio through Si via to facilitate every connection. The detailed process flows, advantages and disadvantages are explained in elsewhere.[4-14] Metallic bonding, however, is more attractive in terms of high bandwidth and divergent process capabilities. To obtain the full benefits of 3D high performance applications like logic IC stacking system has to be evaluated with few micrometers of fine pitched metallic bonding processes.

Fig. 3 schematically explains the interconnect benefits of 3D stacking. Among many stacking structures, stacking multiple parts of a device to make one device such as one CPU unit or one memory unit will offer the best performance improvement. Fig. 4 is the electrical simulation by Intel comparing conventional, RF, optical, and 3D stacking system. It indicates that in order to improve a device performance significantly a local level of interconnects has to be improved. To achieve

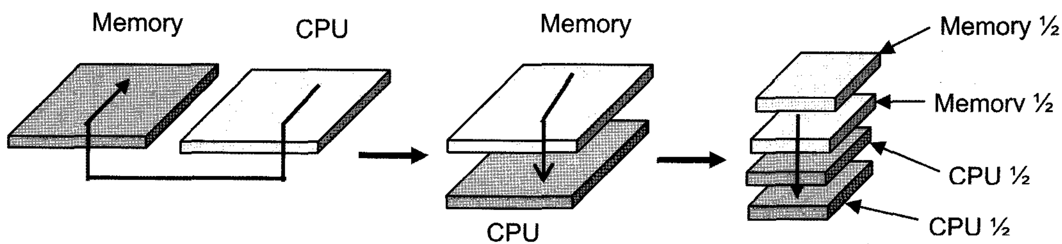

Fig. 3. Performance Improvement in Stacking Options.

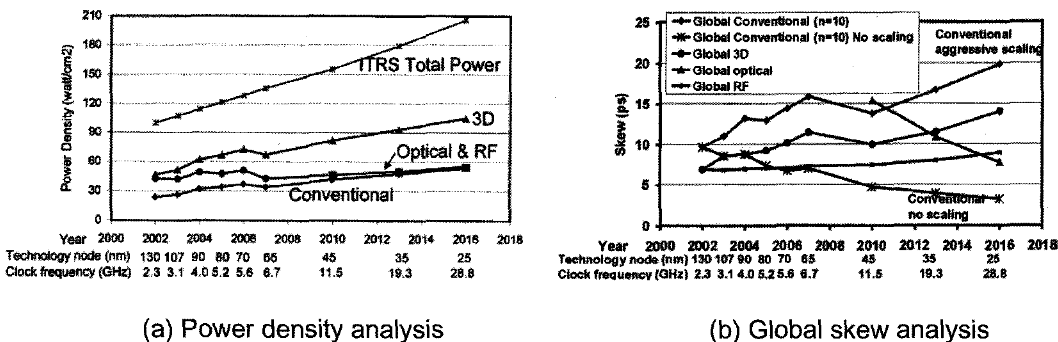

Fig. 4. Comparison between conventional, 3D, Optical, and RF Interconnect: (a) power density and (b) global skew.[3]

this high performance by 3D stacking very fine pitched metallic bonding and ultra-thinning process developments are required.

In 2004 Intel presented 300mm wafer-to-wafer Cu bonding process.[4] This result has demonstrated the possibility of a fine pitched metallic bonding process and improved 300 mm tool capability, but for high performance applications further studies on processing, system design and their reliability have to be greatly investigated. In addition to a fine pitched metallic bonding process ultra-thinning wafer process for less than 50 micrometers becomes one of key processes of wafer stacking system. Other processes such as thru-via drilling and filling processes have been developed and shown widely. Although wafer stacking processes have been improved significantly for the last few years, all these technologies have still faced issues with both power delivery and heat extraction which need careful consideration, especially for high power and high performance applications.

3. Current Status of 3D Technologies

During the last few years, 3D technologies have been explored with many publications and even commercial products. At a moment, a majority of commercial interests is related to die-to-die (or wafer) memory options for higher density and smaller die size in volume and weight.

Matrix first shipped one-time-programmable memories with eight layers in 2003 and now is shipping in volume. Inline has demonstrated die-on-die stacking, using diffusion soldering in 2002 and prototype security chip-card was demonstrated in 2004. Vertical Circuit has a custom service on die-on-die stacking commercial memory. SamSung announced chip-on-chip and chip-on-wafer stacking (prototype) for high-density memory, 8-chip stack in 2005 and 16-chip stack in 2006. Elpida memory in Japan announced recently in 2007 20-chip

Table 1. 3D Technology Status [15].

Company	Research Area	Process	Presentation
Infineon	Die stacking: demonstrated in 2002; prototype security chip-card demonstrated Nov 2004. 2-level die-on-wafer memory stacking	Die stacking w/ soldering or micro-bump bonds, Deep vias	TechVenture 2004: MRS 2006
IMEC	Various 3D approaches	Die stacking & thinning, Chip-in-polymer stacking & through-vias	ISSCC 2004: TechVenture 2005 & 2006 : IITC 2006
Cornell	3D wafer-level low-temp circuit layering 3D electronic integration, crosstalk & heat issues, etc	SOI wafer process	VMIC 2004 & 2005.
IBM	Wafer stacking process Design tools, methodology In 2002, deposited the active layer of one wafer on another w/o interconnects	Wafer stacking using SOI wafers, fusion bonding, and a "glass handle" to transfer layers	TechVenture 2004 & 2005 : MRS 2006
MIT	3D IC layout issues Sensor design in 2001 4-wafer stacks in 2005	Wafer stacking, high-density interconnect, Cu bonding, oxide fusion bonding	TechVenture 2004 & 2005 : IAB 2004: VMIC & MRS 2006
RPI	Wafer Stacking Interconnect process announced in 20	Wafer stacking, bonding, thinning or SOI; dielectric adhesive for low-temp bonding	TechVenture 2004, 2005, & 2006 : VMIC 2004, 2005, & 2006: MRS 2006
Samsung	Announced 16-chip stack (prototype) in 2006	Chip-on-chip & chip-on-wafer stacking	TechVenture 2005 & 2006
SEMATECH (R&D Consortium)	Identified 3D interconnect research as a "top technical challenge" in ITRS for 2005. Organized symposium "3D Chips" in 2004 and "3D Infrastructure Roadmap Workshop" in 2005		TechVenture 2005 : VMIC 2006
Tohoku University	Developed a 3D artificial retina, various 3-layer chips (w/ Mitsubishi, MIT, ZyCube).	Wafer stacking with adhesive and micro-bump bonds;	VMIC 2004 : TechVenture 2005
Elpida memory	Announced 20-chip stack MCM in 2007		

stack MCM technology. There are many other companies and suppliers who are providing a custom based service on die stacking processes.

For more cost effective and high density, high performance options, wafer-to-wafer stacking is more of interest. Recently, ZyCube has announced commercial lunch on wafer-on-wafer stacking with Tohoku University process using insulating adhesives and "micro-bump" connectors. In 2002 IBM showed that the active layer of one wafer was deposited on another, creating the equivalent of a two-wafer stack without interconnects. They are also investigating on 3D design tools, methodology, process and infrastructure. MIT is studying on both processes and 3D IC layout issues and four-wafer stacks were announced in 2005. Intel has presented successful electrical measurements of stacked ring oscillators and stacked SRAM devices with 300 mm Cu wafer-to-wafer bonding process in 2004.

Only several industries and universities have been named in this paper summarized in Table 1. To name several more, they are Albany NanoTech, Cornell, DARPA, EV Group, GE, Georgia Tech, Irvine Sensors, Lincoln Labs, MARCO, SRC, Stanford, Sun Microsystems, Suss MicroTech, Toshiba, Ziptronix, and Xan3D.

4. Technology Limitations and Challenges

3D wafer level stacking technologies have five major limitations including thermal heat extraction, power delivery, manufacturing yield, process challenges, and architectural revolutions including design tools and methodology. Although the impact of a die area reduction by 3D stacking will depend upon the particular application, for high power density 3D logic applications thermal heat extraction can be a potential performance limiter. It has been demonstrated that a simple SRAM/logic stack has a minimal increase of maximum power density, but uniform power distribution. But, this may not be possible for multiple logic stacks causing the architectural constraints. Also, if bump pitch does not scale, the total number of bumps will be decreased in half and there will be a power delivery problem due to a decrease in power bumps since the I/O bump count must remain constant.

The manufacturing yield issues are still argumentative, but are best illuminated by many researchers. Last few years, many process challenges are either resolved or showed great potential demonstrating with process repeatability and electrical measurements. With the recent process improvements and manufacturing yield potentials, architectural layouts and design tools has become the major technological limiter. Complete changes to floor plan layout, optimization strategies, layout methodologies and software development are required to fully leverage the advantages of 3D wafer stacking technologies.

5. Conclusions

3D wafer level stacking offers the most promising solution for the high performance device system and it also provides relatively low cost, flexible integration solutions for diverse process flows and volume and weight reductions. Many specific 3D technologies are being developed in many research institutes for generic 3D core processes. Nevertheless for large potential gains in performance, new stacking processes such as fine pitched metallic bonding and ultra thinning process need to be evaluated further. In addition 3D wafer level stacking technology may need to focus on and evaluate potential increased power densities, high volume manufacturing yield, thermal and reliability issues.

Current 3D technology is still at the R&D stage. As the first step, many 3D applications such as low power, handheld and hybrid applications may take great advantage of 3D technology. However, for the next step high performance device will be in great demand and 3D WLP will offer a promising process option prior to 3D IC for continued extensions of Moore's law and has great opportunities for the future generation of electronic areas.

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