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회로면적에 효율적인 3 GHz CMOS LNA설계

(Size-Efficient 3 ㎓ CMOS LNA)

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요 약

본 논문에서는 vertical shunt symmetric inductor를 이용하여 CMOS LNA의 설계에 있어서 회로의 면적을 줄이는 설계기술 및 구현에 관한 내용을 제시하고자 한다. 본 연구에 있어서 vertical shunt symmetric inductor는 LNA의 입력단과 출력단을 3GHz로 정합하기 위해서 사용되었다. 이렇게 구현된 보다 면적에 있어서 효율적인 증폭기를 0.18um digital logic공정으로 구현되었다. 본 논문에서는 일반적으로 LNA에서 사용하고 있는 inductor를 이용하는 경우와, vertical shunt symmetric inductor를 이용하여 LNA를 설계하는 경우에 대한 부분을 비교하였고, 최종적으로 면적에 효율적인 회로설계 기술을 제시하고자 한다.

Abstract

This paper presents the implementation technique to reduce circuit area occupation in designing Low Noise Amplifier (LNA) using vertical shunt symmetric inductor. We applied a vertical shunt symmetric inductor to match the input and output in 3 ㎓ CMOS LNA to reduce the circuit area. This size efficient amplifier has been designed in a 0.18 ㎛ digital logic CMOS process. In this paper, the case of conventional asymmetric inductor, and vertical shunt symmetrical inductor with a relatively higher number of turns have been compared in order to present a size efficient CMOS LNA design method while still retaining the circuit operation characteristics.

Keywords: CMOS, Low Noise Amplifier (LNA), vertical shunt inductor, thin metal CMOS process

I. 서 론

Recent continuous scale-down of CMOS technology is driving force to realize low cost single-chip RF-ICs[1~4]. Among them, one of the most critical operational blocks in the wireless receivers is the low noise amplifier (LNA). Lots of researches on CMOS LNA design in submicron technologies have been done in recent years: from the investigation[5] and the design guidelines[6~7], up to various new ideas on design improvement of low noise figure[8], high power gain, low power consumption[9~10], and high linearity[11~12]. Despite these endeavors, many challenges in design and optimization of low cost and small sized CMOS LNAs are still the key design goal for RF-ICs. From this point of view, the using of the vertical shunt symmetric inductor in thin metal CMOS process, which is cost-competitive compared to conventional RF CMOS process, is one of solutions to reduce the circuit area and implementation cost at the same time respectably.

In this paper, using symmetric vertical shunt inductor for LNA design in thin metal CMOS process is proposed to minimize area occupation and cost. A 3 ㎓ CMOS LNA was designed in a 0.18 ㎛ (1-poly and 6-metal) digital logic process.

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II. SIZE-EFFICIENT LOW NOISE AMPLIFIER DESIGN

1. Vertical Shunt Symmetric Inductor

If one uses the thin metal digital logic process for low cost CMOS LNA implementation, one should consider carefully the high signal-line resistance which causes the Q-factor degradation of inductor. Therefore, the one of reduction methods of series resistance as well as size of inductor simultaneously is used for vertical shunt inductor[13].

From this point of view, vertical shunt inductor was implemented by the neighboring metal layers (top metal, M6 = 0.84 ㎛ and M5=0.53 ㎛) that are shunted through via arrays, so the effective thickness of the spiral inductor was increased up to 2.17 ㎛, and the series resistance was reduced effectively. To enhance performance, the patterned-ground shield (PGS) was used for all the inductor test pattern[14~15]. Small-signal performance of the test devices was characterized by on-wafer 2-port S-parameter measurement. Fig. 1 and 2 show the measured series resistance, inductance and quality factor of vertical inductor with symmetrical type and conventional inductor with asymmetrical type for 3 ㎓ LNA design. The 4.9 nH inductor L_g and L_{out} in Fig. 4 (a) are used for input and output matching at the resonance frequency, respectively. The equivalent series resistance R_s and Q-factor were extracted from Y_{11} and Y_{21} as follows: $R_s = Re(-1/Y_{21})$ and the quality factor was evaluated by Q-factor= $Im(Y_{11})/Re(Y_{11})$.

The measured inductance, R_s and Q-factor at 3 ㎓ for 5 turns, 286 ㎛ out-diameter symmetric vertical inductor were about 13 Ω, 4.5 and 4.9 nH respectively. Also, above parameters for 3.5 turn 390 ㎛ outer diameter conventional device were about 14.3 Ω, 4.4 and 4.9 nH respectively.

We can find the Q-factor and R_s of symmetric vertical shunt inductor were a little improved while inductance was almost same value between two devices. From these measurement results, we confirm 46.3 % size reduction by vertical shunt inductor compared to conventional case while showing no degradation in terms of device performance. The

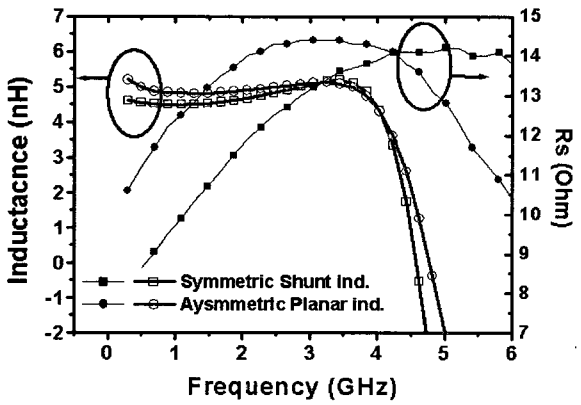


그림 1. vertical shunt symmetric 와 conventional inductor 의 inductance와 series resistance 측정결과

Fig. 1. The measurement results of the vertical shunt symmetric and conventional inductor in terms of inductance and series resistance.

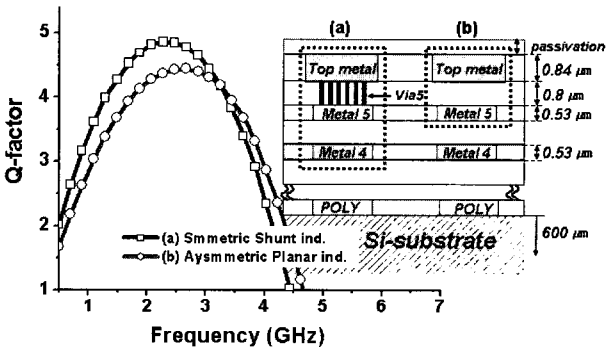


그림 2. vertical shunt symmetric 와 conventional inductor 의 Q-factor 측정값

Fig. 2. Measured Q-factor of vertical shunt symmetric and conventional inductor.

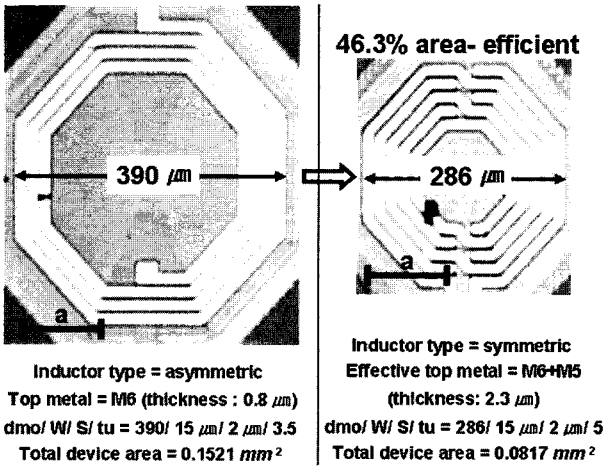


그림 3. 제작된 test device의 칩사진

Fig. 3. Die microphotographs of the test device.

microphotograph of a monolithic inductor fabricated using thin metal process is shown in Fig. 3.

2. Low Noise Amplifier Design

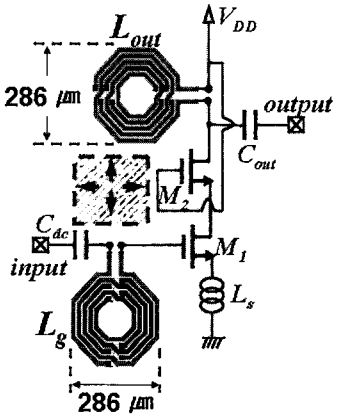
A single-ended conventional cascode LNA topology is shown in Fig. 4 (a). For simultaneous matching of power and noise, inductive source degeneration inductor (L_s) is widely used. As to the input match, from the input circuit in Fig. 4 (a), we can calculate the input impedance as

$$Z_{in} = R_l + R_g + \left(\frac{g_m}{sC_{gs}}\right)L_s + s(L_s + L_g) + \frac{1}{sC_{gs}} \quad (1)$$
$$= R_l + R_g + \omega_t L_s \ (at\ resonance)$$

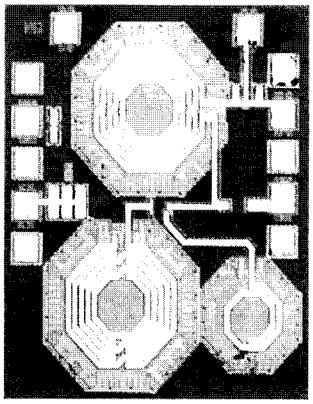
where R_l is the series resistance of the L_g, and R_g is the gate parasitic resistance of the NMOS transistor M1. The output impedance matching can be obtained by tuning the inductor L_{out} and the capacitor C_{out} to provide parallel resonance and increase the gain at the design frequency. In order to match the input and output of the CMOS LNA, both L_g and L_{out} are required, which up to now have commonly been implemented by a conventional asymmetric inductor. An alternative to these two inductors (L_g and L_{out}) are crucial in reducing the size of the LNA circuit because they are large enough to take up most of the area in an LNA circuit.

In this design, from the measurement data of the symmetric inductor - above showing a substantially smaller size than the asymmetric counterpart - was used to design a CMOS LNA.

Fig. 4.(b) shows the microphotograph of fabricated



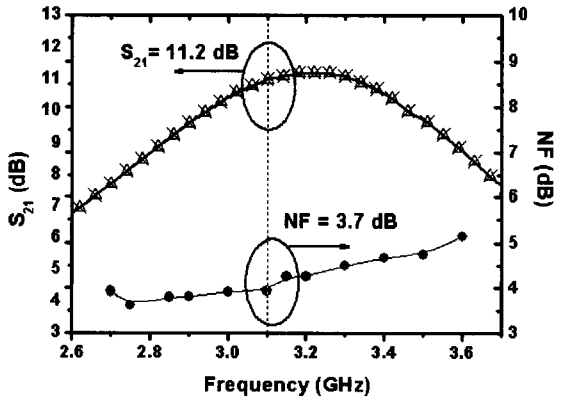
(a)



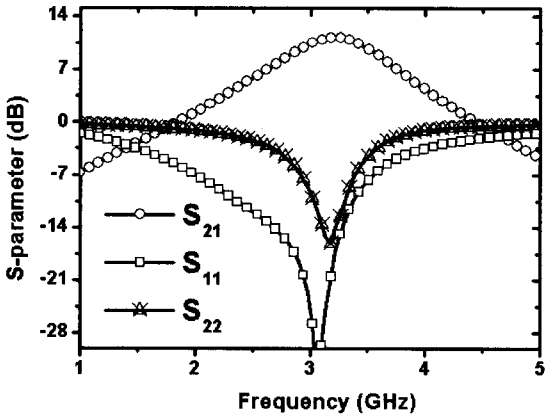
(b)

그림 4 (a) 간단히 제시된 LNA구조도
(b) 제작된 LNA의 칩사진

Fig. 4. (a) Simplified schematic of the LNA.
(b) microphotograph of fabricated LNA.



(a)



(b)

그림 5. 제안한 LNA의 S-parameter 결과들 (a), (b)

Fig. 5. Measurement results of proposed LNA (a), (b).

표 1. 제안한 LNA 성능 요약표
Table 1. Proposed LNA performance summary.

Parameter	Proposed LNA	Unit
Center frequency	3	GHz
Gain	11.2	dB
Noise figure	3.7	dB
S_{11} & S_{22}	< -10	dB
power	6.88	㎽
Size	780 x 900	㎛^{2}

CMOS LNA. The proposed fully integrated LNA with vertical shunt symmetric inductor occupies only 780 ㎛ x 900 ㎛ active silicon area. However, the conventional LNA will occupy 1290 ㎛ x 960 ㎛ active silicon area from the estimation of circuit layout. It was verified that the LNA using the s0 % size reduction compared to the one utilizing the asymmetric inductor. Fig. 5 (a) and (b) shows the measurement results of gain, return loss (S_{11}, S_{22}) and noise figure of amplifiers using symmetric shunt inductor. The proposed LNA has a gain of 11.2 dB, noise figure of 3.7 dB and good input and output matching in the frequency of interest. The transistor M1 with the channel width of 360 ㎛ was selected for low NF_{min} and the current flow in the LNA at V_{DD} of 1.6 V was 4.3 ㎃[16]. Table I summarizes the measurement results of the proposed LNA.

III. Conclusion

We proposed a size-efficient 3 ㎓ low-noise amplifier using two-metal vertical shunt symmetric inductor in 0.18 ㎛ thin metal CMOS technology. It achieved 11.2 dB gain, 3.7 dB noise figure, and 6.88 ㎽ power dissipation. The size of the proposed LNA was reduced by 44 % compared to those using the conventional asymmetric inductor. The proposed scheme has application to not only small sized LNA but also small sized high linearity mixer and VCO design.

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