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# Low Cost Driving System for Plasma Display Panels by Eliminating Path Switches and Merging Power Switches

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## ABSTRACT

Recently, plasma display panels (PDP) have become the most promising candidate in the market for large screen size flat panel displays. PDPs have many merits such as a fast display response time and wide viewing angle. However, there are still concerns about high cost because they require complex driving circuits composed of high power switching devices to generate various voltage waveforms for three operational modes of reset, scan, and sustain. Conventional PDP driving circuits use path switches for voltage separation and a scan switch to offer a scan voltage for reset and scan operations, respectively. In addition, there exist reset switches to initialize PDPs by regulating the wall charge conditions with ramp shaped pulses, which means the necessity of specific power devices for the reset operation. Because power for the plasma discharge accompanied by a large current is transferred to a panel via path switches, high power rating switches are used for path switches. Therefore, this paper proposes a novel low-cost PDP driving scheme achieved by not only eliminating path switches but also merging the function of reset switches into other switches used for sustain or scan operations. The simulated voltage waveforms of the proposed topology and experimental results implemented in a 42-inch panel to demonstrate the validity of using a new gate driver that merges the functions of power switches are presented.

**Keywords:** plasma display panel(PDP), power switch, reset and scan operations, gate driver

## 1. Introduction

With the rapidly increasing demand for flat panel displays (FPDs) with large screen size and high resolution, devices such as plasma display panels (PDPs) and LCDs have been widely researched and commercialized. Currently, the competition among FPDs has become so severe that their manufacturers are struggling to cut down the set price to maintain competitiveness in the FPD market. PDPs have advantages of a fast display response time and wide viewing angle [1-2]. However, PDPs have high costs due to complex driving circuits using high power devices. Therefore, there is high demand for developing a low cost driving circuit for PDPs.

Fig. 1 shows the structure of an AC PDP having three electrodes of X, Y, and A (Address) in which the PDP is modeled as a capacitor $C_p$ and a current source representing panel discharge currents. The $C_p$ represents the inherent capacitance due to the structure of the dielectric layer covered on the top of the sustain electrodes (X and Y). The Mgo is coated on the dielectric layer to

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protect the dielectric layer and to release secondary electrons that aid a plasma discharge. A PDP consists of many RGB cells corresponding to the horizontal and vertical resolution such as 1024 x 768. Red, green, and blue (RGB) phosphors are filled in each cell. The address electrodes are located under the RGB cells perpendicular to the X and Y electrodes. Cells in a PDP emit visible lights by the plasma discharge induced by a square-wise alternating electric field applied between X and Y electrodes. The plasma discharge ionizes the gas inside the cell, and then the excited gas generates ultraviolet lights that make the phosphors create red, green, and blue visible light. For charging or discharging $C_p$ and supporting the plasma discharge, a large amount of displacement and discharge currents are demanded. Hence, it is needed to use switches that can cope with high peak and RMS currents, which means a high cost driving system.

Much research has been carried out to improve performance of sustain circuits and to reduce their cost [3-6], but this work has only focused on the sustainer that has a voltage and switching frequency of typically 200 *V* and 200 *kHz,* respectively. Even though the sustain circuit is the main part of the driving system, the driving system needs other circuits to generate specific voltage waveforms for a gas discharge such as reset and scan. Therefore, this paper proposes new low-cost PDP driving schemes that replace so-called path switches with power diodes and eliminate power switches for the reset operation by merging the reset function into other switches such as sustain or scan switches.

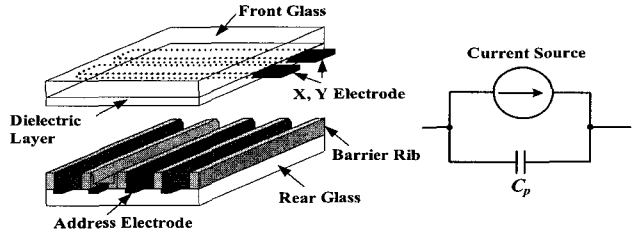



Fig. 1 The structure of three-electrode AC PDP and its equivalent circuit

## 2. Conventional Driving Method

### 2.1 Driving System

Fig. 2 shows voltage waveforms of X, Y, and A electrodes corresponding to the voltage waveforms for the address display period separation (ADS) driving scheme that is a commonly used driving method in commercialized plasma TVs. The operational periods of PDPs in 1 TV subfield can be divided into reset, scan (or address), and sustain period. The ramp reset is widely adopted, which initializes cells to have the same wall charge conditions by a weak gas regardless of the previous on/off state of cells. In the address period, scanning pulses are sequentially applied to the Y electrode, and data pulses are given to the cells to be addressed. During the sustaining (or display) period, the addressed cells emit light by sustain pulses imposed between X and Y electrodes in an alternating manner.

Fig. 3 shows the whole schematic diagram of a conventional driving system consisting of X, Y, scan, and address boards. Address boards are not being shown for simplification. The X board shown inside the square consists of sustain and bias circuits. The bias circuit applies the voltage level of $V_{bias}$ to the X electrode for controlling wall charge conditions during the reset and scan periods. Usually, sustain circuits have a half bridge structure with energy recovery circuits (ERC) of the Weber type. The Weber type ERC, which is based on *LC* series resonance between an inductor and the panel capacitor, is typically used for the ERC in most commercialized PDP TVs. Under ideal conditions, the resonance between the inductors and the $C_p$ raises and decreases the panel voltage from zero to $V_s$ level in a half resonant period, and vice versa. The series resonance is terminated after a half resonant period because reverse resonant currents are blocked by the diode $D_r$ and $D_f$ during sustain rising and falling, respectively.

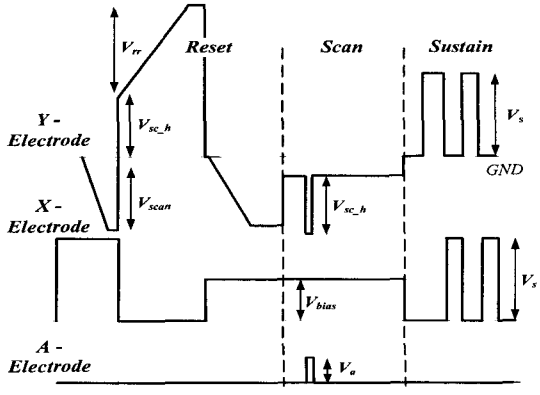



Fig. 2 Voltage waveforms of Y, X, and A electrodes for the ADS driving scheme

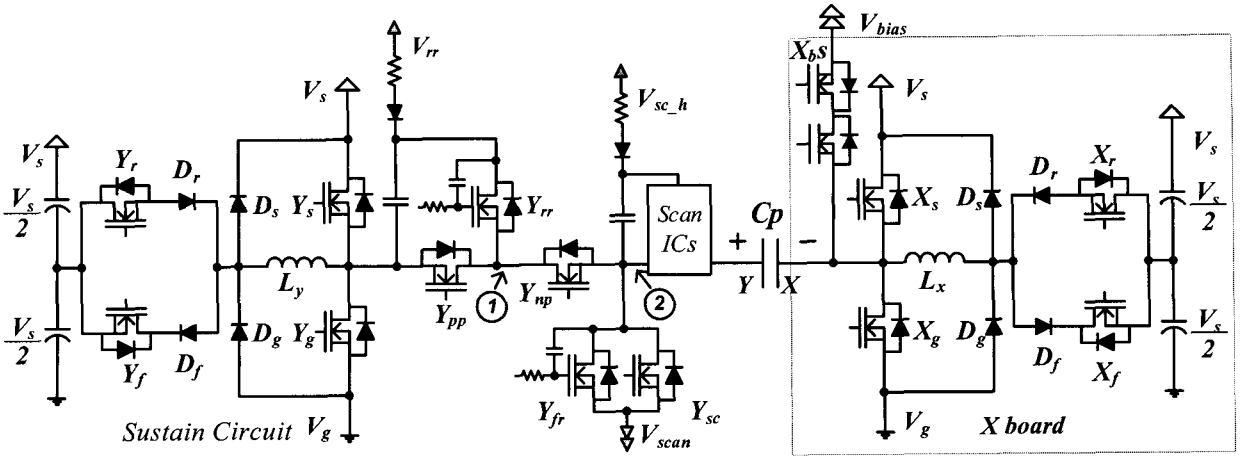



Fig. 3 Overall diagram of conventional PDP driving system

### 2.2 Problems of the Conventional Driving System

In the conventional scheme illustrated in Fig. 3, there exist $Y_{np}$ (negative-path) and $Y_{pp}$ (positive-path) commonly called path switches, which are used for voltage separation during reset and scan periods. Some commercialized PDP TVs employ only one path switch, which is usually $Y_{np}$. By changing the reset voltage levels of the X and Y electrodes, it is possible to use only $Y_{np}$ for voltage separation. $Y_{np}$ isolates the circuits connected in the point 1 from that of point 2 during the ramp-down and scan periods. Unless $Y_{np}$ is turned off during the period when the $V_y$ goes below zero potential such as ramp down and scan periods, unexpected currents can flow through the diode inside $Y_g$ to the $Y_{fr}$ (ramp falling) or to the $Y_{sc}$ (scan), respectively.

Among three operational periods of PDPs, most powers are consumed in the sustaining period because of large displacement and discharge currents for generating and supporting the plasma discharge, respectively. The sustain switches as well as path switches are involved in transferring the power for plasma discharge during sustain period. Fig. 3 shows that displacement current flows via the path of $V_s/2 \rightarrow Y_r \rightarrow D_r \rightarrow L_y \rightarrow (Y_{pp} \rightarrow)$ $\boldsymbol{Y_{np}} \rightarrow C_p \rightarrow$ *X board* and that of the discharge current is $V_s \rightarrow Y_s \rightarrow (Y_{pp} \rightarrow)$ $\boldsymbol{Y_{np}} \rightarrow C_p \rightarrow$ *X board.* Since displacement and discharge currents are always flowing through the path switches, several switches are connected in parallel for path switches to cope with the large current and power dissipation occurring in the switches.

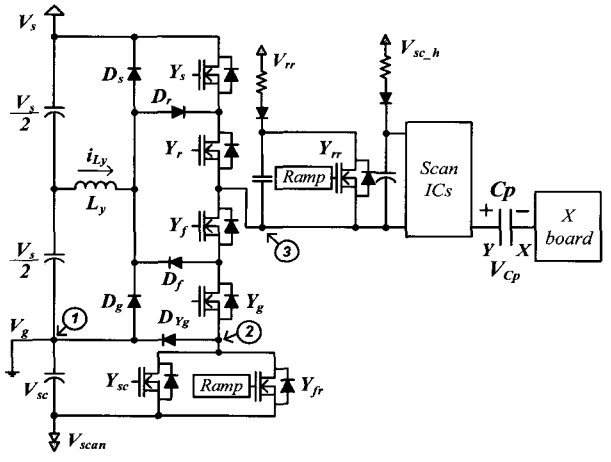
Besides path switches, conventional systems have the reset switches, $Y_{rr}$(ramp-rising) and $Y_{fr}$ (falling-ramp), to initialize PDPs with the ramp shaped pulses. The reset switches operates in an active region by using the external high resistor and external capacitor connected in the switches, which make reset switches turn on with slow switching transition. In summary, the conventional system needs specific power devices for generating reset voltage waveforms and path switches for voltage isolation.

Therefore, it is apparent that eliminating path switches and reset switches can considerably lower the price of PDP driving systems.

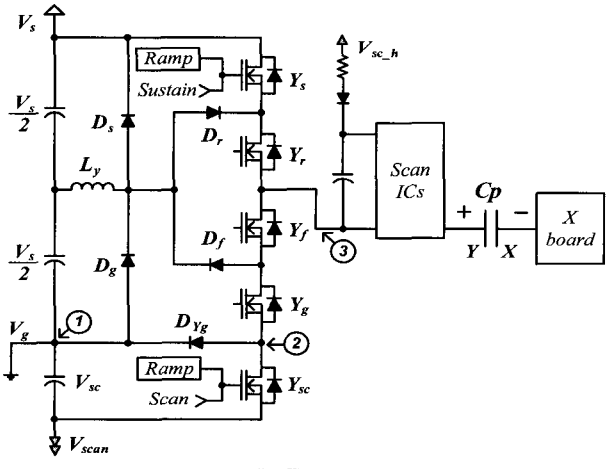
## 3. Proposed System

Topology removing both $Y_{np}$ and $Y_{pp}$ has been reported [7] and it has devices replacing positive-path switches. On the other hand, this research focuses on the $Y_{pp}$–less scheme that aims more at cost reduction by removing $Y_{pp}$ and modifies the reset voltage waveforms to improve the addressing ability for PDPs. Fig. 4 shows the proposed driving systems that do not have path switches, which are based on the $Y_{pp}$–less scheme. In the proposed system, the diode $D_{Yg}$ replaces the $Y_{np}$ that isolates the voltage of point 2 from that of point 1 to inhibit the short current from ground potential $V_g$ to the negative voltage $V_{scan}$ during ramp-down and scan period, respectively. The configuration of the X board of the proposed system is the

same as that shown in Fig. 1. Furthermore, switches are connected in series to withstand voltages across them together, which makes it possible to use lower V-rating ones. The switches involved in reset and scan operations have to withstand the maximum voltage differences of the highest and lowest ones in the system, which is normally over 400 V for commercialized plasma TVs. Therefore, devices over 500 V are usually used for the switches in consideration of voltage safety margins. On the other hand, it can be shown from Fig. 4 of the proposed scheme that the maximum voltages across the switches of $Y_r$, $Y_f$, $Y_s$ and $Y_g$ are $V_s$ level. Consequently, it is clear that the proposed scheme has advantages of using fewer power devices with a lower voltage rating.



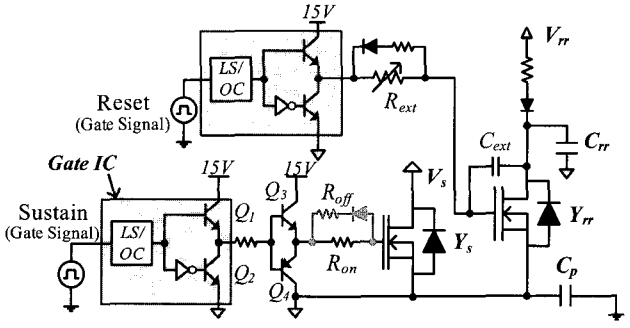

(a) Type I



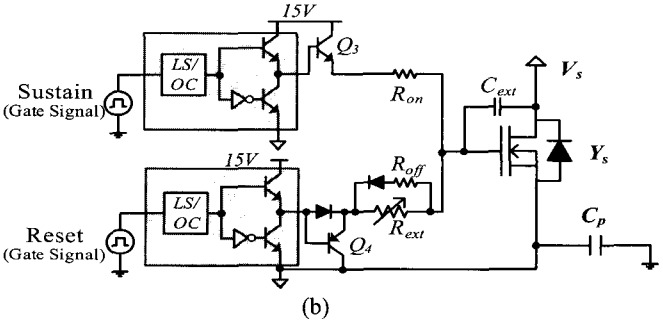

(b) Type II

Fig. 4 Proposed low-cost systems (a) using $Y_{rr}$ and $Y_{fr}$ and (b) without using $Y_{rr}$ and $Y_{fr}$

The scheme shown in Fig. 4(a) uses reset switches, $Y_{rr}$ and $Y_{fr}$, for generating ramp pulses. For greater cost reduction, the scheme of Fig. 4(b) merges the function of reset switches into sustain and scan switches by the help of a new gate driver. Fig. 5(a) shows conventional gate drivers for $Y_s$ and $Y_{rr}$ switches in which LS/OC represents a level shifter or an opto-coupler to provide an electrical isolation between the gate signal from a control board and power side having high voltage. In order to do switching $Y_s$ (sustain switch) with a relatively high switching speed over 200 *kHz* during the sustain period, the gate on/off currents for $Y_s$ are supplied by $Q_3$ and $Q_4$ consisting of the push-pull current amplifier. Since the ramp-rising switch $Y_{rr}$ does work only during the reset period and requires small gate current to operate $Y_{rr}$ in an active region, the gate signal from the gate IC is delivered to $Y_{rr}$ without the current amplification. Fig. 5(b) shows the novel gate driver that can merge the function of reset switches into other switches. In this case, $Y_s$ generates both sustain and ramp-rising pulses. It consists of two parts; a gate for sustain operation with a low gate resistor and that for reset operation with a high external resistor.




(a)




(b)

Fig. 5 Gate driver for sustain and scan in (a) conventional schemes and (b) a novel gate driver working for both reset and sustain operations

Table 1 summarizes four possible modes corresponding to on/off signals from each gate IC. In reality, there are three modes because the sustain off and reset off have the same role of turning of $Y_s$ with the fast off process. The slow turn-on process of $Y_s$ for ramp reset is done with the external resistor $R_{ext}$ having high resistance. While high on/off currents for fast switching during the sustain period are supplied via the $R_{on}$ and $R_{off}$ having low resistance.

Table 1 Gate signals for four possible modes

| | RESET Signal | SUSTAIN Signal |
|---|---|---|
| Reset ON | ON | OFF |
| Reset OFF | OFF | OFF |
| Sustain ON | ON | ON |
| Sustain OFF | OFF | OFF |

Fig. 6 shows the timing schedule for the proposed driving scheme of Fig. 4(b) that has no path switch and merges the roles of power switches by using the new gate driver. The operational modes of switching cycle are described below, and current paths corresponding to the sustain period are shown in Fig. 7.

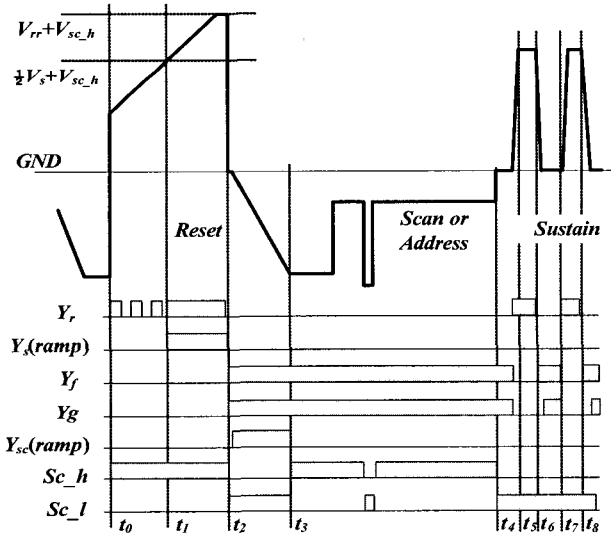



Fig. 6 Timing chart for the proposed system of Fig. 4 (b)

**Reset Period (Ramp-Rising):**

During $t_0 - t_1$, relatively short gate pulses are applied to $Y_r$ until the voltage at point 3 of Fig. 4 (b) reaches the level of $V_s/2$. Because the high side transistors of the scan ICs are turned on during this period to add the $V_{sc\_h}$ on the Y electrode voltage $V_y$, the level of $V_s/2$ at point 3 is equivalent to $V_y$ of $V_s/2 + V_{sc\_h}$.

Turning on the $Y_r$ charges the $C_p$ with a current flowing through the path of $V_s/2 \rightarrow L_y \rightarrow D_r \rightarrow Y_r \rightarrow$ *Scan IC (high side)* $\rightarrow C_p$. Neglecting parasitic circuit components and voltage drops in the circuit, the inductor current $i_{Ly}$ during on time, $t_{on}$, and the voltage increment of the panel $\Delta v_{Cp}$ can be expressed as (1).

$$i_{Ly}(t) = \sqrt{C_p / L_y} \cdot [V_s / 2 - v_{Cp}(0)] \cdot \sin \omega t$$
$$\Delta v_{Cp}(t) = [V_s/2 - v_{Cp}(0)] \cdot (1 - \cos \omega t_{on}) \quad (1)$$

where, $\omega = 1/\sqrt{L_y C_p}$ and $0 < t < t_{on}$. The $v_{Cp}(0)$ represents the potential $V_y$ referred at point 3 before turning on the $Y_r$. Equation (1) shows that the $\Delta v_{Cp}$ is varied by the $t_{on}$ of $Y_r$. After $V_y$ increases to $V_s/2 + V_{sc\_h}$ level, $Y_s$ can be operated when either the sustain or reset is turned on by the reset gate signal shown as $Y_s$(*ramp*) in Fig. 6 to generate the ramp-up voltage waveform.

**Reset Period (Ramp-Falling):**

At $t = t_2$, $V_y$ rapidly goes to zero voltage level by turning on $Y_f$ and $Y_g$. After that $Y_{sc}$ is turned on by the reset gate signal shown as $Y_{sc}$(*ramp*).

**Scan Period:**

The scan ICs impose line-by-line sequential scan pulses to each Y electrode, and corresponding data are applied in data electrodes by data buffers. Turning on the switches $Y_f$, $Y_g$, and $Y_{sc}$ is required to maintain the scan voltage $V_{scan}$ that has negative value.

**Sustain Period:**

During this period, the addressed cells are lighted by sustain pulses. The Y voltage rises toward $V_s$ by turning on the $Y_r$. The switch $Y_s$ is turned on at $t = t_5$. X and Y voltages are alternating from mode 1.

Mode 1 ($t_6 - t_7$): Turning on $Y_f$ and the switch $X_r$, rising switch in X board, makes the $v_{cp}$ change from $V_s$ to $-V_s$ through the path of *X board* $\rightarrow C_p \rightarrow Y_f \rightarrow D_f \rightarrow L_y \rightarrow V_s/2$ as shown in Fig. 7(a) with the initial condition of $v_{cp} = V_s$. Two inductors in X and Y boards are involved in the

$LC$ resonance. The panel voltage $v_{cp}$ and the current $i_{cp}$ during the sustain-falling period can be obtained as (2).

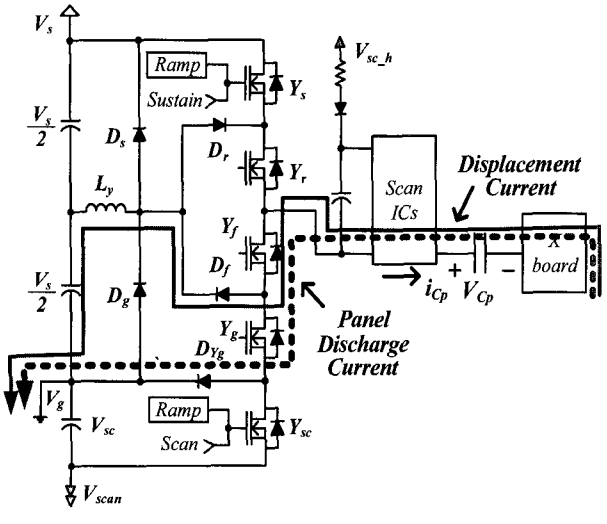
$$v_{cp}(t) = V_s \cdot \cos\omega(t - t_6)$$
$$i_{cp}(t) = -V_s/Z \cdot \sin\omega(t - t_6) \quad (2)$$
$$\text{where, } Z = \sqrt{L/C_p},\ \omega = 1/\sqrt{LC_p},\ L = L_x + L_y$$

After $v_{cp}$ becomes $-V_s$, $Y_g$ and $X_s$ are turned on, and the power for plasma discharge is supplied via *X board* → $C_p$ → $Y_f$ → $Y_g$ → $D_{Yg}$ → *GND* as shown as the dotted line in Fig. 7(a).

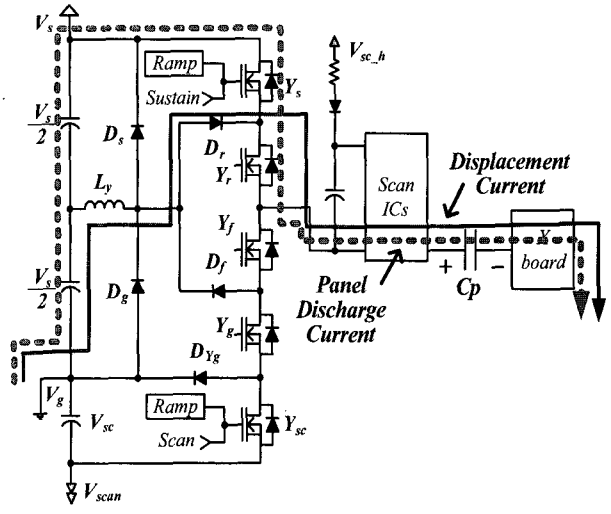
Mode 2 ($t_7$ – $t_8$): Turning on the switches $Y_r$ and $X_f$, falling switch in X board, makes the $v_{cp}$ change from $-V_s$ to $V_s$ through the path of $V_s/2$ → $L_y$ → $D_r$ → $Y_r$ → $C_p$ → *X board* with the initial condition of $v_{cp} = -V_s$. The $v_{cp}$ and $i_{cp}$ for the rising sustain pulse can be expressed as (3).

$$v_{cp}(t) = -V_s \cdot \cos\omega(t - t_7)$$
$$i_{cp}(t) = V_s/Z \cdot \sin\omega(t - t_7) \quad (3)$$

After the $v_{cp}$ becomes $V_s$, the switches $Y_s$ and $X_g$ are turned on to support the gas discharge illustrated as the dotted line in Fig. 7(b), while $Y_r$ remains on status. At $t = t_8$, switching operations are repeated from mode 1.




(a)




(b)

Fig. 7 The path of panel currents during period of (a) sustain –falling and (b) sustain-rising

Table 2 compares power switches used in the conventional and proposed systems. It clearly shows that the proposed system uses fewer power devices with a lower voltage rating.

Table 2 Power devices used in conventional and proposed systems

| Devices | Conventional | Proposed |
|---|---|---|
| $Y_s$ | 88N30(300V) | 88N30(300V) |
| $Y_{pn}$ | 88N30(300V) | none |
| $Y_{rr}$ | SK2837(500V) | none |
| $Y_{fr}$ | SK2837(500V) | none |
| $Y_{sc}$ | 14NK60(600V) | 88N30(300V) |
| $D_{Yg}$ | none | 40P03(300V) |

## 4. Verifications

### 4.1 Simulation Results

Fig. 8 shows the Y voltage waveform for 1 TV subfield that has a main reset simulated by Pspice® with parameters listed in Table 3. It can be clearly shown that the generated Y voltage of the proposed system is identical to that of the conventional driving circuit. As shown in the timing chart of Fig. 6, $Y_r$ has been turned on/off repeatedly until $t = t_1$ when $V_y$ rises up to $V_s/2 + V_{sc\_h}$ voltage level, and then $Y_s$ is turned on by the ramp gate signal.

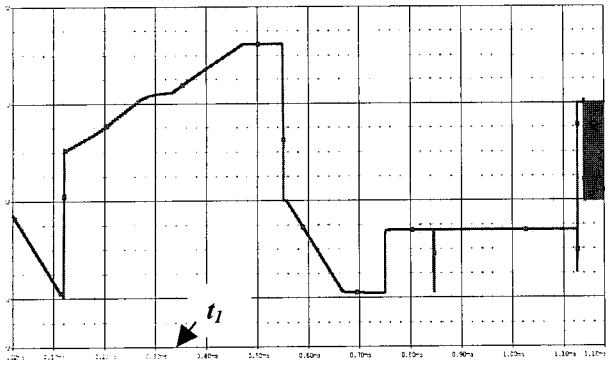



Fig. 8 Simulated Y voltage waveform having main reset (200V/div., 100$\mu s$/div.)

Table 3 Parameters used in simulations for the proposed circuit of type II

| Parameters | Value |
|---|---|
| Inductor | 250 $nH$ |
| Panel capacitance | 100 $nF$ |
| Switching frequency | 200 $kHz$ |
| Rising falling time | 700 $ns$ |

### 4.2 Experimental Results using the New Gate Driver

Experiments have been carried out using a 42-inch PDP panel to demonstrate the validity of the new gate driver. The new driver circuit for $Y_s$ and $Y_{rr}$ has been implemented in the PDP driving circuit having the conventional topology of Fig. 3. In other words, the gate driver shown in Fig. 5(a) has been replaced by the novel driver presented in Fig. 5(b). Fig. 9 shows the ramp rising $V_y$ and gate-source voltage waveform of $Y_s$ using the novel gate driver. Two levels of gate-source voltage of $Y_s$ appear in Fig. 9; one having the level of around threshold voltage during $t_0 - t_1$ and another having around 15 V after $t = t_1$, which is the voltage level of the gate power supply. Consequently, Fig. 9 implies that $Y_s$ has been turned on and off in two different ways by using the novel gate driver.

There is a demand for the reset pulses of $V_y$ to have several different slopes corresponding to the ambient temperature to effectively regulate the wall charge conditions under various operating environments for the plasma TVs. It is possible to generate the ramp-rising $V_y$ voltage waveforms with either a continuous turn-on signal or short gate pulses. Unless using additional circuits that can change circuit parameters especially the value of an external resistor and a capacitor, it is hard to generate $V_y$ having different slopes. Therefore, to realize this function with the same circuit, the proposed scheme varies the slope of reset waveforms by changing the switching frequency or the on-time of $Y_s$ in stead of adding additional circuits. Therefore, gate-source voltages waveforms of $Y_s$ during $t_0 - t_1$ are shown as short gate pulses. At $t = t_1$, the gate signals from the sustain gate IC, which has around 15V gate output, immediately turns on $Y_s$ either by a continuous on signal as shown in Fig. 9(a) or by short pulses in Fig. 9(b). In fact, during the ramp-up period, it is not necessary to turn on $Y_s$ with the fast on-process. Therefore, it should be noted that the experiments illustrated in Fig. 9 have been performed to verify the validity of the new gate driver by showing that the gate-source voltage of $Y_s$ shows two voltage levels required for slow or fast switching action. This means that two operations of reset and sustain have been realized by one $Y_s$ switch by using the new gate driver.

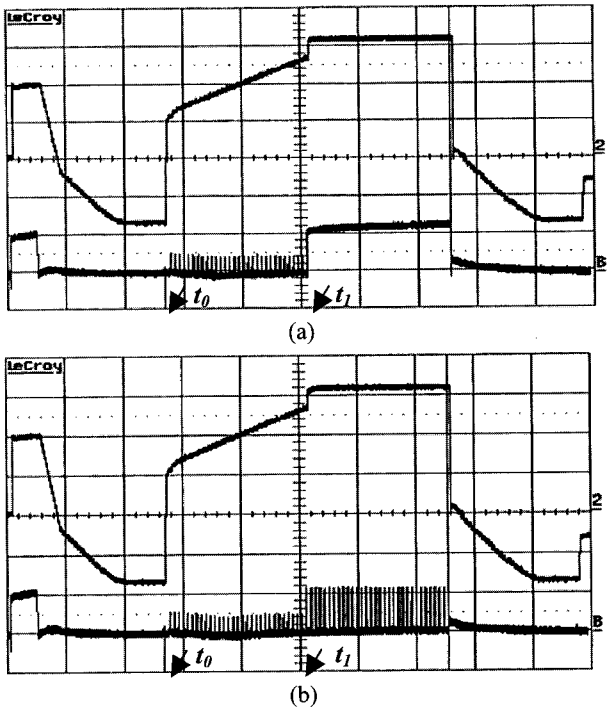



Fig. 9 Experimental $V_y$ voltage waveforms (100V/div., 100$\mu s$/div.) and gate-source voltage of $Y_s$ (10V/div.) during the ramp-rising reset period (a) by imposing a continuous turn-on gate signal at $t = t_1$ and (b) short pulses at $t = t_1$

## 5. Conclusions

This paper has proposed a PDP driving circuit that eliminates path switches and a new gate driver that can merge the function of reset switches to sustain or scan switches. Only five switches with a voltage rating lower than $V_s$ have been used to generate the voltage waveforms for a gas discharge, and this scheme has been devised to realize low-cost driving circuits by considering not just sustain circuits but the entire PDP system. The simulated Y voltage waveform of the proposed scheme has been in accordance with that of the conventional system. The experimental results for the new gate driver implemented in 42 inches panel have shown that the gate drive can turn on the switch with slow or fast switching actions.

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