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A New Single-Stage PFC AC/DC Converter with Low Link-Capacitor Voltage

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ABSTRACT

A conventional Single-Stage Power-Factor-Correction (PFC) AC/DC converter has a link capacitor voltage problem under high line input and low load conditions. In this paper, this problem is analyzed by using the voltage conversion ratio of the DC/DC conversion cell. By applying this analysis, a new Single-Stage PFC AC/DC converter with a boost PFC cell integrated with a Voltage-Doubler Rectified Asymmetrical Half-Bridge (VDRAHB) is proposed. The proposed converter features good power factor correction, low current harmonic distortions, tight output regulations and low voltage of the link capacitor. An 85W prototype was implemented to show that it meets harmonic requirements and standards satisfactorily with near unity power factor and high efficiency over universal input.

Keywords: Single-Stage Power-Factor-Correction (PFC), Voltage-Doubler Rectified Asymmetric Half-Bridge

1. Introduction

Conventional off-line power converters with diode-capacitor rectifier front-ends have distorted input current waveforms with high harmonic content. Since these converters have a low power factor, they cannot meet harmonic regulations and standards such as the European line-current harmonic regulations defined in the IEC 61000-3-2 document and the Japanese input-harmonic current specifications. To comply with these standards, a number of single-stage and two-stage PFC circuits have been developed and reported in the literature. In the two-stage approach, it is customary to add a power-factor corrector ahead of the dc/dc converter to provide a regulated and isolated dc output. This approach provides good power-factor correction and fast output regulation, but the power-factor corrector increases the size and cost of the overall system. Therefore, the two-stage approach is not desirable in low power applications [1-2].

Recently, many single-stage approaches have been suggested to achieve both power-factor correction and power conversion from the ac line to a desired dc output [3]. Since these topologies have a PFC cell integrated with a DC/DC conversion cell and both cells share an active switch and controller, the single-stage approach is a better choice from a cost point of view. Unfortunately, most of the proposed converters have one or more of the following disadvantages: large low-frequency output voltage ripple, low efficiency due to the switching and rectification loss, variable switching frequency and high-voltage stress on

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the switch [1-7].

In this paper, specifically, the link capacitor voltage is analyzed by using the voltage conversion ratio of the DC/DC conversion cell of a single-stage PFC AC/DC converter. Moreover, by adapting this analysis, a new single-stage PFC AC/DC converter with boost for PFC cells integrated with VDRABH for DC/DC conversion cell is proposed. To confirm the validity of the proposed converter, the operation principles and the experimental results of an 85W prototype will be presented.

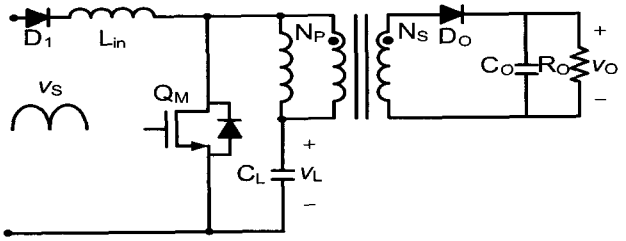


Fig. 1 Conventional Single-Stage PFC AC/DC Converter

2. Analysis of Link Capacitor Voltage

A conventional Single-Stage PFC AC/DC converter with a PFC cell operated in Discontinuous Conduction Mode (DCM) and a DC/DC cell operated in Continuous Conduction Mode (CCM) is shown in Fig. 1 [5]. Since the DC/DC cell is operated in CCM, the duty ratio does not change with load variation as shown in Fig. 2. Moreover, the DC conversion ratio of the PFC cell increases as the load decreases as shown in Fig. 3. Therefore, the link capacitor voltage increases as the load decreases. Due to the high voltage stress and the impossibility of using a commercial capacitor, the increase of the link capacitor voltage is one major problem with Single-Stage PFC AC/DC converters. To overcome this problem, there have been many approaches, for example, a Bi-flyback PFC converter [1], DC bus-voltage feedback [3], a Charge-pump PFC converter [4] and Variable Frequency Modulation.

The characteristics of this link capacitor voltage can be explained by using the voltage conversion ratio of the DC/DC conversion cell of the single-stage PFC AC/DC converter. The relation between the link capacitor voltage, v_L, and the output voltage, v_O can be expressed as a function of the duty ratio, D.

$$\frac{V_O}{V_L} = f(D) \tag{1}$$

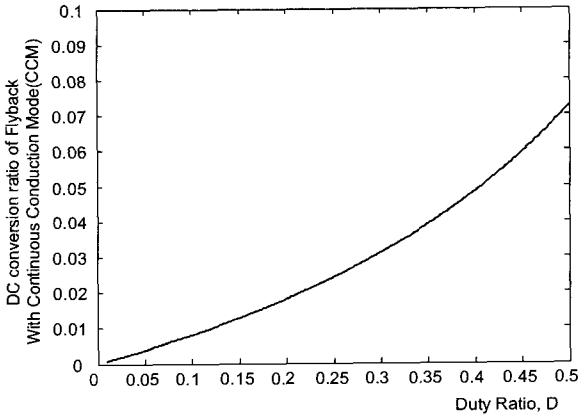


Fig. 2 DC conversion ratio of Flyback with CCM

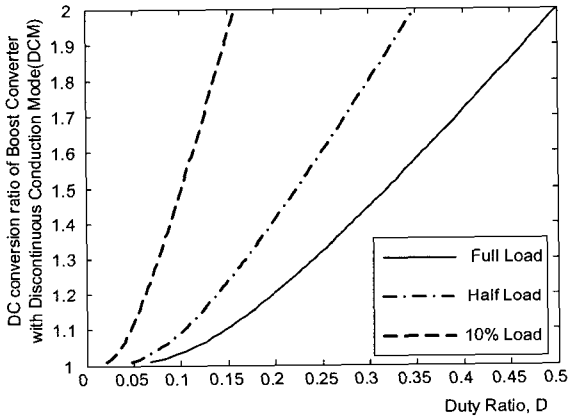


Fig. 3 DC conversion ratio of Boost with DCM

In a general single-stage PFC AC/DC converter, f(D) is highly dependent on the duty ratio, D, as shown in Fig. 4(a). Since the voltage conversion ratio, f(D), varies with load changes, the link capacitor voltage, v_L has to vary as the load changes to regulate the output voltage, v_O. As a result, the link capacitor voltage increases as the load decreases.

In the case where f(D) is minimally dependent on the duty ratio, D, as shown in Fig. 4(b), the link capacitor voltage increase problem can be resolved. Since the voltage conversion ratio, f(D), hardly ever varies with load variations, the link capacitor voltage, v_L only slightly varies to regulate the output voltage, v_O. For this reason, in the event that one converter has the voltage conversion

ratio of the DC/DC conversion cell as shown in Fig. 4(b) it can be applied to a single-stage PFC AC/DC Converter without the link capacitor voltage problem.

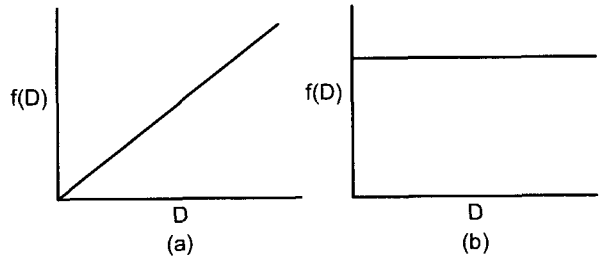


Fig. 4 (a) Rough voltage conversion ratio of DC/DC conversion cell in general single-stage PFC converter

(b) Roughly desired voltage conversion ratio of DC/DC conversion cell in proposed single-stage PFC converter

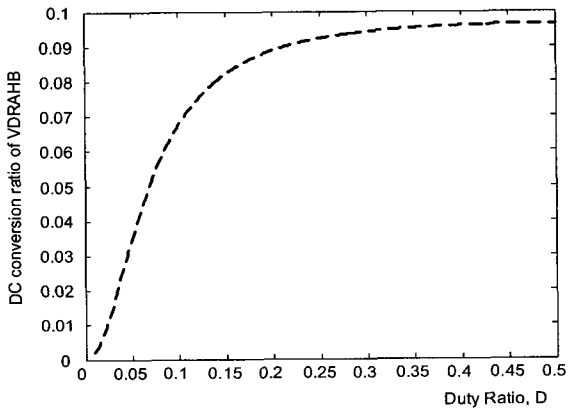


Fig. 5 DC conversion ratio of VDRAHB

The voltage conversion ratio of the Voltage Doubler Rectified Asymmetric Half-Bridge(VDRAHB) converter is plotted as a function of the duty ration, D, as shown in Fig. 5. Since f(D) of the VDRAHB is minimally dependent on the duty ratio, D, a new single-stage PFC AC/DC converter in which a VDRAHB converter is applied to the DC/DC conversion cell using a boost PFC cell is proposed as shown in Fig. 6.

3. Operational Principles

The circuit diagram of the proposed single-stage PFC AC/DC converter is shown in Fig. 6. The proposed circuit is composed of a boost for the PFC cell integrated with a VDRABH for the DC/DC conversion cell.

3.1 Mode Analysis

The operation of the proposed converter can be classified into the three modes (t_0~t_0') and the corresponding waveforms are presented in Fig. 7.

Mode 1 (M_1, t_0~ t_1) : Mode 1 begins at t_0 when Q_M is turned-on. The input voltage, v_S, is applied to the inductor L_{in}, i_{Lin} starts to build up from zero. At the same time, (v_L-v_H) is applied to the primary winding of transformer T_1, i_{Lk} increases. The slopes of these currents, i_{Lin}, i_{Lk} are given by

$$\frac{d}{dt} i_{Lin}(t) = \frac{V_S}{L_{in}} \tag{2}$$

$$\frac{d}{dt} i_{Lk}(t) = \frac{1}{L_K}\left[V_L - V_H - \frac{N_P}{N_S}(V_O - V_{SB})\right] \tag{3}$$

Mode 2 (M_2, t_1~ t_2) : Mode 2 begins at t_1 when Q_M is turned-off and Q_A is turned-on, respectively. As (v_S-v_L) is applied to the inductor L_{in}, i_{Lin} starts to flow through Q_A, and decreases to zero. As -v_H is applied to the primary winding of T_1, i_{Lk} decreases. The slopes of these currents, i_{Lin}, i_{Lk} are determined by

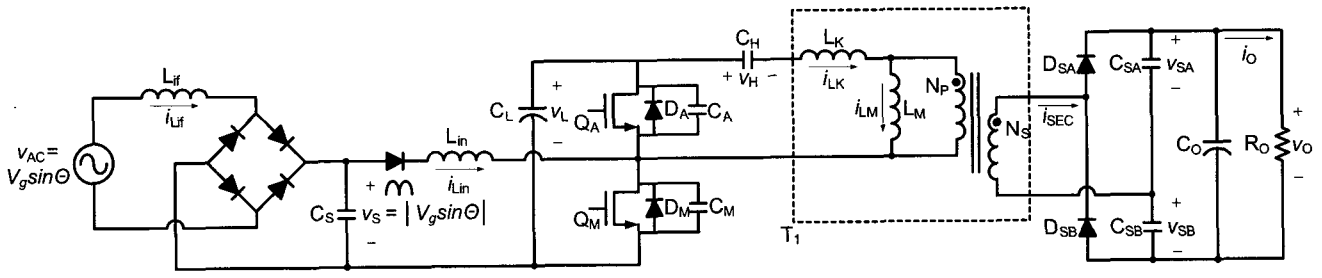


Fig. 6 Circuit Diagram of the proposed converter

$$\frac{d}{dt}i_{Lin}(t)=\frac{1}{L_{in}}(V_S-V_L) \tag{4}$$

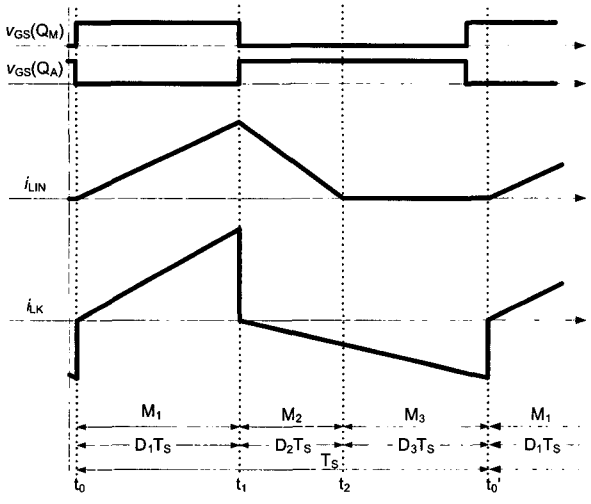


Fig. 7 Key Waveforms of the proposed converter

$$\frac{d}{dt}i_{Lk}(t)=\frac{1}{L_K}\left[-V_H+\frac{N_P}{N_S}(V_O-V_{SA})\right] \tag{5}$$

**Mode 3 (M_2, t_2~ t_0`)** : Mode 3 begins at $t_2$ when $i_{Lin}$ decreased to zero and $i_{Lk}$ decreases with the same slope during mode 2. Mode 3 ends when $Q_M$ is turned-on and starts another switching cycle at $t_0$`.

The slope of current, i_{Lk} is determined by the following equation.

$$\frac{d}{dt}i_{Lk}(t)=\frac{1}{L_K}\left[-V_H+\frac{N_P}{N_S}(V_O-V_{SA})\right] \tag{6}$$

3.2 Input-Output Voltage Conversion Ratio

The voltage conversion ratio of the proposed converter can be divided into two conversion ratios. M_{boost} is the voltage conversion ratio of the boost converter between v_g and v_L, and M_{VDRAHB} is the voltage conversion ratio of the VDRAHB converter between v_L and v_O. Each conversion ratio can be expressed as :

$$M_{boost}=\frac{V_L}{V_g} \tag{7}$$

$$M_{VDRAHB}=\frac{V_O}{V_L} \tag{8}$$

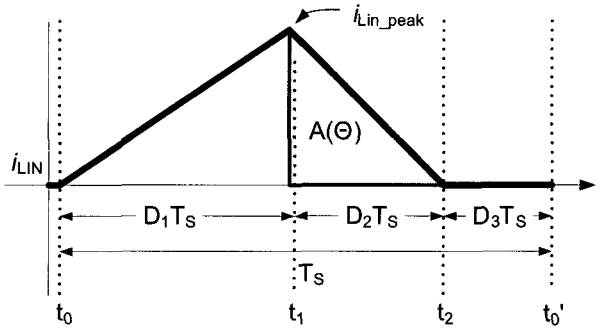


Fig. 8 Waveform of the boost inductor current

The waveform of the boost inductor current is shown in Fig. 8. By applying the voltage-second balance of L_{in} during one switching cycle, Ts, the following equations are derived.

$$\frac{V_S}{L_{in}}D_1T_S=\frac{V_L-V_S}{L_{in}}D_2T_S \tag{9}$$

$$D_2=\frac{\sin\theta}{M_{boost}-\sin\theta}\times D_1 \tag{10}$$

The peak current of L_{in} is determined by the following equation.

$$i_{Lin\_peak}=\frac{V_S}{L_{in}}\times D_1T_S \tag{11}$$

A(Θ), which represents the charging energy into C_L during one switching cycle, T_S, is derived as follows by using (7) and (8).

$$\begin{aligned}A(\theta)&=\frac{1}{2}\times i_{Lin\_peak}\times D_2T_S\\&=\frac{D_1^2\times V_g\sin^2\theta}{2\times L_{in}\times(M_{boost}-\sin\theta)\times F_S^2}\end{aligned} \tag{12}$$

,where F_S is the switching frequency of the converter.

Since the average of B(Θ), which is the average of A(Θ) during T_S, during the 120Hz is equal to the value of

the input current of VDRAHB as shown in Fig. 9, the voltage conversion ratio of the boost converter, M_{boost} can be obtained as follows.

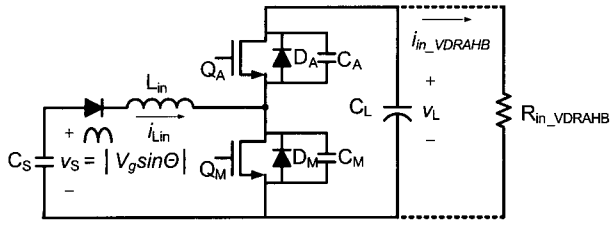


Fig. 9 Circuit Diagram with equivalent resistance

$$\frac{V_L}{R_{in\_VDRAHB}} = \frac{1}{\pi}\int_0^{\pi} B(\theta)d\theta = \frac{1}{\pi}\int_0^{\pi}\frac{A(\theta)}{Ts}d\theta = \frac{1}{\pi}\int_0^{\pi}\frac{D_1^2 \times V_g \sin^2\theta}{2\times L_{in}\times F_S\times\pi\times(M_{boost}-\sin\theta)}d\theta \quad (13)$$

,where R_{in_VDRAHB} is the equivalent input resistance of the Voltage-Doubler Rectified Asymmetric Half-Bridge Converter. R_{in_VDRAHB} can be expressed as follows.

$$R_{in\_VDRAHB} = (\frac{V_L}{V_O})^2 \times R_O = \frac{R_O}{M_{VDRAHB}^2} \quad (14)$$

By arranging the (13), M_{boost}, can be expressed as :

$$M_{boost} = \frac{V_L}{V_g} = \frac{D_1^2 R_{in\_VDRAHB}}{2\times L_{in}\times F_S\times\pi}\int_0^{\pi}\frac{\sin^2\theta}{M_{boost}-\sin\theta}d\theta \quad (15)$$

The voltage conversion ratio of the VDRAHB has been described in reference [6] as follows.

$$M_{VDRAHB} = \frac{V_O}{V_L} = \frac{\frac{N_S}{N_P}D_1^2(1-D_1)^2}{D_1^2(1-D_1)^2 + \frac{2L_kF_S}{R_O}\left(\frac{N_S}{N_P}\right)^2\left[D_1^2+(1-D_1)^2\right]} \quad (16)$$

, where D_1 is the duty ratio of Q_M and F_S is the switching frequency.

The DC conversion ratio of M_{boost} and M_{VDRAHB} are plotted as a function of the duty ratio in Fig. 3 and Fig. 10 with load variation, respectively, based on the design specifications and the circuit parameters for the 85W prototype in Table 1 and Table 2, respectively.

Table 1 Design specifications

Specification	Value
Input voltage, V_S	90V ~ 270V_{AC_RMS}
Output voltage, V_O	18.5V
Max. output power, $P_{O,max}$	85W
Switching frequency, f_S	100kHz

Table 2 Circuit Parameters

Parameter		Value
Transformer	N_P: N_S	51 : 5
	L_M	1.37mH
	L_K	12uH
C_H		2.2uF / 630V
C_{SA} & C_{SB}		22μF / 25V, 2EA

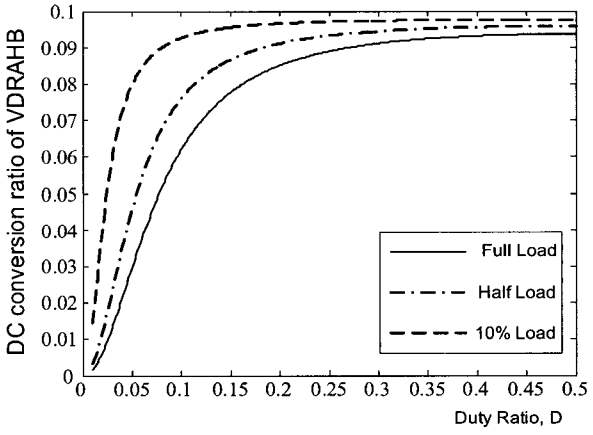
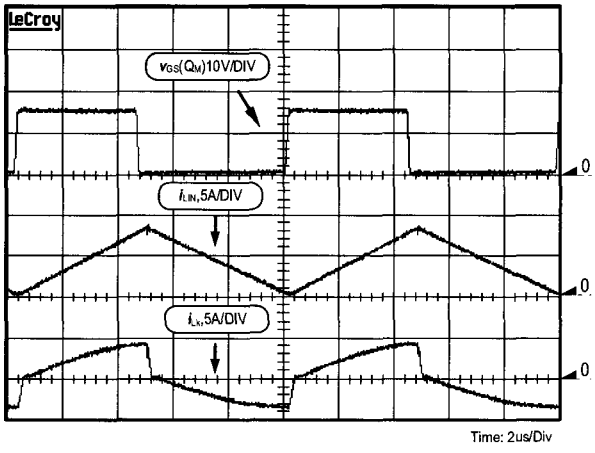


Fig. 10 DC conversion ratio of VDRAHB

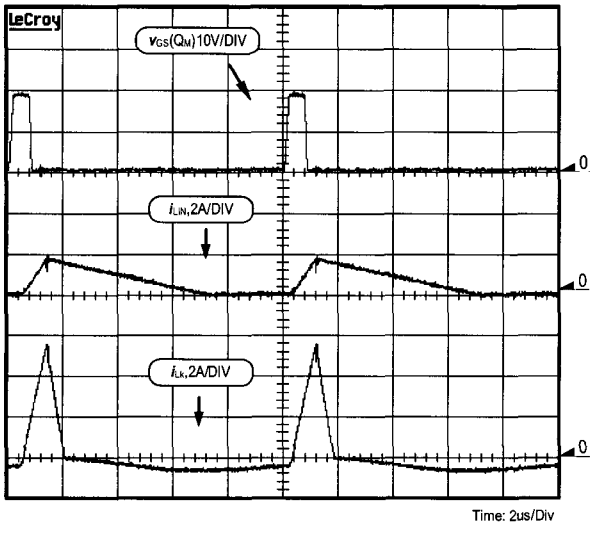
4. Experimental Results

To verify the operational principles and the feasibility of the proposed single-stage PFC AC/DC converter, an 85W prototype of the proposed converter has been implemented. The design specifications and circuit parameters of this prototype are the same as presented in Table 1 and Table 2, respectively. Fig. 11(a) and Fig. 11(b) show the Boost PFC cell operated in Boundary Conduction Mode(BCM) at 90 $V_{AC,RMS}$ and 270$V_{AC,RMS}$, respectively. The line input current follows the shape of

the line input voltage as shown in Fig. 12(a) and Fig. 12(b) at $90V_{AC,RMS}$, and $270V_{AC,RMS}$, respectively. The power factors and the efficiencies of the proposed converter are measured as presented in Fig. 13(a) and Fig. 13(b), respectively. The harmonic line currents of the proposed converter are analyzed as shown in Fig. 13(c). The proposed converter meets the harmonic requirements of IEC 61000-3-2 Standards. The voltage of the link capacitor is sustained below 405V during line and load variations as shown in Fig. 13(d). Therefore, the commercial capacitor can be used in the proposed converter.

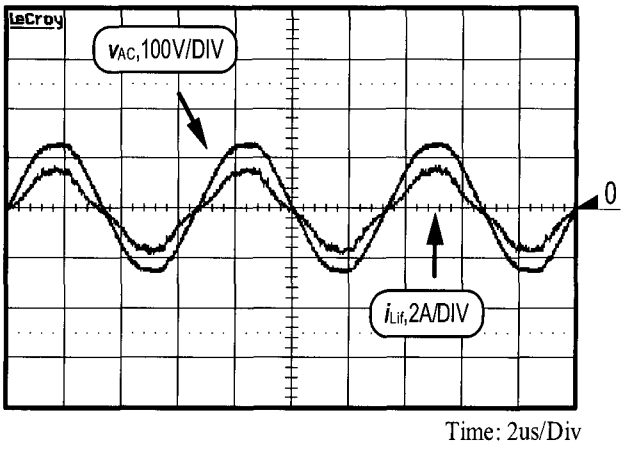


(a)

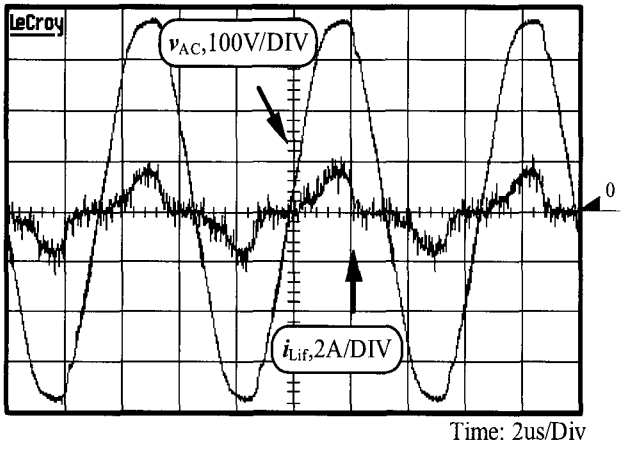


(b)

Fig. 11 Experimental Key waveforms
(a) V_{AC_RMS} = 90V (b) V_{AC_RMS} = 270V

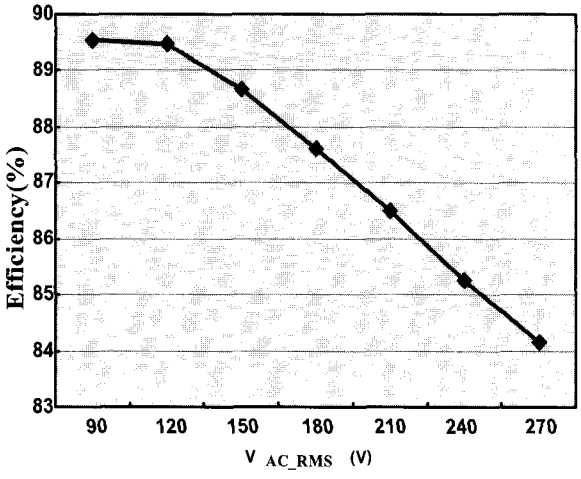


(a)

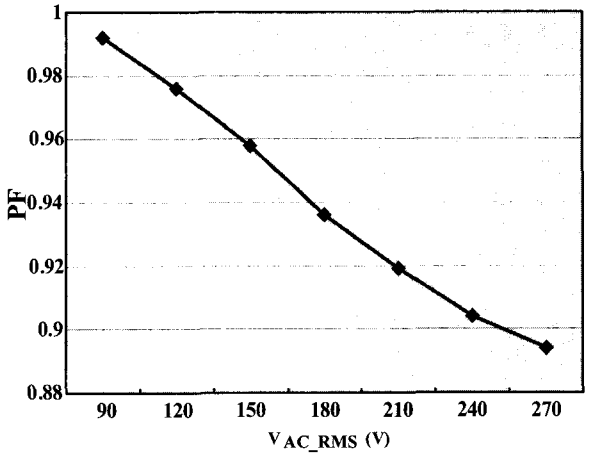


(b)

Fig. 12 Line Input Voltage and Current Waveforms
(a) V_{AC_RMS} = 90V (b) V_{AC_RMS} = 270V



(a)



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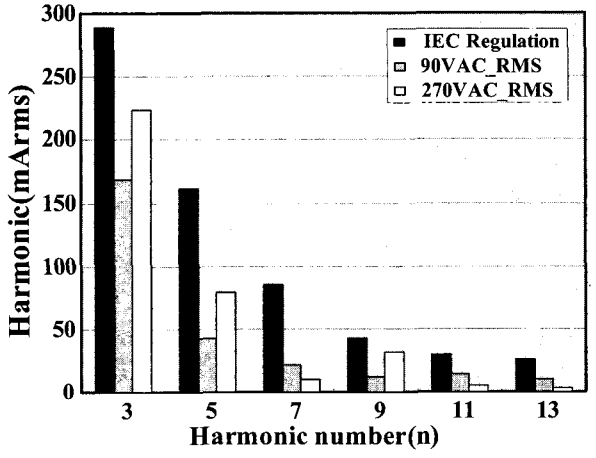
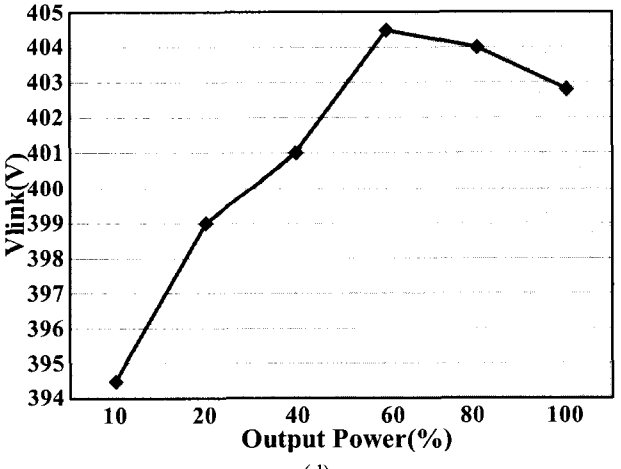


(c)



(d)

Fig. 13 (a)Measured Efficiency, (b)Measured Power Factor, (c) Measured Harmonic Components, (d)Measured Link Capacitor Voltage

5. Conclusions

In this paper, the link capacitor voltage problem in single-stage PFC AC/DC converters is analyzed from the point of view of the voltage conversion ratio of the DC/DC conversion cell and a new single-stage PFC AC/DC converter is proposed. Based on the experimental results of an 85W converter, the operation principles and main features of the proposed converter are confirmed. Since the link capacitor voltage of the proposed converter could be sustained below 405V under all load and line input conditions, the commercial capacitor can be used. Moreover, the proposed converter met the harmonic regulations and had high efficiency. Therefore, the proposed converter can be expected to be widely used for low power applications such as laptop adapters.

References

[1] M. H. Kheruluwala, R. L. Steingerwald, and R. Gurumoorthy, "Fast Response high power factor converter with a single power stage", in *IEEE Proc. PESC*, 1991, pp. 769~779.

[2] J. Zhang, Milan M. Jovanovic, and Fred C. Lee, "Comparison Between CCM Single-Stage And Two –Stage Boost PFC Converters", in *IEEE Proc. APEC*, 1999, pp. 335~341.

[3] R. Redl, L. Balogh, and N. O. Sokal, "A new family of single-stage isolated power-factor correctors with fast regulation of the output voltage", in *IEEE Proc. PESC*, 1994, pp. 1137~1144.

[4] C. Qiao, and K. M. Smedley, "A topology survey of single-stage power factor corrector with a boost type input-current-shaper", in *IEEE Proc. APEC*, 2000, pp. 460~467.

[5] M. Madigan, R. Efickson, and E. Ismail, "Integrated high-quality rectifier-regulators", in *IEEE Proc. PESC*, 1992, pp. 1043~1051.

[6] W. Qiu, W. Wu, S. Luo, W. Gu, and I. Batarseh, "A Bi-flyback PFC converter with low intermediate bus voltage and tight output voltage regulation for universal input applications", in *IEEE Proc. APEC*, 2002, pp. 256~262.

[7] A.A. Aboulnaga, and A. Emadi, "Integrated magnetic BIFRED converter with lower intermediate capacitor voltage", in *IEEE Proc. PESC*, 2004, pp. 1551~1556.

[8] C. E. Kim, S. K. Han, and G. W. Moon, "A New High

Efficiency and Low Profile On-Board DC/DC Converter for Digital Car Audio Amplifier", in Proc. Journal of Power Electronics, Vol. 6, No. 1, pp. 83~93, Oct. 2005.

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