A Millimeter-Wave LC Cross-Coupled VCO for 60 GHz WPAN Application in a 0.13-μm Si RF CMOS Technology

Namhyung Kim*, Seungyong Lee, and Jae-Sung Rieh***

Abstract—**Recently, the demand on mm-wave (millimeter-wave) applications has increased dramatically. While circuits operating in the mm-wave frequency band have been traditionally implemented in III-V or SiGe technologies, recent advances in Si MOSFET operation speed enabled mm-wave circuits realized in a Si CMOS technology. In this work, a 58 GHz CMOS LC cross-coupled VCO (Voltage Controlled Oscillator) was fabricated in a 0.13-μm Si RF CMOS technology. In the course of the circuit design, active device models were modified for improved accuracy in the mm-wave range and EM (electromagnetic) simulation was heavily employed for passive device performance prediction and interconnection parasitic extraction. The measured operating frequency ranged from 56.5 to 58.5 GHz with a tuning voltage swept from 0 to 2.3 V. The minimum phase noise of -96 dBc/Hz at 5 MHz offset was achieved. The output power varied around -20 dBm over the measured tuning range. The circuit drew current (including buffer current) of 10 mA from 1.5 V supply voltage. The FOM (Figure-Of-Merit) was estimated to be -165.5 dBc/Hz.**

Index Terms—**Millimeter-wave, WPAN, VCO, RFCMOS, electromagnetic simulation**

I. INTRODUCTION

The mm-wave frequency band, defined as the frequency range from 30 to 300 GHz with corresponding wavelength in the millimeter range, is attracting growing interest these days. Increasingly popular applications in this band include 60 GHz wireless personal area network (WPAN) systems, 77 GHz automotive radar systems, and 94 GHz image sensing systems. In particular, the 60 GHz WPAN systems are expected to find applications in the area of consumer electronics, potentially leading to a huge emerging market.

The frequency band near 60 GHz, in fact, suffers from a raised attenuation level in the atmosphere due to the resonance with oxygen molecules, preempting its application in the long-haul communication systems. However, such apparently adverse characteristic turned out to be highly favorable for personal area network systems, in which high isolation is desired to avoid channel interference between adjacent areas. From this point of view, the frequency band near 60 GHz is highly opted for WPAN or other narrow area communication applications. In addition, a frequency band of several GHz range near 60 GHz is open for unlicensed use in various regions over the world, facilitating the immediate use of the band for WPAN applications as shown in Fig. 1 [1]. Such availability adds to the attraction of the 60 GHz frequency band.

In the past years, III-V compound semiconductor technologies were dominantly used for the implementation of mm-wave circuits. However, recent advances in Si technologies have enabled their applications in the mm-wave circuits as well. It was SiGe BiCMOS technology that first proved the successful application of Si-based technology to the mm-wave circuits [2]. More recently, the application of Si CMOS technology, which has long been considered unsuitable for high frequency application, has

Manuscript received Nov. 24, 2008; revised Dec. 1, 2008.
* School of Electrical Engineering, Korea University, Seoul 136-713, Korea
** Kasan R&D campus, LG electronics, Seoul 153-802, Korea
E-mail : scone82@korea.ac.kr

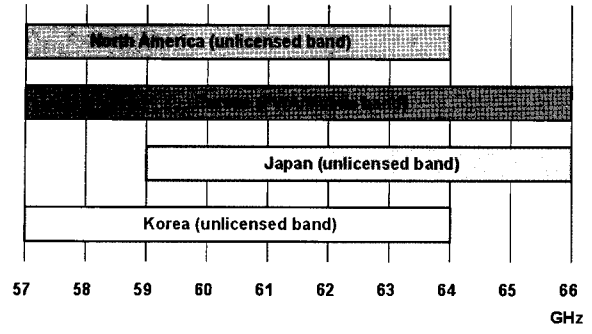

Fig. 1. Frequency band available for 60 GHz WPAN application in various regions over the world.

been successfully demonstrated for the mm-wave applications [3,4]. This was possible owing to the recent rapid enhancement in the operating speed of Si MOSFET devices which now exhibit cutoff frequency (f_T) exceeding 400 GHz [5].

VCO is one of the main building blocks in the transceivers for wireless communication systems, which is employed to generate the local oscillation frequency for modulation/demodulation. While ring oscillators are widely adopted in digital-based applications, LC cross-coupled oscillators and Colpitts oscillators dominate the applications in RF and mm-wave frequency band owing to their excellent phase-noise performance despite the rather larger area occupation. In this work, an NMOS LC cross-coupled VCO for 60 GHz WPAN applications is designed and fabricated in 0.13-μm Si RFCMOS technology and then characterized.

II. Technology

Dongbu Hitek 0.13-μm 1P8M Si RF CMOS technology was employed for the implementation of the circuit in this work. It offers a UTM (Ultra Thick Metal) in the BEOL (Back-End Of the Line) process along with various active and passive devices required for RF applications. NMOSFET provides the cut-off frequency (f_T) of around 80 GHz and the maximum oscillation frequency (f_{max}) typically exceeding 100 GHz although it shows a strong layout dependence. Fig. 2 shows the current gain and MSG/MAG (Maximum Stable Gain / Maximum Available Gain) of a typical NMOSFET (5 × 0.13 μm × 2 μm) based on the offered model, from which f_T and f_{max} of 88 GHz and 120 GHz, respectively, are extracted.

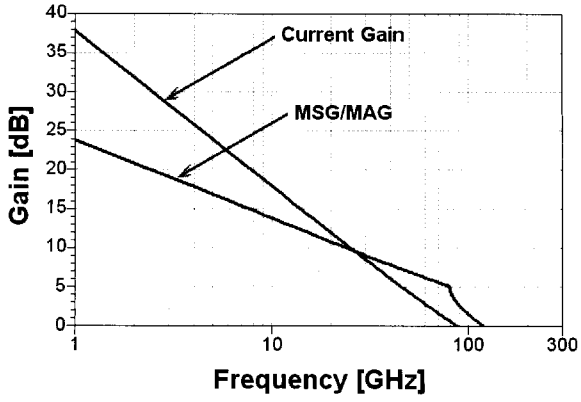

Fig. 2. Current gain and MSG/MAG of a typical NMOSFET (5 × 0.13 μm × 2 μm) offered in the technology.

III. Circuit Design

The schematic of the VCO designed in this work is shown in Fig. 3. The core consists of cross-coupled NMOSFETs and an LC tank composed of two spiral inductors and two accumulation-mode MOS varactors. Source follower buffers are inserted at either end of the differential outputs.

The first step in the design of VCO is to determine the oscillation frequency. It is well known that the oscillation frequency of a LC tank, and hence that of oscillators employing the LC tank, is given as:

$$f_{OSC} = \frac{1}{2\pi\sqrt{L_{eq}C_{eq}}} \quad , \tag{1}$$

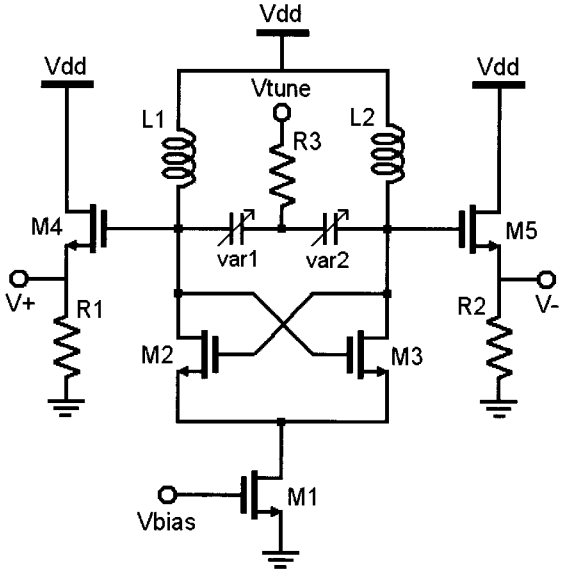

Fig. 3. Schematic of the LC cross-coupled VCO.

where L_{eq} and C_{eq} are the equivalent inductance and capacitance, respectively, of the LC tank core in the VCO. For low frequency designs, the typical values of these parameters are much larger than those of parasitic components and thus are nearly determined by the designed values. In mm-wave designs, however, the required values for L_{eq} and C_{eq} are significantly reduced, while the parasitic components remain roughly at the same level. Hence, the parasitic component values become comparable to the design values and it becomes critical to identify the source of the parasitics and accurately extract their values.

For the VCO topology employed in this work, the equivalent capacitance of the core circuit (C_{eq}) can be described as following:

$$C_{eq} = C_{VAR} + C_{GS} + 4C_{GD} + C_{DB} + C_{GS,b} + C_{GD,b} \ . \quad (2)$$

Note that C_{eq} (and L_{eq} as well) are values seen from the drain node of each cross-coupled NMOSFET in the half circuit. In (2), C_{VAR} is the capacitance of the varactor, C_{GS} and C_{GD} are gate-source and gate-drain capacitance, respectively, and C_{DB} is drain-bulk junction capacitance, all of the core NMOSFET comprising the cross-coupled loop. The factor of 4 arises from the fact that C_{GD} of both transistors are seen from a given drain node and they are further doubled for the half circuit analysis. $C_{GS,b}$ and $C_{GD,b}$ are input capacitances of the buffer. Each of these capacitances can be extracted from the device model. In mm-wave band, the magnitude of C_{VAR} becomes comparable to those of other parasitic terms in (2), which are fixed in their values. Therefore, achieving a high tuning range becomes increasingly difficult as the oscillation frequency increases. The value of L_{eq} can be obtained by accurate EM simulation. As it is closely related to the layout, the details are described in the next section along with other layout issues.

Another important consideration in the VCO design is to make the circuit oscillate. The LC tank in the VCO should satisfy the following condition for the oscillation to occur:

$$(G_m R_P)^2 \geq 1 \ , \quad (3)$$

where G_m is the negative transconductance looking into the cross-coupled pair and R_P is the parallel resistance of the LC tank, which can be roughly given as following:

$$R_P = 2\pi f_{OSC} L_{TANK} Q_L \ . \quad (4)$$

As the value of R_P is fixed once the design of the LC tank is completed (typically for the desired oscillation frequency), the transistor size needs to be tuned to satisfy (3).

The quality factor (Q-factor) is another important parameter for passive devices such as inductors and capacitors. To improve the phase noise of the VCO, inductors and capacitors with high Q-factor should be adopted to the LC tank in the VCO. For low frequency design, the Q-factor of an LC tank is typically limited by that of inductor. For high frequency regime such as mm-wave band, however, the Q-factor of varactor becomes the dominant factor since inductor Q-factor tends to increase while varactor Q-factor decreases with increasing frequency. As the Q-factors of passive devices are determined not only by the process but also by layout, a proper choice of device parameters is important in the stage of circuit design. An accurate estimation of the Q-factor is important as well, and EM simulation has been carried out in this work. As the simulation results may differ for different simulators, data from multiple EM tools were compared for a sanity check [6]. The critical issues of layout are discussed in the next section.

Buffer is the impedance translation structure in the output part of the VCO. Common source (CS) and source follower (SF) topologies are typically employed as the buffer structures, which can translate the impedance of the VCO output. While the CS topology provides a higher gain and thus is preferred when high output power is desired, the input capacitance of the CS topology would be multiplied by its own gain due to the Miller Effect. This causes a reduction in the oscillation frequency of the VCO and, more importantly, the tuning range because the fixed components in C_{eq} are effectively increased. On the other hand, SF buffer exhibits high input and low output impedance compared to the CS case, thereby minimizing the effect on the VCO core and allowing 50 ohm matching easily. For this reason, SF buffer was employed in this work.

The device models provided by the foundry guarantee their accuracy only up to 20 - 30 GHz range for typical CMOS technologies. Therefore, the model performance tends to deviate from the actual performance when fre-

quency enters the mm-wave regime. This necessitates a modification of the model for a better accuracy for mm-wave circuit designs. In this work, such in-house modeling was carried out for active devices based on accurate s-parameter measurement [1] and utilized for the circuit design throughout the work.

IV. Layout Issues

Due to the critical effects of parasitic reactive components with increasing operation frequency, a precise extraction of the parasitic components becomes an important procedure in mm-wave circuit designs. For this reason, EM simulation tools were heavily used in this work to analyze and extract the parasitic components.

As mentioned in section III, the Q-factor of LC tank affects the oscillation condition and the phase noise of the VCO. Hence, the design of inductors with high Q-factor becomes essential in VCO design. Fig. 4 shows a spiral inductor which is designed for high Q-factor in this work. The 45° tilted line is employed to reduce the parasitic inductance. Since attached feed lines behave as additional inductance components, they were included as part of the inductor in the design. Presented in Fig. 5 are the simulated inductance and Q-factor of the spiral inductor incorporated in LC tank, for which the Agilent ADS momentum, a 2.5-D EM field simulator, was used. Inductance of the inductor falls near 120 pH and Q-factor is over 11 at the oscillation frequency.

While the feed lines attached to the inductor were incorporated as part of the inductor, there are additional interconnect lines between device components, which causes interconnects parasitic effects and results in inaccurate simulation results. In order to account for such effects,

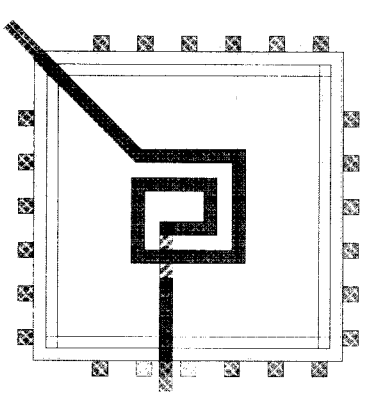

Fig. 4. Spiral inductor employed for the LC tank.

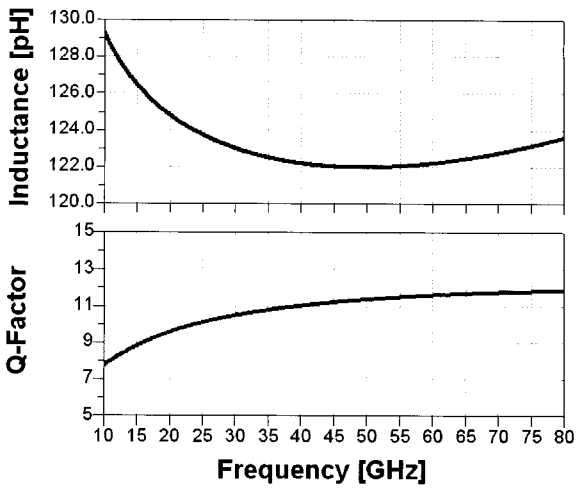

Fig. 5. Inductance and Q-factor of the core inductor obtained from EM simulation.

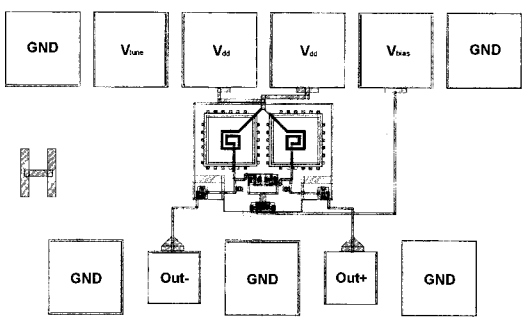

Fig. 6. Complete layout of the VCO.

post-layout multi-port s-parameter simulations were subsequently carried out by using EM simulators [7]. Such simulation procedure can significantly improve accuracy of the circuit design and be more predictable [8].

The complete layout of the designed VCO is provided in Fig. 6. Chip size including RF and DC supply pads is 580 μm × 340 μm. To minimize the substrate loss, ground metal with metal 1 layer was laid beneath the entire signal lines.

V. Measurement

Agilent 11974V preselected mm-wave mixer and two spectrum analyzers, E4407B and HP8563E, were used for on-chip measurement of the fabricated circuit. The measurement was conducted in a single-ended configuration. One of the output nodes was terminated with 50 ohm connector and the other node was linked to the measurement equipment. The supply voltage was set to 1.5 V and

the tail transistor was biased to 0.7 V. The circuit, including the buffer, drew 10 mA current, resulting in the DC power consumption of 15 mW.

Fig. 7 shows a typical output spectrum of the fabricated VCO measured with E4407B spectrum analyzer connected with 11974V mixer. The number of iterations to average out the variations over measurements was set to 30 in the measurement. Depicted in Fig. 8 is the variation of the oscillation frequency over the tuning voltage, which was swept from 0 to 2.3 V. Over the tuning range, the oscillation frequency varied from 56.6 to 58.6 GHz, leading to a tuning range of 3.5% and an average K_{VCO} of 870 MHz/V. Output power is presented in Fig. 9 as a function of the tuning voltage, which shows the power range around -20 dBm with no clear dependence on the tuning voltage. Note that the measured output power is directly taken from the single-ended configuration.

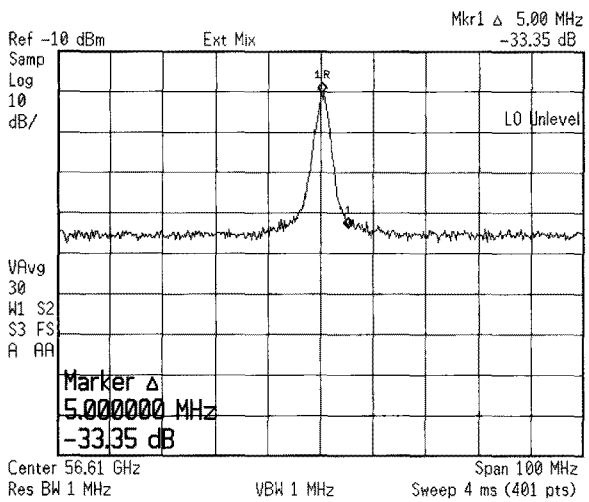

Fig. 7. Measured output spectrum of the VCO.

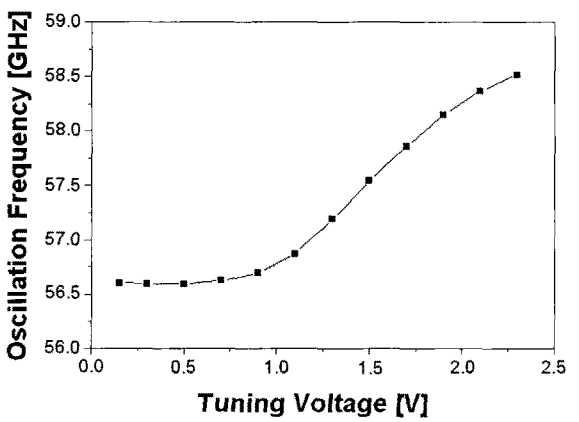

Fig. 8. Measured oscillation frequency versus tuning voltage.

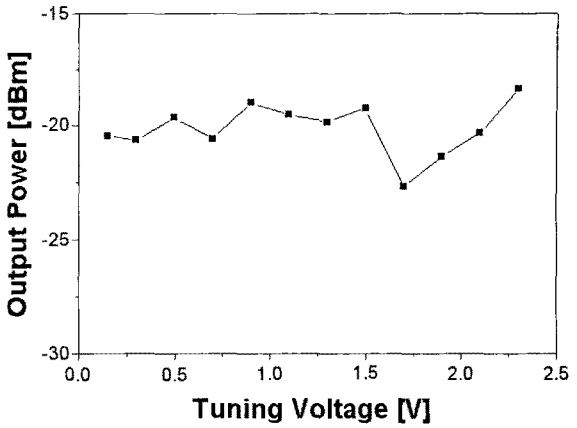

Fig. 9. Measured output power versus tuning voltage.

Accurate measurement of the phase noise in mm-wave band is quite challenging due to the limitation of the equipment. In this work, we employed two different methods for the phase noise measurement and compared the results.

Firstly, the phase noise was estimated by the difference between the spectral power density at the carrier frequency and an appropriate offset frequency, which was 5 MHz in this work. The formula for the phase noise estimation can be expressed as following:

$$L\,[\text{dBc/Hz}] = -\left\{P_{carrier}\,[\text{dB}] - P_{offset}\,[\text{dB}]\right\} - 10\log(RBW), \quad (5)$$

where RBW denotes the resolution bandwidth. Fig. 7 shows the difference of 33.4 dB, which leads to a phase noise of -93.4 dBc/Hz with a RBW of 1 MHz for this particular tuning condition.

Secondly, a direct measurement of the phase noise was carried out by HP8563E spectrum analyzer connected with 11974V mixer. Fig. 10 shows the measurement result, which exhibits the phase noise of approximately -100 dBc/Hz with 10 MHz offset frequency. Considering the typical -6 dB/octave roll-off of the phase noise in the high frequency regime, the two results appear to be consistent to a large extent.

With the consistency confirmed, we proceeded to measure the phase noise over the tuning range based on the first method. As shown in Fig. 11, it does not show a clear trend over the tuning. The FOM is estimated to be -165.5 dBc/Hz based on the formula shown below:

$$FOM = L(\Delta f_{offset}) - 20\log\left(\frac{f_0}{\Delta f_{offset}}\right) + 10\log(P_{DC}). \quad (6)$$

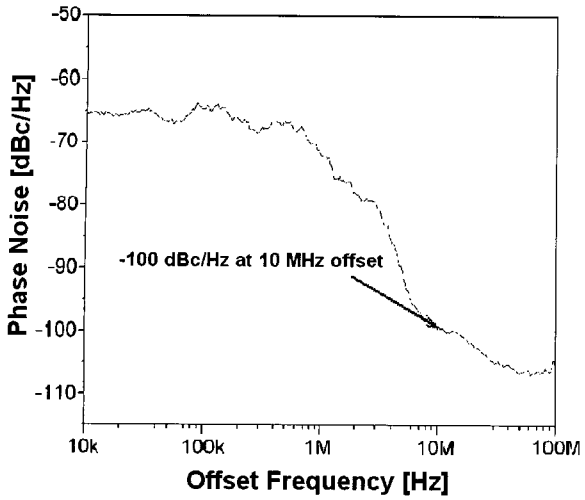

Fig. 10. Measured phase noise with phase noise mode.

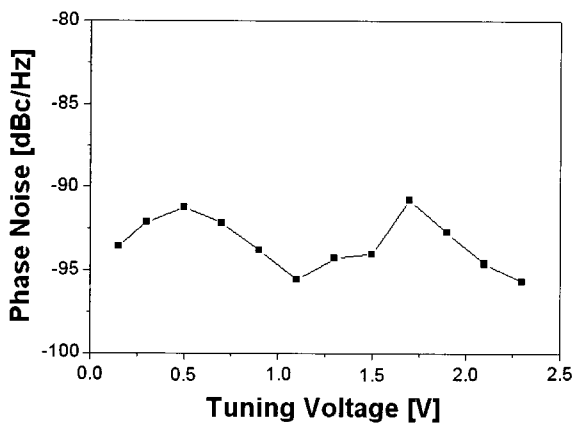

Fig. 11. Phase noise versus tuning voltage.

VI. CONCLUSIONS

A mm-wave LC cross-coupled VCO has been designed and fabricated in a 0.13-μm Si RFCMOS technology. The measured operating frequency of the VCO varied from 56.6 to 58.6 GHz with a tuning voltage from 0 to 2.3 V, leading to a tuning range of 3.5% and an average K_{VCO} of 870 MHz/V. The maximum single-ended output power was -18.3 dBm and minimum phase noise was -96 dBc/Hz at 5 MHz offset frequency. The FOM is estimated to be -165.5 dBc/Hz based on the measurement result. The power consumption of the VCO including buffer was 15 mW with 1.5 V supply voltage. The results show that 60 GHz VCO can be readily implemented in a Si RFCMOS technology with rather relaxed lithography node of 0.13 μm. It is expected that the phase noise can be further improved with proper optimization of the design.

ACKNOWLEDGMENTS

This work was supported partly by IT R&D program of MKE/IITA (2008-F-006-01) and Samsung Electro-Mechanics. The authors would like to thank Dongbu HiTek for chip fabrication.

REFERENCES

[1] J. -S. Rieh, and S. Kim, "Technology and Design Considerations for Millimeter-Wave Circuits," *The 9th International Conference on Solid-State and Integrated-Circuit Technology,* pp. 1352-1356, Beijing, China, Oct. 2008.

[2] S. K. Reynolds, B. A Floyd, U. R. Pfeiffer, T. Beukema, J. Grzyb, V. Haymes, B. Gaucher, and M. Soyuer, "A Silicon 60-GHz Receiver and Transmitter Chipset for Broadband Communications," *IEEE Journal of Solid-State Circuits*, Vol. 41, pp. 2820-2831, Dec. 2006.

[3] S. Pinel, S. Sarkar, P. Sen, B. Perumana, D. Yeh, D. Dawn, and J. Laskar, "A 90 nm CMOS 60GHz Radio," *IEEE Int. Solid-State Circuits Conf Dig. Tech. Paper*, pp. 130-601, Feb. 2008.

[4] B. Afshar, Y. Wang, and A. M. Niknejad, "A Robust 24 mW 60 GHz Receiver in 90 nm Standard CMOS," *IEEE Int. Solid-State Circuits Conf Dig. Tech. Paper,* pp. 182-605, Feb. 2008.

[5] S. Lee, L. Wanger, B. Jangnnathan, S. Csutak, J. Pekaric, N. Zamdmer, M. Breitwisch, R. Ramachandran, and G. Freeman, "Record RF Performance of Sub-45 nm L_{gate} NFETs in Microprocessor SOI CMOS Technologies, " *IEEE Int. Electron Devices Meeting,* pp. 255-258, Dec. 2007.

[6] S. Kim, Y. Oh, and J. -S. Rieh, "Performance Prediction of Deep Sub-nH Inductors for Millimeter-Wave Applications," *2008 Asia-Pacific Workshop on Fundamentals and Applications of Advanced Semiconductor Devices,* pp. 221-226, Sapporo, Japan, July 2008.

[7] N. Kim, S. Lee, and J. -S. Rieh, "A CMOS Millimeter-Wave Cross-Coupled LC VCO for 60 GHz WPAN Application," *IEEK RF Integrated Circuit Technology Workshop,* pp. 397-398, Sept. 2008.

[8] K. Kim, S. Lee, and J. -S. Rieh, "Fast EM Simulation-Based Parasitic Extraction for Quasi-Millimeter-

Wave Circuits," *IEEK RF Integrated Circuit Technology Workshop,* p. 521, Jeju, Korea, Sept. 2007.

Namhyung Kim received his B.S. degree in electronic engineering from Korea University in 2008. He is currently pursuing the M.S. degree in the School of Electrical Engineering, Korea University. His major research interest lies in the design of Si-based mm-wave VCOs and PLLs for high speed wireless communication systems.

Seungyong Lee received his B.S. and M.S. degrees, all in electronic engineering, from Korea University in 2006 and 2008, respectively. His research involved RFCMOS VCO design and substrate noise coupling analysis. In 2008, he joined LG electronics, where he is involved in the development of wireless power transfer systems.

Jae-Sung Rieh received the B.S. and M.S. degrees in electronics engineering from Seoul National University, Seoul, Korea, in 1991 and 1995, respectively, and the Ph.D. degree in electrical engineering from the University of Michigan, Ann Arbor, MI, USA, in 1999.

In 1999, he joined IBM Microelectronics, Essex Junction, VT, USA, where he was involved in the development of 0.18 μm SiGe BiCMOS technology. In 2000, he moved to IBM Semiconductor R & D Center, Hopewell Junction, NY, USA, where he was involved in the research and development activities for 0.13 μm and next generation SiGe BiCMOS technologies. Since 2004, he has been with the School of Electrical Engineering, Korea University, Seoul, Korea, where he is currently an Associate Professor. His major interest lies in the Si-based RF devices and their application to mm-wave and terahertz circuits.

Dr. Rieh is a recipient of 2004 IBM Faculty Award and a co-recipient of 2002 and 2006 IEEE EDS George E. Smith Award. He served as the Conference Chair for 2007 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, and is currently serving as an Associate Editor of the IEEE Microwave and Wireless Components Letters.