Impact of Fin Aspect Ratio on Short-Channel Control and Drivability of Multiple-Gate SOI MOSFET's

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***Abstract*—This paper puts forward an advanced consideration on the design of scaled multiple-gate FET (MuGFET); the aspect ratio ($R_{h/w}$) of the fin height (h) to fin width (w) of MuGFET is considered with the aid of 3-D device simulations. Since any change in the aspect ratio must consider the trade-off between drivability and short-channel effects, it is shown that optimization of the aspect ratio is essential in designing MuGFET's. It is clearly seen that the triple-gate (TG) FET is superior to the conventional FinFET from the viewpoints of drivability and short-channel effects as was to be expected. It can be concluded that the guideline of $w < L/3$, where L is the channel length, is essential to suppress the short-channel effects of TG-FET.**

***Index Terms*—Aspect ratio, FinFET, triple-gate FET, short- channel effects, drivability, subthreshold swing, DIBL, 3-D device simulations**

I. INTRODUCTION

As MOSFET's continue to be aggressively scaled to suppress short-channel effects (SCE's) and advance device performance, the physical limit of conventional scaling is becoming more obvious [1]. In order to overcome this difficulty, the performance of multiple-gate MOSFET's (MuGFET's) is being investigated; for example, FinFET like double-gate (DG) FET's and triple-gate (TG) FET's [2,3] have been extensively studied because it can be expected that mature devices will sufficiently suppress the SCE's and have high drivability [4]. However, these MuGFET devices cause new problems such as the corner effect [5] and switching performance is sensitive to geometrical parameters [6]; the driving current (I_{on}) and SCE's are also significantly influenced by geometrical parameters. A couple of people considered the scaling scheme and impacts on device characteristics [7-9], where the natural length is derived theoretically assuming a very small drain bias except for [9]. Consequently, their results are not always so useful to quantitative consideration on suppression of short-channel effects because bias-dependent SCE's are not taken into account.

Y. Liu et al. discussed the impact of the cross-section (aspect ratio ($R_{h/w}$) of the Si-fin height (h) to fin width (w)) of FinFET's on SCE's [4]. J.-W. Yang and J. G. Fossum compared the performances of double-gate like FinFET's and TG-FET's; they conclude that double-gate like FinFET's are superior to TG-FET's from the viewpoint of area penalty. They described a design guideline for double-gate like FinFET's [10], but not for TG-FET's. However, it is not clear from the viewpoints of various applications and fabrication technology whether FinFET's are actually superior to TG-FET's because the former has many disadvantages with regard to drivability and SCE's as discussed later.

In this paper, we put forward, with the aid of 3-D device simulations, an advanced consideration of FinFET and TG-FET designs; we examine SCE's and the enhancement of I_{on} of FinFET's and TG-FET's against the conventional DG-FET's over a wide range of aspect ratios ($R_{h/w} = h/w$). Engineering the aspect ratio and the trade-off of drivability and SCE suppression are also discussed.

II. DEVICE STRUCTURES AND SIMULATION MODEL

We used Synopsys-*DESSIS* for realizing the 3-D device

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simulations [11]; various device characteristics (drive current (I_{on}), subthreshold swing (*SS*), and buried-insulator-induced barrier lowering (*BIIBL*) [12] were evaluated as functions of $R_{h/w}$. The device structures assumed in these meters are shown in Table 1; here we assume that 5 nm < h < 40 nm and 5 nm < w < 40 nm. These values are extracted from recent published data [3,4] by taking into account plausible process technology; in addition, a low fin manifests the corner effect [5], resulting in enhanced drivability [13]. Fig. 1(a) shows a bird's-eye view of the devices; Fig. 1(b) and Fig. 1(c) show half cross-sectional views of the devices; Figs. 1(b) and 1(c) show half cross-sectional views of the FinFET and TG-FET, respectively. We simulated only one half of each device to reduce the simulation time; d. c. analysis of half of device gives a correct result because the total gate capacitance is simulations are illustrated in Fig. 1, and device para-

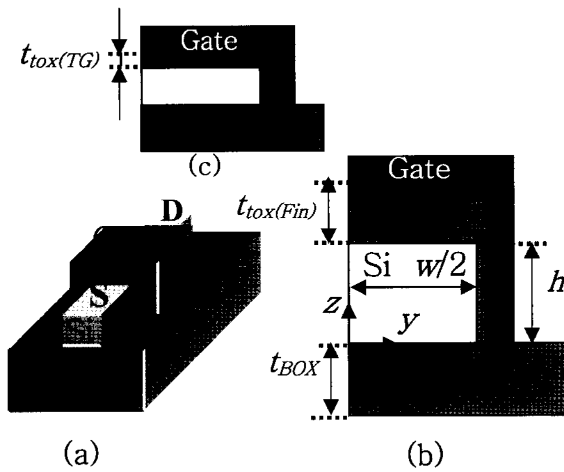

Fig. 1. Schematics of 3-D FET simulated.
(a) Bird's-eye-view of 3-D FET
(b) A half cross-sectional view of FinFET structure
(c) A half cross-sectional view of TG-FET structure

Table 1. Device parameters assumed.

Parameters	Values [unit]
Channel length, L	20, 30, 100 [nm]
Top gate oxide thickness, t_{tox}	2, 40 [nm]
Side gate oxide thickness, t_{sox}	2 [nm]
Buried oxide thickness, t_{BOX}	100 [nm]
Si-fin width, w	5 - 40 [nm]
Si-fin height, h	5 - 40 [nm]
Si-fin doping conc., N_a (p-type)	1×10^{17}–1×10^{15}[cm^{-3}]
Source/drain doping conc., N_d (n-type)	1×10^{20} [cm^{-3}]

meters are shown in Table I; here we assume that 5 nm < h < 40 nm and 5 nm < w < 40 nm. These values are extracted from recent published data [3, 4] by taking into account plausible process technology; in addition, a low fin manifests the corner effect [5], resulting in enhanced drivability [13]. Fig. 1(a) shows a bird's-eye view of the devices; Fig. 1(b) and Fig. 1(c) show half cross-sectional views of the devices; Figs. 1(b) and 1(c) show half cross-sectional views of the FinFET and TG-FET, respectively. We simulated only one half of each device to reduce the simulation time; d. c. analysis of half of device gives a correct result because the total gate capacitance is correctly taken into account on the basis of Gauss law assuming its symmetry, although coupling effect of gate capacitance is not straightforwardly calculated in a. c. analyses of half of device. The top gate oxide thicknesses for the FinFET and TG-FET are 40 nm and 2.0 nm, respectively. The gate length (L_g) is taken as the sum of channel length (L) and twice the 10-nm-long gate-overlap extension region. The silicon body is p-type. Source and drain contacts are put on the top surface of the fin; i.e., the device has no contact on the side surfaces of the fin. Bottom of source and drain diffusions touches the buried oxide layer. Lengths of electrode contact on the S/D diffusion region are 30 nm. This configuration gives the most realistic device structure considering fabrication concerns [14] because we think that the multiple-fin structure is promising for future LSI's, and that this configuration suits to multiple-fin devices [15]. The simulations assume the hydrodynamic transport model because of the very short channel. Since the mobility model significantly influences *I-V* characteristics, we chose the *Masetti Model* [16], *Lombardi Model* [17] and *Hydrodynamic Canali Model* [18] in the simulations [19]. Note that the quantum-effect models aren't included because the Si-fin is wider than 5 nm; distinct quantum effects were ignored because they only slightly influence device characteristics [20,21].

III. RESULTS AND DISCUSSIONS

1. Influence of Aspect Ratio ($R_{h/w}$) on Short-Channel Effects

We pay attention to the short-channel effects of FinFET and TG-FET because the 3-D potential profile is sensitive to the geometrical parameters of the device [22]. Since buried-insulator-induced barrier lowering (*BIIBL*)

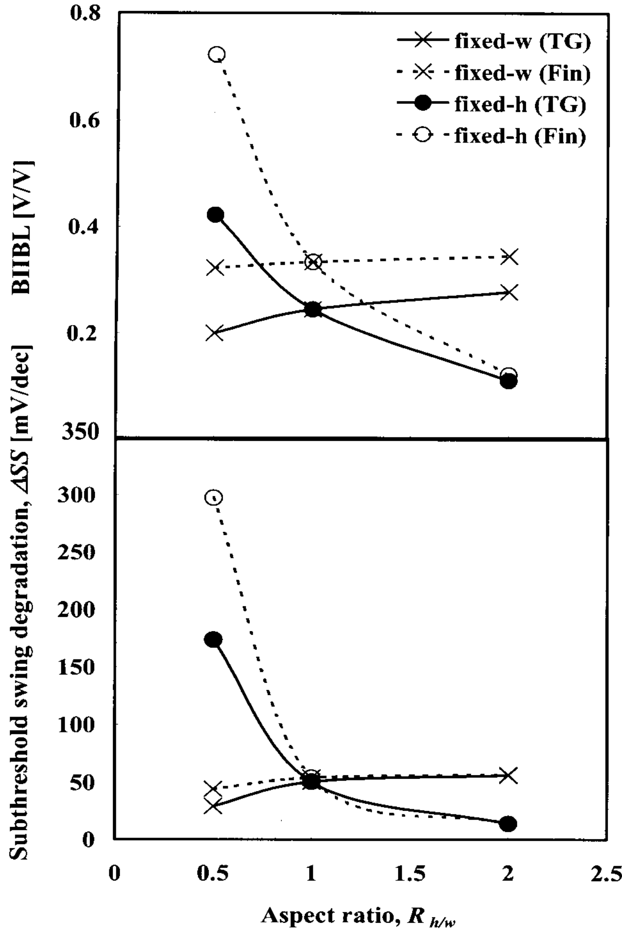

Fig. 2. Aspect ratio dependence of *BIIBL* and subthreshold swing degradation for 30-nm-channel device. *BIIBL* is defined as $|\Delta V_{th}/\Delta V_d|$ (= $|V_{th}(V_d = 1) - V_{th}(V_d = 0.1)|/0.9$). ΔSS is defined as $SS(L = 30$ [nm]$) - SS(L = 100$ [nm]$)$ at Vd= 1 V. It is assumed that $N_a = 1\times10^{17}$ cm^{-3}, the fixed-*h* value is 20 nm and the fixed-*w* value is 20 nm.

plays a significant role in short-channel devices [23,21], we examined the threshold voltage (V_{th}) from the viewpoint of the influence of drain potential, and the subthreshold swing (*SS*) from the viewpoint of geometrical factors.

At first, we discuss the influence of the drain potential on V_{th}. We extract a guideline that suppresses the short-channel effects of threshold voltage (V_{th}) from curves shown in Fig. 2. In Fig. 2, $R_{h/w}$ dependence of *BIIBL* (degradation of V_{th}) is shown for the case of fixed-*h* value (20 nm) or fixed-*w* value (20 nm), where the *BIIBL* is defined as $|\Delta V_{th}/\Delta V_d|$ (= $|V_{th\,(Vd = 1.0\,[V])} - V_{th\,(Vd = 0.1\,[V])}|/0.9$) [24]; we used the above definition of *BIIBL* because the buried-oxide layer is much thicker than the gate oxide layer and *BIIBL* dominates the short-channel effects. It should be noted that the short-channel effects are significantly enhanced as *w* increases when *h* is fixed, while a wide variation of *h* yields little influence on the *BIIBL* value when *w* is fixed. Generally speaking, a large *w* is undesirable in fin-type devices because the *BIIBL* is enhanced [4]. The FinFET shows a stronger *BIIBL* effect than the TG-FET, which indicates that the TG-FET is more suitable in suppressing *BIIBL* as expected. This feature stems from the successful body potential control imposed by the top-gate-induced electric field in the TG-FET. Therefore, we should design TG-FET's to have a large $R_{h/w}$ value when we narrow the fin to suppress *BIIBL* effects. However, narrowing *w* for fixed-*h* has less impact on the *BIIBL* difference between the TG-FET and the FinFET; this occurs when $R_{h/w}$= 2 (*h*= 20 nm and *w*= 10 nm). Here we must consider the technical reality of a "10-nm-wide fin." Such a fin demands great advances in lithography. At present, however, we must select a smaller $R_{h/w}$ value, so we can expect that the TG-FET still has some advantage over the FinFET.

Next, we move on to the influence of geometrical parameters on *SS*. In Fig. 2, $R_{h/w}$ dependence of ΔSS (degradation of *SS*) is shown at two different conditions, where ΔSS is defined as $SS_{(L=30\,nm)} - SS_{(L=100\,nm)}$ at V_d= 1 V. ΔSS is insensitive to $R_{h/w}$ for the fixed-*w* condition, while it rapidly falls as $R_{h/w}$ increases for the fixed-*h* condition. Accordingly, we can readily see that the ΔSS behavior is quite similar to the *BIIBL* behavior shown in Fig. 2; we can see that the fundamental mechanism is the same. By tuning $R_{h/w}$ for the fixed-*h* value, we can realize a very small *BIIBL* value of 0.1 V/V and a very small ΔSS value of 10 mV/dec if we can ignore concerns about technical reality.

For present TG-FET's and FinFET's, $R_{h/w}$=2 is the best solution; this satisfies the condition of $w < L/3$. T. Skotnicki et al. have already shown the guideline of $w<L/3$ for planar devices [1], not for MuGFET devices. To examine the validity of this tentative guideline, we simulated I_{on} and *SS* for the fixed-*w* value of 10 nm as a function of $R_{h/w}$. Simulation results for 30-nm-channel devices are also shown in Fig. 3. These results are useful since they show that *SS* is smaller than 80 mV/dec, and that large I_{on} and small *SS* have a trade-off relation regardless of device structure [15]. The present guideline of $w<L/3$ is very practical in terms of suppressing the standby-power consumption. A couple of the remaining issues faced by the present guideline are considered later.

2. Influence of Aspect Ratio ($R_{h/w}$) on Drivability

Fig. 4 shows I_{on} dependence on aspect ratio ($R_{h/w}$) for the 30-nm-channel FinFET and TG-FET; one group of curves is calculated for fixed-h value of 20 nm and the other group for fixed-w value of 20 nm, where the threshold voltage (V_{th}) is fixed at 0.25 V by changing the work function of the gate electrode. I_{on} is defined as drain current (I_d) at $V_g = V_d = 1.0$ V. In the case of fixed-w value, I_{on} monotonously increases as $R_{h/w}$ increases (h increases) independent of device structure; this is because the increase in h (fin height) yields, straight forwardly, an increase in channel width for both devices. However, we can see that the I_{on} of the TG-FET is higher than that of the FinFET independent of $R_{h/w}$ value; this means that the conductive channel below the top gate contributes to I_{on}. In contrast, I_{on} increases as $R_{h/w}$ falls (increase in w) in the case of fixed-h value of 20 nm for the TG-FET, while I_{on} decreases as $R_{h/w}$ falls (increase in w) in the case of fixed-h value of 20 nm for the FinFET. For the TG-FET, the increase in I_{on} can be readily understood because the conductive channel created below the top gate is widened as w increases. We can see briefly that the behavior of carrier density per unit length (N_{tot}) under the gate of TG-FET is basically similar to the behavior of I_{on} as shown in Fig. 5. For the FinFET, however, the decrease in I_{on} primarily stems from short-channel effects as Fig. 2 suggests, although the threshold voltage increase also contributes to the decrease in I_{on} because of less potential coupling of side gate electrode.

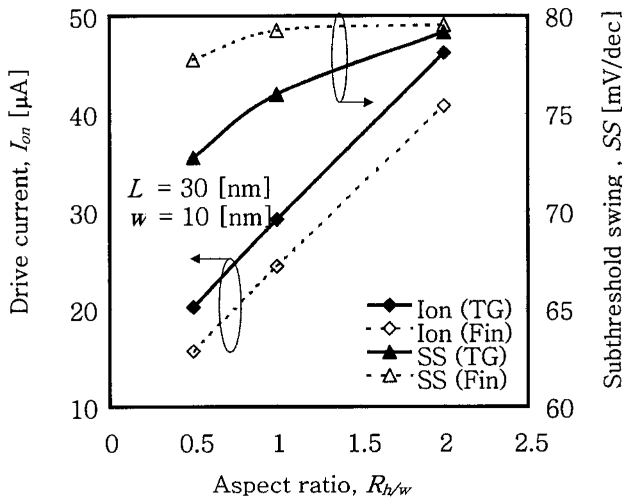

Fig. 3. Aspect ratio dependencies of various characteristics. In the plots of aspect ratio dependencies of drive current and subthreshold swing of 30-nm-channel device, it is assumed that w = 10 nm, V_d = 1 V, and N_a= 1×10^{17} cm^{-3}. Dashed line and solid line denote the simulation result for FinFET and TG-FET, respectively.

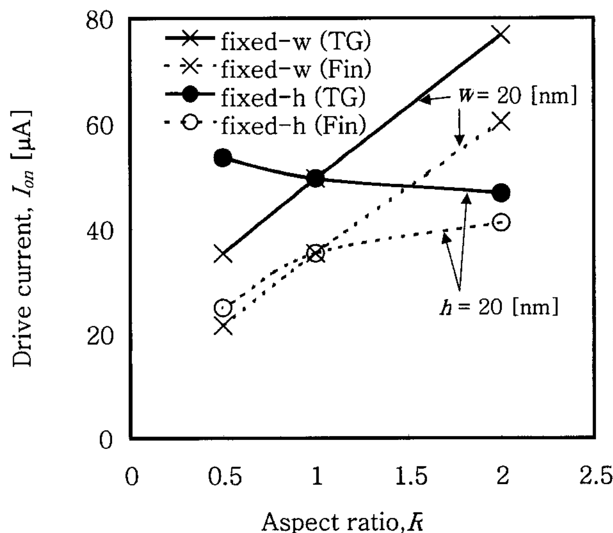

Fig. 4. Aspect ratio dependence of drive current at V_d = 1 [V] for 30-nm-channel device; N_a= 1×10^{17} cm^{-3}. Solid line and dashed line denote the result for TG-FET and FinFET, respectively. Cross symbols and circle symbols denote the result for the fixed-w of 20 nm and the fixed-h of 20 nm, respectively.

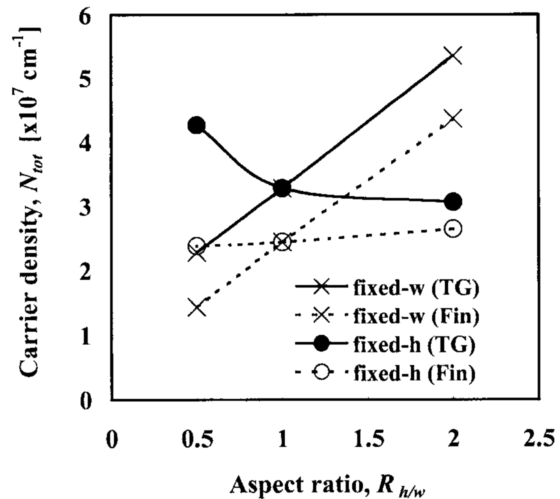

Fig. 5. Aspect ratio dependence of inversion carrier density per length along drain-to-source at V_d = 1[V] for 30-nm-channel device. N_{tot} is defined as the integration of inversion carrier density ($n(y,z)$) over the cross-section of fin near the source junction.

3. Impact of Series Resistance on Drivability

Influence of the contact resistance (R_{con}) and S/D diffusion resistance ($R_{S/D}$) on I_d must be discussed. In addition, silicidation of S/D diffusion must be considered in the future because we must determine the device parameters of TG-FET carefully as described in previous sections.

Reduction of net drain-to-source bias drops due to the S/D diffusion resistance suppresses the *DIIBL* effect stemming from the drain-to-source field through the buried oxide layer. The short-channel effects are also suppressed due to the high S/D resistance since this resistance yields an effective (and negative) substrate bias [15].

Since the gate-overlap region has to be formed along the gate-electrode edge, the diffusion layout plays an important role in multi-fin TG-FET because the multi-fin TG-FET cannot have wrapping metal contact in many cases.

We discus the influence of $R_{S/D}$ and R_{con} on drivability. In the present simulation, $R_{S/D}$ is ranging from 2500 Ω (for h=w=5 nm) to 350 Ω (for h=w=40 nm), while the channel resistance is around 600 Ω. On the other hand, contact resistivity usually ranges from 10^{-7} to 10^{-9} Ω-cm^2 [14]. Here, we assumed the contact resistivity of 10^{-8} Ω-cm^2; the local contact resistance was automatically inserted between metal and diffusion in the simulation. R_{con} that was extracted from simulation results was taken to range from 280 to 1800 Ω for the devices. We can no longer neglect the influence of $R_{S/D}$ and R_{con} on I_{on} in scaled-down devices [26]. However, in the present simulation, the I_{on} value in the saturation condition is reduced by about 30% when finite $R_{S/D}$ and R_{con} are assumed. Therefore, meaning of simulated I_{on} values shown in Figs. 3, 4, 5(b), and 8 would be somewhat poor for a small w value. In addition, reduction of I_{on} means that $V_D/3$ is applied to the total parasitic resistance, and that $V_D/6$ works as an effective substrate bias. When the buried oxide layer is as thin as 100 nm, this effective substrate bias rises the threshold voltage of the device and suppresses SCE's effectively. In this case, the deterioration of subthreshold swing (SS) is suppressed and the design guideline of $w<L/3$ might not be so stringent (see Fig. 9).

We address the silicidation of S/D diffusion briefly. As clearly demonstrated in [14], silicidation process of S/D diffusion requires a wide fin because the full silicidation of fin does not result in the lowest parasitic resistance [25,26]. When we assume the multi-fin TG-FET, we think that a buried silicide layer will be the best solution from the viewpoint of lower contact resistance on the basis of consideration appearing in [25,26].

4. Advantage of TG-FET

Before discussing the advantages of the TG-FET, we show additional simulation results of *BIIBL, ΔSS,* I_{on} and *SS* as functions of body doping concentration (N_a) in Fig. 6; Fig. 6(a) shows the *BIIBL* and *ΔSS* dependencies on N_a, while Fig. 6(b) shows I_{on} and *SS* dependencies on N_a. Here, we assume that L= 30 nm to examine the guideline of w=L/3; the device is fully depleted in the present N_a range. In Fig. 6(a), it is seen that short-channel effects represented by *BIIBL* and *ΔSS* are almost independent of N_a from 10^{15} cm^{-3} to 10^{17} cm^{-3}. It is clearly demonstrated that *BIIBL* and *ΔSS* are primarily ruled by $R_{h/w}$. It can be appreciated that the assumed guideline of $w<L/3$ is appropriate in suppressing short-channel effects. In Fig. 6(b), it is seen that *SS* is almost independent of N_a, while I_{on} is reduced with the increase in N_a. However, the reduction

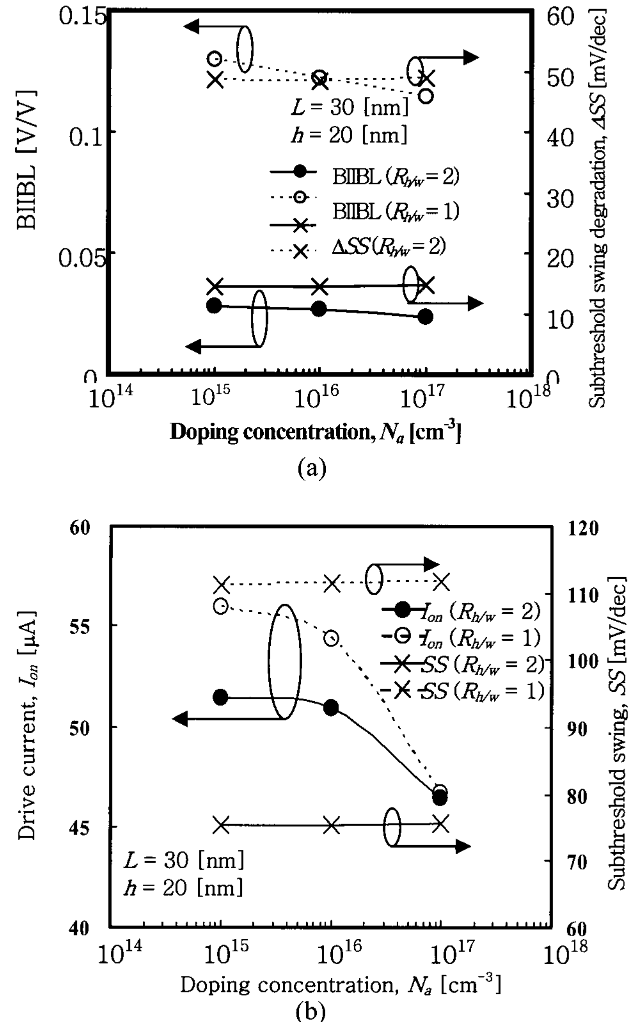

Fig. 6. Device performance dependence on SOI doping concentration for L= 30 nm and h= 20 nm.
(a) *BIIBL* and *ΔSS* dependencies on N_a
(b) I_{on} and *SS* dependencies on N_a

in I_{on} is primarily responsible for the mobility reduction in the high doping range, not for others. It is also clearly demonstrated that I_{on} and SS are primarily ruled by $R_{h/w}$. It can also be appreciated that the assumed guideline of $w<L/3$ is basically appropriate in suppressing short-channel effects.

In order to examine more carefully the advantages of TG-FET, we consider the TG-FET enhancement of I_{on} compared to that of the planar double-gate (p-DG) SOI MOSFET for various $R_{h/w}$ values; simulated enhancement rate of I_{on} is shown as a function of $R_{h/w}$ in Fig. 7 for the fixed-h value of 20 nm and the fixed-w value of 20 nm, where the device parameters of TG-FET are identical to those of p-DG SOI MOSFET except for the top gate oxide thickness (t_{tox}). The enhancement rate is defined by $(I_{on(TG)}-I_{on(p-DG)})/I_{on(p-DG)}$, where $I_{on(p-DG)}$ is extracted from 2-D simulations of the p-DG SOI MOSFET. The enhancement rate increases as $R_{h/w}$ decreases, although the enhancement rate is larger with fixed-h value than that with fixed-w value for all $R_{h/w}$ values. These behaviors are attributed primarily to the short-channel effects, and secondarily to the contribution of the effective top-gate width. The first mechanism is significant in the case of fixed-h value. The smaller the value of $R_{h/w}$ is, the more significant the influence of the short-channel effects becomes; namely, a TG-FET with large w value suffers from the *BIIBL* effect stemming from a weak carrier-confinement field near the buried-oxide layer as was discussed previously. The second mechanism is dominant at large $R_{h/w}$ for fixed-h value because the side-gate electrode can control almost entirely the body potential. In other words, the 3-D advantage of the TG-FET, i. e. utilizing the increase in gate width, is mostly lost, while the corner effect still remains and contributes to the enhancement of I_{on} as discussed in [13], where we already demonstrated that the corner effect yields a drivability enhancement of FinFET. However, it should be also mentioned that the drivability enhancement of FinFET results in the performance trade-off due to SCE's; the trade-off is more crucial than TG-FET because of thick top gate oxide layer of FinFET.

As mentioned above, the enhancement rate for fixed-h is larger than that for fixed-w. Under the present condition of fixed-w, the w value does not satisfy the condition of $w<L/3$; the carrier density (N_{tot}) in the fin is lower than that in the present condition of fixed-h because of short channel effects and the enhancement rate is smaller than is true for fixed-h (not shown here). As a result, it can be concluded that a narrow and high fin is recommended for realizing high performance TG-FET's because the short-channel effects are sufficiently suppressed, although a large enhancement in I_d cannot be expected because the contribution provided by corner effect becomes relatively minor [13].

5. On Design Guideline of TG-FET's and FinFET's

The short-channel effect is still one of the more serious problems in short-channel MuGFET's. It can be concluded that $R_{h/w}$ should be large (i.e., w should be small) when h value is fixed so as to achieve the condition of $w< L/3$. It should be noted that the apparent enhancement of I_{on} appearing in Fig. 7 for $R_{h/w} < 1$ is primarily attributed to short-channel effects; the meaningful enhancement rate of I_{on} that we can expect from TG-FET's is at most 20%. In addition, short-channel effects don't seem to be sensitive to $R_{h/w}$ (or h value) for fixed w in Figs. 2 and 3. However, it should be noted that the condition of $w<L/3$ is not satisfied in the range of $R_{h/w}$ examined here. This means that when designing 30-nm-channel FinFET's or TG-FET's with suppressed short-channel effects for a certain fixed-w value, we must reduce the fin width w to 10 nm, although the parasitic resistance must be reduced.

We also investigated the design feasibility of the 20-nm-channel TG-FET. Figures 8 and 9 show fin width (w) dependence of I_{on} and SS with the parameter of fin height (h), respectively. The dashed line in both figures indicates the condition of $w = L/3$. It is clearly seen from Fig. 8 that I_{on} rapidly increases as h increases, independent of w. This can be understood as an increase in channel width that was mentioned previously; here, it is useful to state that I_{on} is not simply proportional to h because the corner effect plays an important role [13]. On the other hand, we cannot expect a significant enhancement of I_{on} when $w$increases; we can see that the increase in w yields a slight increase in I_{on} in low fin devices because of the increase in effective channel width, and that the increase in w yields a decrease in I_{on} because of the short-channel effects. In Fig. 9, the shaded region indicates that SS values are under 80mV/dec.; that is, the region suggests that the standby leakage current would be sufficiently suppressed. When $w = L/3$, SS of 20-nm-channel devices is about 80 mV/dec. independent of h. This means that the present guideline can also be applied to the design of sub-20-nm-channel

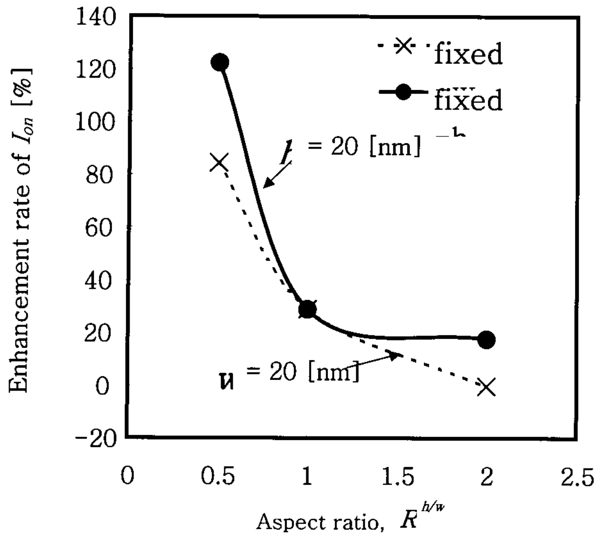

Fig. 7. Aspect ratio dependence of the enhancement rate of I_{on} of TG-FET compared to that of 2-D planar DG SOI MOSFET. It is assumed that the devices have 30-nm channels with N_a= 1x10^{17} cm^{-3}, and that I_{on} is calculated at V_g = V_d = 1 [V]. Dashed line and solid line denote the results for the fixed-w of 20 nm and the fixed-h of 20 nm, respectively.

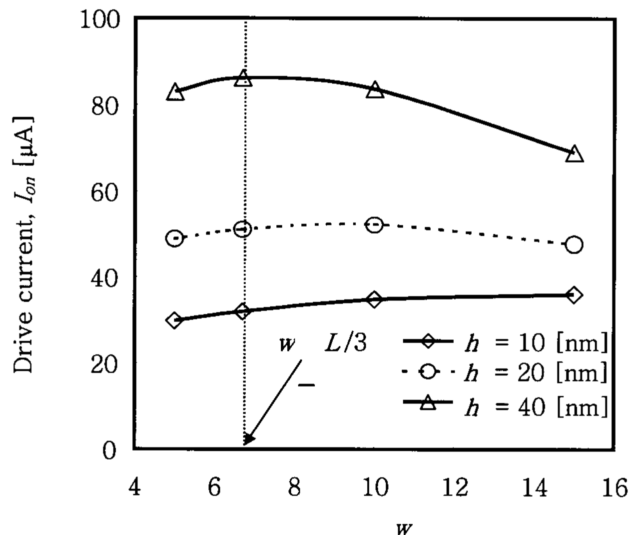

Fig. 8. Fin width dependence of drive current at V_g = V_d = 1 [V] for 20-nm-channel TG-FET with parameter of fin height; N$_a$= 1x10^{17} cm^{-3}. Symbols of open diamond, open circle and open triangle are the results for h = 10, 20, and 40 [nm], respectively. The dotted line indicates the condition of w = L/3.

devices in a similar manner. It is worthwhile nothing that SS remains small independent of h when $w<L/3$ is satisfied. Desired value of I_{on} should be set by changing h value. Here, as suggested in the previous section, we must take account of impact of the parasitic resistance on suppression of SCE's. When this effect is taken into account, it is suggested that the present guideline of $w<L/3$ is

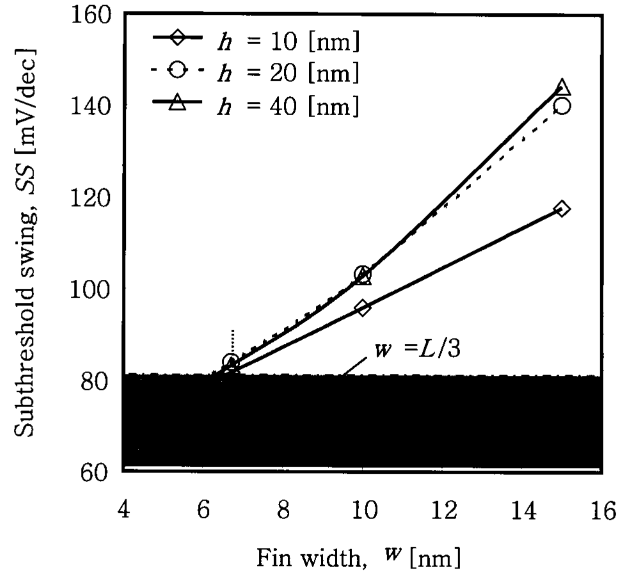

Fig. 9. Fin width dependence of subthreshold swing at V_d = 1 [V] for 20-nm-channel TG-FET as a parameter of fin height; N$_a$= 1x10^{17} cm^{-3}. Symbols of open square, open circle and open triangle are the results for h = 10, 20, and 40 [nm], respectively. The dotted line indicates the condition of w = L/3. The shaded region satisfies the condition of SS < 80 mV/dec.

sufficiently robust in determining the device parameters.

IV. Conclusions

In this paper, we studied, with the aid of 3-D device simulations, how the geometric condition of the fin body influenced the drivability and short-channel effects of MuGFET's. We successfully extracted a key design guideline for MuGFET's.

In order to realize MuGFET's with high drivability, we must use a TG-FET having a large $R_{h/w}$ and a small w because this combination also well suppresses the short-channel effects. This primary guideline is correct if the condition of $w<L/3$ is satisfied. When we need a high I_{on} with sufficient suppression of SCE's, a narrow, high-fin device should be used, which means that the proposed guideline is automatically satisfied. In addition, it has been demonstrated that the proposed guideline is valid over a wide range of $R_{h/w}$.

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