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Analysis, Design, Modeling, Simulation and Development of Single-Switch AC-DC Converters for Power Factor and Efficiency Improvement

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ABSTRACT

This paper addresses several issues concerning the analysis, design, modeling, simulation and development of single-phase, single-switch, power factor corrected AC-DC high frequency switching converter topologies with transformer isolation. A detailed analysis and design is presented for single-switch topologies, namely forward buck, flyback, Cuk, Sepic and Zeta buck-boost converters, with high frequency isolation for discontinuous conduction modes (DCM) of operation. With an awareness of modern design trends towards improved performance, these switching converters are designed for low power rating and low output voltage, typically 20.25W with 13.5V in DCM operation. Laboratory prototypes of the proposed single-switch converters in DCM operation are developed and test results are presented to validate the proposed design and developed model of the system.

Keywords: Single-Switch Forward, Flyback, Cuk, Sepic and Zeta Converter, Power Factor Correction, Power quality improvement, Efficiency, Output Voltage Ripple

1. Introduction

Single ended converters, such as the forward, flyback, Cuk, Sepic, Zeta and others, are often chosen for implementing simple low cost and low power converters. The use of only one switch and the relatively simple control circuit required are strong reasons for their choice^[1]. The discontinuous mode operation (DCM) of all single-switch topologies is most suitable for low power applications, where these converters present excellent characteristics of power factor correction using a very

simple control scheme with only one voltage feedback loop^[2].

The conventional single-phase diode rectifier draws pulsating current due to the direct connection of the diode to an electrolytic capacitor. The amount of line current distortion produced by the single low power converter is minimal. However, a large number of electronic devices generate a large amount of current distortion, and this results in environmental pollution such as electromagnetic interference. For consumer electronics and other similar equipment with relatively low power, less than a hundred watts, a solution to suppress its input current distortion, i.e. to improve its power factor, is required. Therefore, a simple-structure PFC converter is desirable. On the other hand, sufficient suppression of the output-voltage ripple

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and high power efficiency are also required [3]-[6]. Power quality has become an important consideration when designing any converter. As a result, more attention has been given to the design of converters with good power factor correction (PFC), reduced input harmonics and better efficiency [7]-[9]. The aim is to produce a converter that draws sinusoidal input current while providing well regulated output voltage at the required power rating. A variety of converter topologies and implementations to achieve this aim have been reported in the literature [10]-[12].

There are numerous applications which need power conditioning, such as battery charging, DC power supplies, office equipment and household applications. In this paper, analysis, design, modeling, simulation and development of single-phase single-switch AC-DC flyback, Cuk, Sepic, Zeta buck-boost and forward buck converters in DCM are carried out for power factor correction and efficiency improvement. For wave shaping in single-phase single-switch AC-DC converters different techniques are used with various combinations of inductors and capacitors. The simulated results have also been verified experimentally.

2. Circuit and Operation

Fig.1 shows the block diagram of a single-phase AC-DC converter with power correction in DCM operation. As shown in Fig.1, discontinuous conduction mode (DCM) uses a very simple control feedback, which only requires output voltage sensing. The bridge rectifier is used at the input AC side with a power factor corrector using an inductor and capacitor combination. Now, a small value of output voltage, compared to the reference value and resulting value, passes through the output voltage controller G(s), which generates the PWM output and is used for switching the converter. It has inherent power factor correction characteristics with constant duty ratio and switching frequency, offering an attractive solution for lower power applications.

The output voltage regulation is provided by the feedback loop as shown in Fig.2, where the output sensed voltage V_o is compared with a reference V_{oref} value and the error is amplified in a proportional integral (PI) controller which is compared with a saw-tooth ramp V_s , thus providing the pulse to power switch. Therefore, this

circuit is controlled by the difference in the on- time interval and the constant switching frequency f_s .

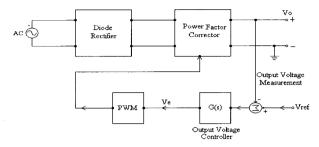


Fig. 1 Block diagram of single phase AC-DC converter with power factor correction and feedback control in DCM operation

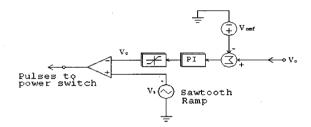


Fig. 2 Practical voltage follower approach for PWM control

3. Design Equation for Single-Phase, Single-Switch AC-DC Converters

The different parts of all single-switch converter systems are modeled using basic equations and all equations are summarized in Table 1.

Table 1 Basic equations for single switch AC-DC converters

	Forward	Flyback	Cuk	SEPIC	Zeta
Voltage ratio,V _o /V _{in}	$\frac{N_2}{N_1}D$	$\frac{N_2}{N_1} \frac{D}{(1-D)}$	$\frac{N_2}{N_1} \frac{D}{(1-D)}$	$\frac{N_{2}}{N_{1}}\frac{D}{(1-D)}$	$\frac{N_1}{N_1}\frac{D}{(1-D)}$
Critical inductance L _{cr}	Rr(1-D) 2fs	$\frac{R}{46\left(\frac{N}{N} + \frac{V_0}{V_0}\right)^2}$	$\frac{R}{46(\frac{N}{N} + \frac{V_0}{V_0})}$	$\frac{V_{\text{in(min)}}}{\Box I_{L}f_{s}}D$	$\frac{\mathbf{R}_{\mathbf{i}}(1-\mathbf{D})^2}{2\mathbf{f}_{\mathbf{s}}}$
Min. output capacitorC _o	(1-D) 8Lf² (□V√	$\frac{V_o}{r_v f_s R_L}$	$\frac{V_o}{r_v L \omega_L R_L}$	$\frac{1}{\mathrm{kf_sRL}}$	$\frac{V_{o}}{\omega r_{v}R_{L}}$
Voltage stress of switch, V _{sw}	$\frac{2V_{\rm in}}{(1-D)}$	$\frac{V_{in}}{(1-D)}$	V _{in} +V _o	V _{in} +V _o	$V_{in} + V_{o}$
Voltage stress of switch, V _D	$\frac{V_{o}}{(1-D)}$	$\frac{V_o}{D}$	$V_{in} + V_o$	$V_{in}+V_{o}$	V _{in} +V
Coupling voltage,V _{cp}	NA	NA	$V_{in}+V_{o}$	Vin	$V_{in}+V_{in}$

where N_1 and N_2 are the primary and secondary turns of the transformer, D is the duty ratio, f_s is the switching frequency, r_v is the peak to peak output voltage ripple, and V_o and V_{in} are output and input voltage, respectively.

4. Modeling and Simulation

The importance of simulation is apparent for the preliminary design of any system. System behavior and performance can be predicted with the help of the simulation. To verify and investigate the design and performance of the preliminary stage, a simulation study of all converters is performed in DCM operation for input AC voltage 220V at 50 Hz and output DC voltage of 13.5V and 20.25W output power rating using the PSIM6.0 platform. Figs.3-7 show the PSIM models of forward, flyback, Cuk, Sepic and Zeta converters in DCM operation. Simulation results show high quality steady state performance from 20% to 100% loading conditions with good power factor and efficiency. In order to demonstrate all converters performance in DCM operation, the design parameters and simulation results are summarized in Table 2 and Table 3, respectively. In order to observe the circuit performance at lower as well as at higher loads, simulation studies are divided into four categories:

- a) Steady state operation with 100% load.
- b) Steady state operation with 50% load
- c) Steady state operation with 20% load
- d) Sudden application and removal of load

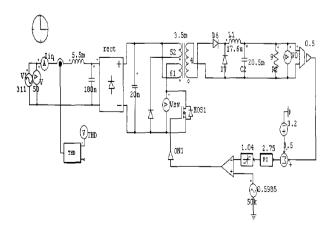


Fig. 3 PSIM model of single switch forward converter in DCM

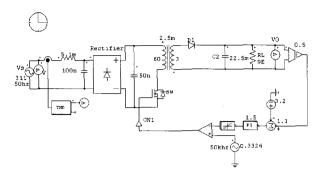


Fig. 4 PSIM model of single switch flyback converter in DCM

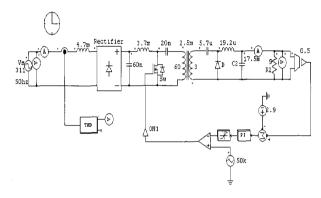


Fig. 5 PSIM model of single switch cuk converter in DCM

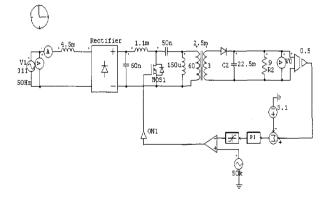


Fig. 6 PSIM model of single switch SEPIC converter in DCM

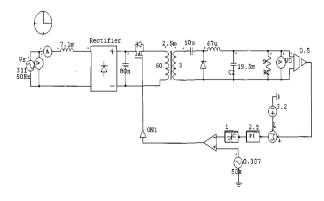


Fig. 7 PSIM model of single switch zeta converter in DCM

Table 2 Design parameters of single-phase, single switch AC-DC converters in DCM operation

	Forw.	Fly.	Cuk	Sepic	Zeta
Transformer					
Turn ratio (n)	15	20	20	20	20
Magnetizing					
Inductance (mH)	3.5	2.5	2.5	2.5	2.5
Input					
Inductor (mH)	5.5	5.1	4.7	4.5	7.1
Output					
Inductor (µH)	17.6	-	19.2	_	67
Output					
Capacitor (mF)	20.5	22.5	17.5	22.5	19.5

Table 3 Simulation results of single-phase, single switch AC-DC converters in DCM operation

0	20% Load	50% Load	100%Load		
Quantity	Forward Converter				
InputCurrent THD	14.8%	13.1%	12.2%		
PF	0.965	0.971	0.982		
Output Ripple	0.5%	0.9%	1.2%		
Efficiency	78.5%	80.1%	82.4%		
	Flyback Converter				
Input Current THD	5.8%	5.1%	4.8%		
PF	0.977	0.981	0.992		
Output Ripple	0.4%	0.8%	1.1%		
Efficiency	78.5%	80.0%	80.8%		
	Cuk Converter				
Input Current THD	5.3%	5.0%	4.5%		
PF	0.979	0.984	0.993		
Output Ripple	0.5%	0.9%	1.2%		
Efficiency	78.1%	79.0%	79.9%		
	Sepic Converter				
Input Current THD	5.1%	4.6%	4.1%		
PF	0.981	0.987	0.993		
Output Ripple	0.4%	0.7%	1.0%		
Efficiency	78.3%	79.7%	80.9%		
	Zeta Converter				
Input Current THD	5.1%	4.6%	4.0%		
PF	0.981	0.989	0.996		
Output Ripple	0.3%	0.7%	0.9%		
Efficiency	78.3%	79.2%	81.1%		

5. Prototypes Developments

The prototypes for single-switch converters are developed for a power rating of 20.25W with 13.5V output voltage at 50kHz switching frequency in DCM operation using PWM controller IC UC3843 approaching

a power factor of 0.99, efficiency more than 80%, less than 1% output voltage peak to peak ripple and less source current harmonic distortion at full load. These converters have been tested for 10% to 120% loading conditions and input supply variation from 100V to 260V. Use of an EMI filter is also tested and demonstrated by conducting tests with and without an EMI filter. The input and isolated output ground is designed using optocoupler IC 4N35 and performance improvement is confirmed by different experimental tests. The power quality observations for all single-switch converters are summarized in Table 4, which shows the comparison between simulation and experimental results at 20% and 100% load. Experimental results are observed to be in good agreement with simulation results. Fig. 8 shows the photograph of a forward converter which is one out of the five single-switch converters.

Table 4 Power quality observation of Forward, Flyback, Cuk, Sepic and Zeta single- switch AC-DC converter

	F		Cimer	lation
	Experimental		Simulation	
-10-1011	Results		Results	
	Output Power		Output Power	
Quantity	4W	20.25W	4W	20.25W
	Forward Converter			
Source Current THD (%)	14.2	12.1	14.8	12.2
Power Factor	0.97	0.986	0.965	0.982
Output Voltage Ripple	0.3	1.0	0.5	1.2
Efficiency (%)	78.7	82.6	78.5	82.4
		Flyback	Converter	
Source Current THD (%)	7.4	6.5	5.8	4.8
Power Factor	0.98	0.996	0.977	0.992
Output Voltage Ripple	0.3	0.9	0.4	1.1
Efficiency (%)	78.8	81.1	78.5	80.8
	Cuk Converter			
Source Current THD (%)	8.3	7.9	5.3	4.5
Power Factor	0.98	0.995	0.984	0.993
Output Voltage Ripple	0.5	1.0	0.5	1.2
Efficiency (%)	78.2	79.9	78.1	79.9
	Sepic Converter			
Source Current THD (%)	8.1	7.4	5.1	4.1
Power Factor	0.98	0.995	0.981	0.993
Output Voltage Ripple	0.4	1.0	0.4	1.0
Efficiency (%)	79.5	80.5	79.7	80.9
	Zeta Converter			
Source Current THD (%)	8.3	7.4	5.1	4.0
Power Factor	0.98	0.995	0.981	0.996
Output Voltage Ripple	0.5	1.1	0.3	0.9
Efficiency (%)	78.8	80.7	78.3	81.1

The full wave rectifier (FWR) has been designed using the diode 1N5408 from General semiconductor having maximum operating voltage 1000V and maximum forward current 1A. For transformer and inductor design the EE25 and EE20 ferrite core of N67 material have been selected, respectively, from EPCOS. The N channel MOSFET, 2SK962 having maximum drain to source voltage 900V and maximum drain current 3A from the International Rectifier has been selected as the switch in all converters.

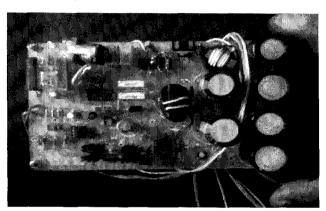


Fig. 8 Photograph of single switch forward converter in DCM

6. Tests and Results

Fig. 9 shows the simulated source voltage and current waveform of the forward buck converter at 100% load in DCM operation. The simulated output voltage waveform with 1.2% peak-to-peak voltage ripple at 100% load for the forward converter is shown in Fig.10. The simulation waveforms for the flyback converters in DCM operation are shown in Figs 11-12. Fig 11 shows the source voltage and current waveforms at 100% load in DCM operation, where the power factor obtained more than 0.99. A THD of less than 5% and an efficiency of more than 80% at 100% load or 20.25W output power is obtained by this converter. The regulated output voltage in DCM operation is shown in Fig.12 at 100% load. The source voltage and current waveform for the Cuk converter at 100% load is shown in Fig.13 for DCM operation. The output voltage of the Cuk converter is shown in Fig.14, where a maximum 1.2% ripple is measured for DCM operation. Fig.15 shows the source voltage and current waveform for the Sepic converter at full load; here THD of the input current is observed at 4.1% and PF is around 0.993, which is very high. The enlarged view of the output voltage at 100% load in DCM is shown in Fig.16 and ripple is observed at 1.0% which is less than the Forward, Flyback and Cuk converters. Last, the simulation results of the Zeta converter are shown in Figs.17-18, where Fig.17 shows the source voltage and current waveform at 100% load and the output voltage waveform is shown in Fig.18 for DCM operation. The output voltage ripple for the Zeta buckboost converter is measured at 0.9% which is better than other converters.

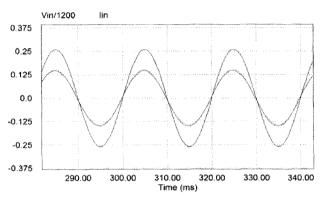


Fig. 9 Source voltage and current of Forward converter in DCM at 100% load

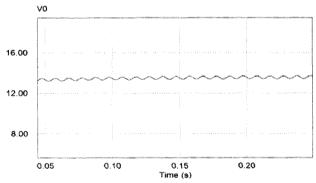


Fig. 10 Steady state output voltage of Forward converter in DCM at 100% load

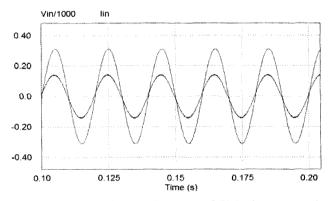


Fig. 11 Source voltage and current of Flyback converter in DCM at 100% load

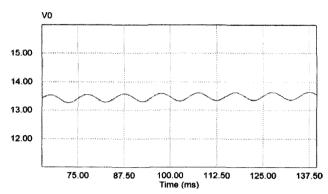


Fig. 12 Steady state output voltage of Flyback converter in DCM at 100% load

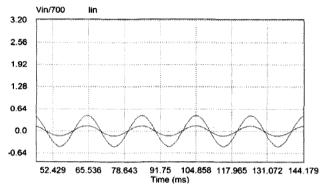


Fig. 13 Source voltage and current of Cuk converter in DCM at 100% load

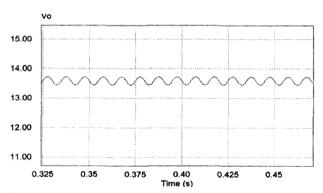


Fig. 14 Steady state output voltage of Cuk converter in DCM at 100% load

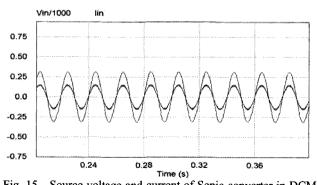


Fig. 15 Source voltage and current of Sepic converter in DCM at 100% load

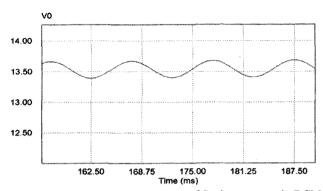


Fig. 16 Steady state output voltage of Sepic converter in DCM at 100% load

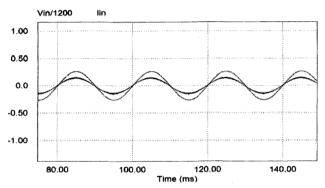


Fig. 17 Source voltage and current of Zeta converter in DCM at 100% load

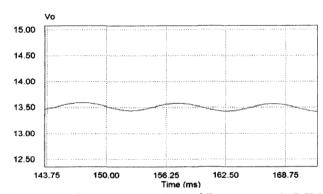


Fig. 18 Steady state output voltage of Zeta converter in DCM at 100% load

The prototypes of all five single-switch converters in DCM operation have been implemented in the laboratory to verify the simulation results. Fig.19 shows the source voltage and current waveform for the forward converter in DCM. The output voltage waveform is shown in Fig.20 and the output voltage ripple is observed at 135mV or 1% and efficiency of 82.6% for the single-switch Forward converter in DCM operation. The flyback converter is implemented in DCM operation. The source voltage and current at 100% load is shown in Fig.21 and an improved

power factor of 0.996 is observed for the single- switch flyback converter. The enlarged view of the output voltage and current waveform with 0.9% output voltage ripple is shown in Fig.22 for the flyback converter in DCM operation.

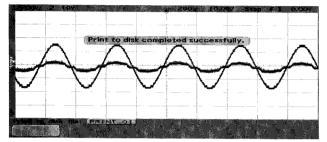


Fig. 19 Source voltage and current of Forward converter in DCM at 20.25W, Scales: 200V/div, 0.5A/div and 5ms/div

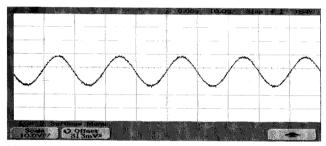


Fig. 20 Output voltage of Forward converter in DCM at 20.25W, Scales: 10V/div and 5ms/div

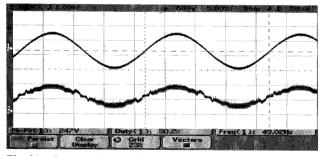


Fig. 21 Source voltage and current of Flyback converter in DCM at 20.25W, Scales: 200V/div, 0.5A/div and 5ms/div

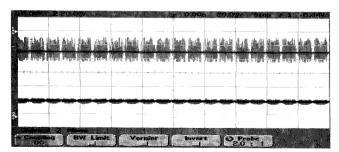


Fig. 22 Enlarged view of output voltage, output current of flyback converter in DCM, Scales: 2V/div, 0.2A/div and 5ms/div

Figs.23-28 shows the experimental results of the single-phase, single-switch Cuk, Sepic and Zeta converters in DCM operation. Fig.23 shows the source voltage and current waveforms at 100% load for the Cuk converter. The output voltage and current waveform for the Cuk converter is shown in Fig.24. The source voltage and current waveform for the Sepic converter in DCM is shown in Fig.25 at 100% load.

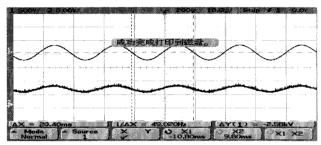


Fig. 23 Source voltage and current of Cuk converter in DCM at 20.25W, Scales: 200V/div, 0.5A/div and 5ms/div

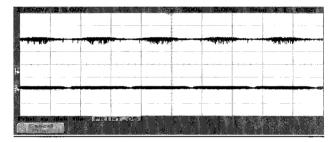


Fig. 24 Output voltage, output current of Cuk converter in DCM at 20.25W, Scales: 5V/div, 0.5A/div and 5ms/div

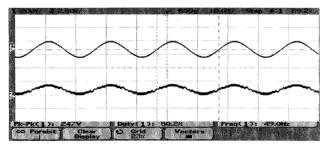


Fig. 25 Source voltage and current of Sepic converter in DCM at 20.25W, Scales: 200V/div, 0.5A/div and 5ms/div

The output voltage and current waveform for 13.5V output is shown in Fig.26 for the single-switch Sepic converter in DCM operation at 100% load. Last, the Zeta converter prototype has been tested, where source voltage and current waveforms at 100% load are shown in Fig.27 in DCM operation. The Zeta converter shows a power factor of 0.95, source current THD of 7.4% and efficiency

of 80.7% for DCM operation at 100% load. The output voltage ripple is observed at 1.1% for the Zeta converter in DCM operation which is shown in Fig.28 along with the output current waveform.

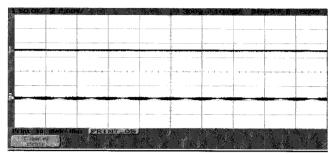


Fig. 26 Output voltage, output current of Sepic converter in DCM at 20.25W, Scales: 5V/div, 0.5A/div and 6ms/div

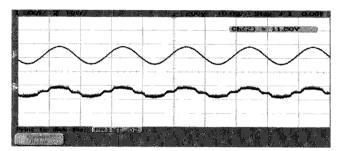


Fig. 27 Source voltage and current of Zeta converter in DCM at 20.25W, Scales: 200V/div, 0.5A/div and 5ms/div

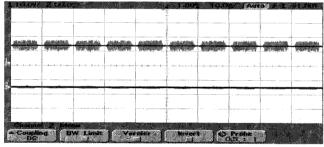


Fig. 28 Output voltage, output current of Zeta converter in DCM at 20.25W, Scales: 5V/div, 0.5A/div and 6ms/div

7. Conclusions

In this paper analysis, design, modeling, simulation and development of single-switch converters are carried out in DCM operation for 13.5V, 20.25W output. High power quality is obtained with design parameters with PF on the order of 0.99 and efficiency more than 80%. The flyback, Cuk, Sepic and Zeta converters show close to unity power factor at full load with more than 80% efficiency and very

low output voltage ripple, which is observed close to 1%. On the other hand, the forward converter shows very good efficiency, which comes out to 82.6% and output voltage ripple, which is observed at 1.2%. So, depending on the requirements we can choose a converter for low power applications, but little compromise between efficiency, THD and Power Factor (PF) is required.

References

- [1] C. A. Canesin, L. Barbi, "A unity power factor multiple isolated outputs switching mode power supply using a single switch," in Proc IEEE APEC'97, vol.2, Nov.1997, pp. 866-871.
- [2] Kin- siu Fung, Wing- Hung Ki and Philip K. T. Mok, "Analysis and Measurement of DCM Power Factor Correctors," in Proc. IEEE Power Electronics Specialists Conference, 1999, pp.709-714.
- [3] F.S Dos Reis, J. Sebastian and J. Uceda, "characterization of Conducted Noise Generation for Sepic, Cuk and Boost Converters Working as Power Factor Preregulators," in Proc. IEEE IECON'93, 1993, pp. 965- 970.
- [4] Buso S., Spiazzi G., and Tagliavia, "Simplified Control Technique For High-Power Factor Fly Back Cuk And Sepic Rectifier Operating In CCM," in Proc. IEEE Conference on Industry Application 1999, vol.3, Oct.1999 pp. 1633-1638.
- [5] Bhim Singh, B.N.Singh, Ambrish Chandra, Kamal Al-Haddad, Ashish Pandey and Dwarka P. Kothari, "A review of single-phase improved power quality ac-dc converters," IEEE Trans. On Industrial Electronics, vol.50, no.5, pp.962-981, Oct. 2003.
- [6] K.H. LIU and Y.L LIN "Current Waveform Distortion In Power Factor Correction Circuit Employing iscontinuous Mode Boost Converter," IEEE PESC 1989, PP.828-829.
- [7] M.T. Madigan, R.W. Erickson and E.H. Ismail, "Integrated High-Quality Rectifier Regulators," IEEE Trans. on Indus. Electro., vol. 46, 1999, pp. 749-758.
- [8] G.C. Hsieh J. F. Tsai, M. Fu Lai and J.C. Li, "Design of power factor corrector for the off line isolated buck/boost converter by a voltage follower technique," in Proc. IEEE IECON'93, 1993, pp. 959-964.
- [9] J.S. Glaser and A. F. Witulski, "design issues for high power factor ac-dc converters systems" in Proc. IEEE PESC'95, 1995, pp.542-548.
- [10] Y. Jiang, and F.C. Lee, "Single-Stage Single-Phase parallel power factor correction scheme," in Proc. IEEE PESC'94, 1994, pp. 1145-1151.
- [11] D. Balocco, E. Derory, D. Ploquin and C. Zardini, "A new

single stage isolated power factor preregulator for avionics distributed power supply systems" in Proc. IEEE PESC'96, June 1996, pp.1717-1723.

[12] T.F. Wu and Y.K. Chen, "Analysis and design of an isolated single-stage converter achieving power-factor correction and fast regulation," IEEE Trans. Industrial Electron., vol. 46, pp. 759-767, August 1999.



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