

Design of LTPS TFT Current Mode Multiplexer and MUX-based Logic Gates

Ju Young Jeong* **and Moon-Pyo Hong****

Abstract

With the aim of creating a high-quality display system with value-added functions, we designed a current mode multiplexer for LTPS TFT devices. The multiplexers had less than 1 volt logic swing, and speed improvement was evident compared with that of conventional CMOS architecture. We refined the multiplexer to achieve a more stable current steering operation. By using the versatility of the multiplexer, a new NAND/AND and NOR/OR logic gates were designed through the simple modification of signal connections. Two micron LTPS TFT parameters were used during the HSPICE simulation of the circuits.

Keywords : LTPS, TFT, SOP, current-mode, multiplexer

1. Introduction

Low-temperature poly-silicon (LTPS) thin film quality has been consistently improved, enabling thin film transistors (TFTs) to be used in a wide variety of logic circuits [1]. However, material quality could not match that of the single crystal silicon, and the process technology requires further refinement. As a result, devices using TFT circuitry tend to be larger and with uniformity that is poorer than those of their single-crystal counterpart.

To implement useful circuits with poor-quality LTPS TFTs, one needs to develop an approach that differs from that of the single crystal integrated circuit, which heavily relies on the CMOS architecture. The current mode logic (CML) [2, 3] is a candidate for this purpose as it can reduce logic swing, which in turn reduces power consumption while maintaining or improving operating speed. The potential drawback of the CML design is its high power consumption, which comes from the static current that has to flow throughout the circuit operation. In the meantime, we have reported that the static power consumption can be significantly reduced and the CML inverter consumed less power than static CMOS inverter [4].

Manuscript received July 31, 2008; accepted for publication September 11, 2008.
* Member, KIDS; ** Student Member, KIDS
Corresponding Author : Ju Young Jeong
Department of Electronic Engineering, University of Suwon
2-2 Wau, Bongdam, Hwasung-si, Kyonggi 445-743, Korea
E-mail : jyjeong@suwon.ac.kr **Tel** : 031-220-2168 **Fax** : 031-220-2494

A multiplexer is an important logic circuit element that has a crucial role in multiple-input/single-output systems. In addition, multiplexers have been used in building logic functions of various degrees of complexity. In this work, we designed a CML multiplexer with LTPS TFTs fabricated using 2-micron technology. Then we applied the CML multiplexer to implement an AND/NAND gate as well as a OR/NOR gate. We used HSPICE and RPI TFT model throughout the work.

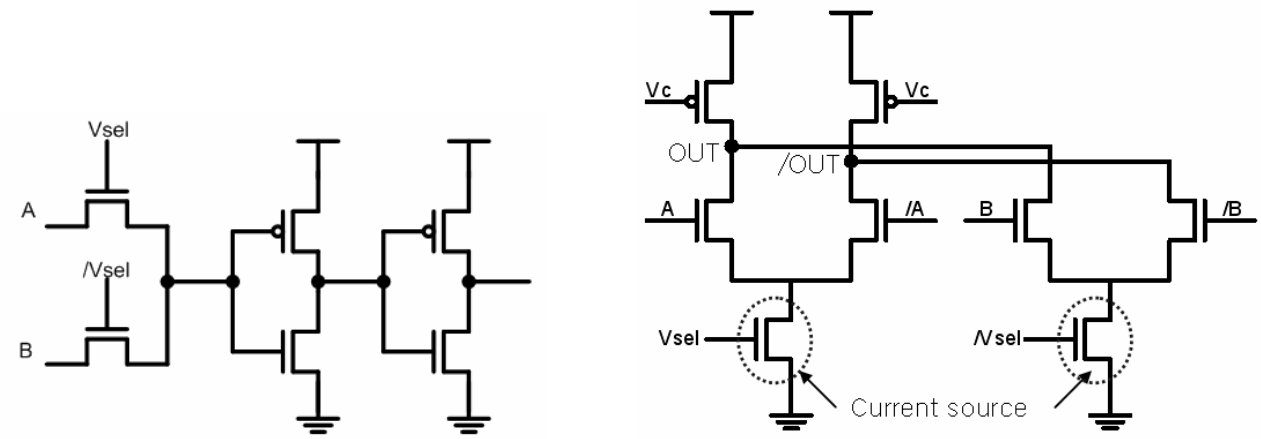
2. Design of CML Multiplexer

A multiplexer can be designed with six MOSFET as shown in Fig. 1 (a). Two-pass transistors at the input select which signal to propagate. Two cascading inverters block the noise and rebuild the logic levels that might have deteriorated by the pass transistor. As the threshold voltage of both pass transistors should be identical for accurate operation, this circuit structure cannot be used for TFT circuits due to poor uniformity. Furthermore, as two inverters in cascade have a logic swing of Vdd, power consumption and delay are large.

As an alternative, we adopted the current mode architecture, which was made of two CML inverters connected in parallel as shown in Fig. 1 (b). Two TFTs at the bottom were connected to SEL and /SEL control signal, respectively, and worked as current sources. According to the control signal, current flows either through the left or the right half of the circuit. Note that the input voltage for SEL and

/SEL swings between 0 and 2 volts. On the other hand, A, /A, B, and /B signal changes between 3 and 5 volts when Vdd is 5 volts. HSPICE simulation results of both the pass transistor and CML multiplexer are summarized in Fig. 2 (b) and (c), respectively. In Fig. 2 (b), the final output of the pass transistor multiplexer is represented by the dotted line. The other signal, which is in-phase with the output signal, is the pass transistor output whereas the 180-degree out of the phase signal is the output of the first CMOS inverter. The CML multiplexer output exhibited smaller delays according to the smaller logic swing as well as the capacitive load. Note that the circuit had been tuned to make the output change between 4.2 and 5 volts.

Although the CML multiplexer worked faster than the pass transistor-based counterpart, it exhibited problems such as severe glitches and slow current switching between two current sources as shown in Fig. 3 (b) and (c). The input signals were prepared to demonstrate the worst operating condition and the glitches in output signals are hardly acceptable in some cases.



(a) (b)

Fig. 1. Multiplexer schematics (a) based on pass transistor, (b) CML design architecture.

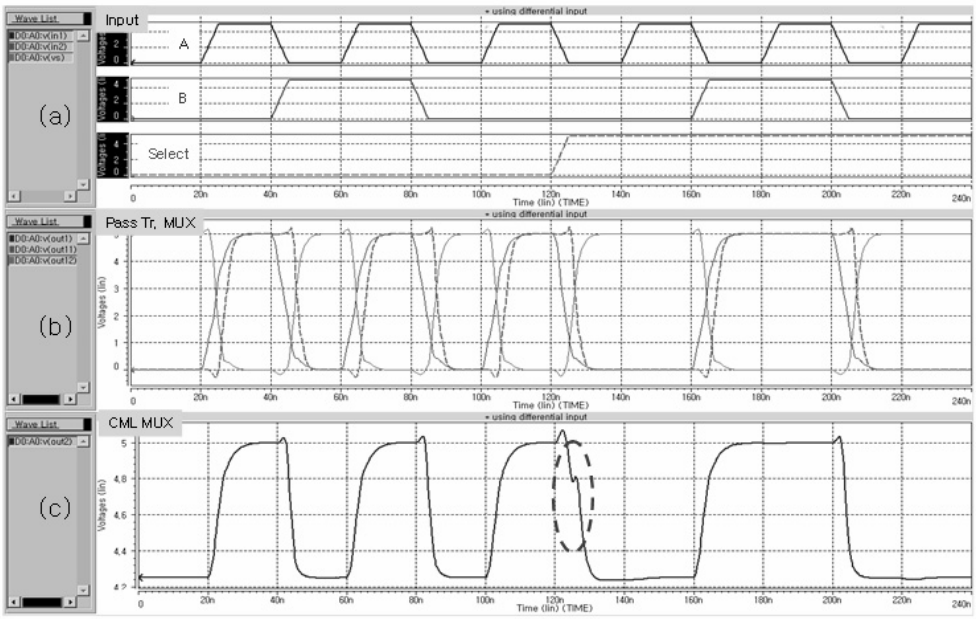


Fig. 2. HSPICE simulation result of multiplexer. (a) input signal A, B and control signal Select, (b) Output of pass transistor multiplexer, (c) output of CML multiplexer.

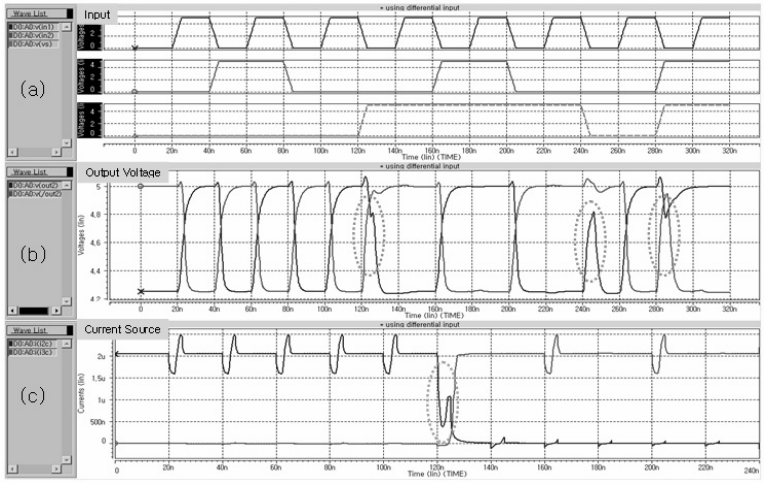
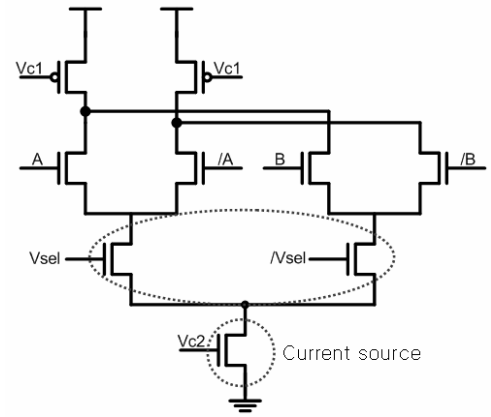


Fig. 3. Detailed HSPICE simulation results of CML multiplexer: (a) inputs, (b) outputs Out and /Out, (c) current supplied by both current sources.



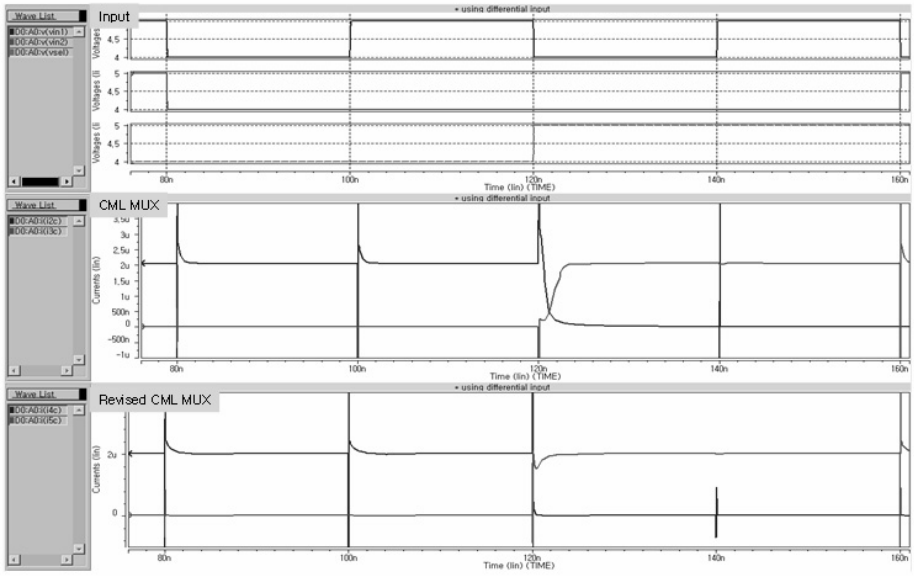
(a)

(b)

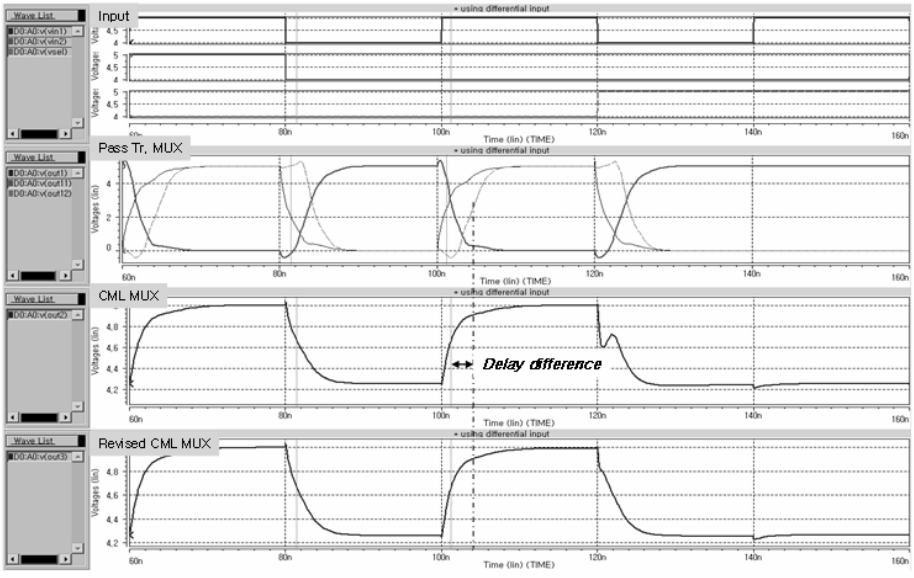
Fig. 4. Revised CML multiplexer: (a) circuit schematic and (b) HSPICE simulation results of the new design showing glitches improved to an acceptable level.

To obtain a more stable operation, a new, simpler CML multiplexer was developed by adding one more transistor to the existing circuit. Fig. 4 (a) shows the circuit schematic, which features only a single current source at the bottom. Here, Vsel and /Vsel signal only steered the currents whose amount is set by the bias voltage Vc2. One important advantage of this circuit was that all signals used the same voltage levels. This is a critical property in designing logic gates with this multiplexer. From Fig. 4 (b), the output voltage exhibited the worst case of glitch that was improved from the previous version of the circuit. As the current source stayed "on" by the bias voltage Vc2, the previously observed anomaly at 120 nsec in Fig. 3 (c) disappeared.

Fig. 5 shows a comparison of the multiplexers. In Fig. 5 (a), we observe the expected reduction of current steering delays in the revised CML multiplexers. This reduction did



(a)



(b)

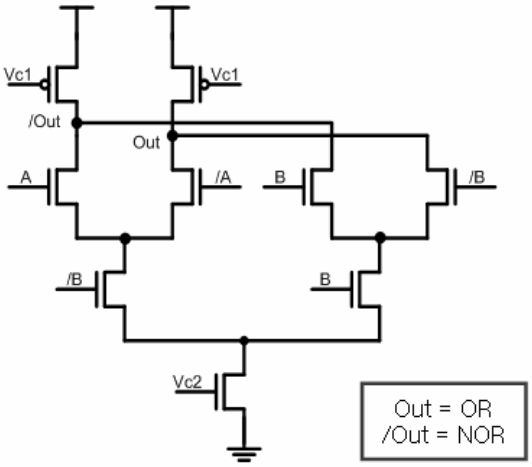
Fig. 5. Comparing performance of three multiplexers: (a) current steering characteristics of two CML multiplexers, (b) switching characteristics of three multiplexers investigated.

not lead to a delay reduction but it prevented any operational anomaly. Note the current levels were 2 micro amperes in both cases. Fig. 5 (b) showed a propagation delay of the three multiplexers. Two CML cases exhibited almost identical low-to-high transition delays. However, the first CML multiplexer had an anomaly during the high-to-low transition that the revised one did not have. From the simulation results, it is clear that the CML circuits with a 1 nsec delay were faster than that of the pass transistor with a 4 nsec delay. This improvement is attributed to the small voltage swing as well as the small switching load of devices that stayed on throughout the operation.

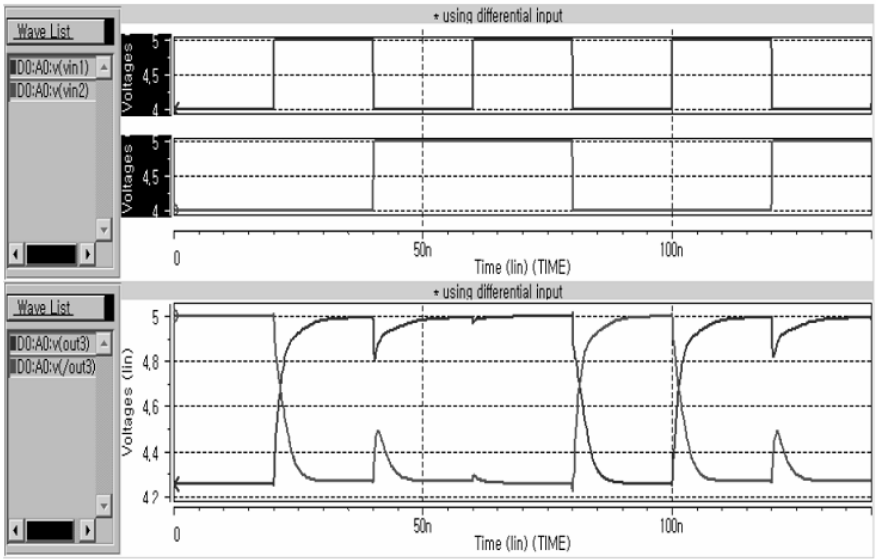
3. Design of CML Multiplexer Logic Gates

It is straightforward to design a NAND and NOR gate by using the previously designed current mode multiplexers. In addition, as the current mode circuits provided inverting and non-inverting the outputs, AND and OR gates were obtained without extra delay.

Fig. 6 (a) is the schematic of NOR/OR gate with CML multiplexers. We have replaced the control signal *Vsel* and



(a)



(b)

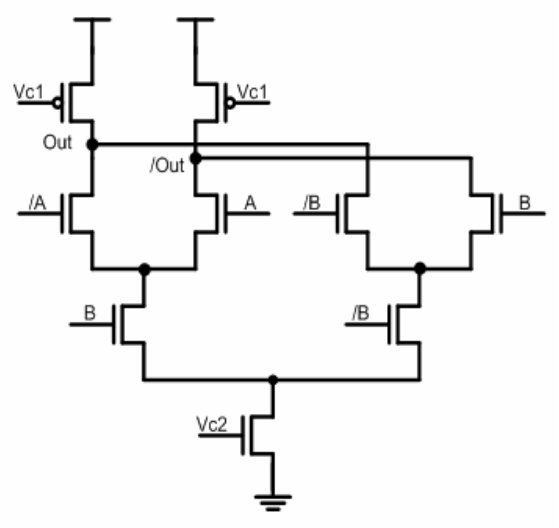
Fig. 6. NOR/OR gate designed with current mode multiplexer: (a) circuit schematic, (b) functional verification through HSPICE simulation.

/Vsel by logic input */B* and *B*. The HSPICE simulation results in Fig. 6 (b) showed operational stability including the worst case of simultaneous opposite transition of logic inputs at 40 and 120 nsec. In current mode logic, glitches are serious because of the small logic swing. However, the glitches did not cross each other and an error-free operation was ensured.

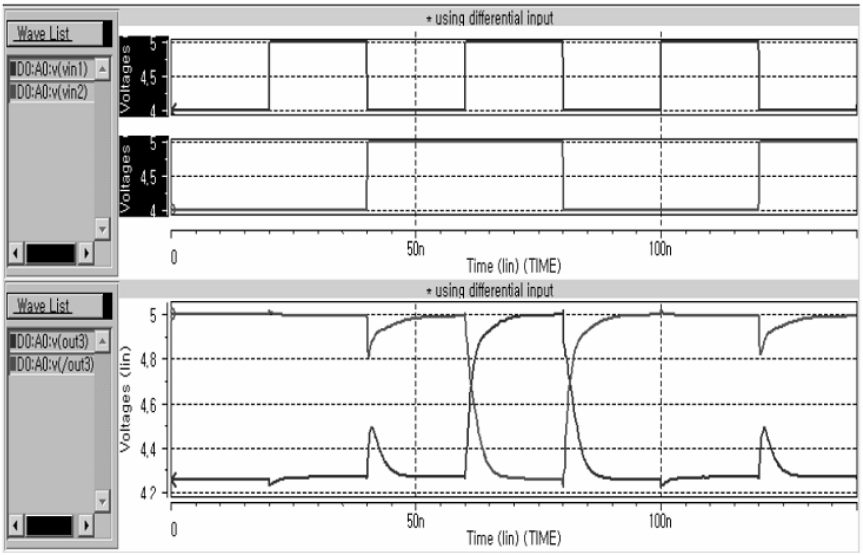
Fig. 7 (a) summarized our result of NAND/AND gate design. Only minor logic input connection change was needed to change the logic function of the circuit. This is the most obvious advantage of the multiplexer based logic gate design. The HSPICE simulation result for the gate is shown in Fig. 7 (b) and it had identical characteristics as that of the NOR/OR gate.

4. Conclusions

We designed improved current mode multiplexers for LTPS TFT applications. By adding one transistor, the new circuit enabled a more stable and faster current steering and



(a)



(b)

Fig. 7. NAND/AND gate designed with current mode multiplexer: (a) circuit schematic, (b) functional verification through HSPICE simulation.

improved noise margin even during the worst case input transition. The small logic swing, small switching capacitance, and current steering mode of operation contributed to obtain a significant delay performance improvement compared with that of the CMOS architecture. By using the multiplexers, we further designed NAND/AND and NOR/OR logic gates. As the architecture of the circuits are identical to the multiplexer, the delay remains the same irrespective of logic functions. A simple and straightforward implementation is advantageous and uniform delays among various logic gates can ease the system design procedure.

References

[1] Y. Matsueda, in Proc. IDW'00 (2000), p.171.

[2] A. Hairapetian, United States Patent: US 6,424,194 B1, July 2002.

[3] A. Bellaouar, United States Patent: US 6,492,840 B1, December 2002

[4] J-G Kim, J.Y. Jeong, and J, H. Hur, in Proc. IDW'04 (2004), p. 443.

[5] Y. Nakajima and Y. Maki, in Proc. IMID'04 (2004), p. 69.

[6] N. Toyozawa, Y. Nakajima, H. Yoshine, S. Noichi, K. Yuda, S. Toriyama, A. Ogawa, T. Yoshikawa, and Y. Maki, in SID'02 Digest (2002), pp. 686.

[7] G. Ferri & N. C. Guerrini, Low-Voltage Low-Power CMOS Current Conveyors (Kluwer Academic, Boston, 2003), ch. 3.