Effect of Some Design Factors in the Front Panel on the Characteristics of a Plasma Display

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Abstract

Low sustained voltage (V_s) and high luminous efficiency (lumen/Watts) are required for the enhanced performance of an AC PDP. Both are not realized in the same condition, however, because luminous efficiency decreases when the sustained voltage is lowered in most cases. In this study, the three design factors in the front panel of a PDP, i.e., the thickness and position of the bus electrode and the thickness of the dielectric layer, were chosen to investigate how they affect the sustained voltage and the luminous efficiency, and to find a way to optimize them. Two values were given to each of the three design factors, and experiments were done via full factorial design, i.e., with a total of eight conditions, using a 3-in.diagonal test panel. The changes in the sustained voltage and the luminous characteristics were explained in connection with the discharge characteristics of the PDP cells.

Keywords : bus electrode, dielectric layer, discharge characteristics, PDP, sustained voltage, luminous efficiency

1. Introduction

Today, the luminous efficiency of the commercial plasma display panel (PDP) is no more than about 1.0-1.5 lm/W, which is considered the product's biggest problem. A remarkable increase in the luminance of the PDP has been reported with positive column discharge [1] and high Xe concentration [2-3]. Positive column discharge uses a long-gap electrode structure between the x, y sustained electrodes to generate low electric field discharges, which enable more UV to be generated via a more effective excitation process. A high Xe concentration of more than 10% in the discharge cell allows more UV to be generated via the excitation of Xe atoms, the wavelength of which is similar to that of UV. Both effectively increase luminous efficiency, but have a fatal drawback, i.e., their increase of the sustained voltage with their increase of the luminance efficiency.

Besides, many researches on the modification of the PDP electrode structure have been conducted with the intention of enhancing the luminous efficiency of the PDP. Experimental results on changing the shape of the ITO electrode [4], the bus electrode [5], and the address electrode [6] have also been reported. Another approach to improving the luminous efficiency of the PDP through its electrode design involves changing the position of the bus electrode on the ITO electrode. Kang [7-8] reported that the in-bus structure showed a higher luminous efficiency and a shorter discharge ignition delay time than the conventional out-bus structure. Lee et al. [9], however, got the opposite results—i.e., that the out-bus structure is more efficient with the luminous characteristics.

Some results of these reports are confusing and are not in accordance with each other. It is supposed that some design factors such as the bus electrode and the dielectric layer have certain subordinate relationships to each other, so they cannot be considered independently.

In this study, the three design factors in the front panel of the PDP, i.e., the thickness and position of the bus electrode and the thickness of the dielectric layer, were chosen. The experiments were designed to consider the three factors at once, to investigate how they affect the sustained voltage and the luminous efficiency and to find a way to optimize them.

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2. Experimental methodology

The experiments were performed using a 3-in. test panel with a cell area of 360x1,080 μms^2 following the typical dimension of the discharge cell of a 42-in. PDP. Table 1 shows the specifications of the test panel that was manufactured in this experiment. PD200 (Asahi Glass) glass substrates that were 2.8mm thick were used as the front and rear substrates. The ITO electrode patterns were manufactured via photolithography using a photosensitive dry film. The bus and address electrodes were manufactured using photosensitive Ag paste. A dielectric layer was printed on the bus and address electrodes. Table 2 shows the design of the experiment. As shown in Fig. 1, the thickness and position of the bus electrode and the thickness of the dielectric layer were varied with two values each. The general specifications of the thickness of the bus electrode and the dielectric layer were 5 ㎛ and 30 ㎛, respectively. These were changed to 20 ㎛ and 45 ㎛, respectively. The position of the bus electrode was also changed from the in position to the out position.

Table 1. Specifications of the Test Panel.

Bus width	100 μm
ITO width	320 μm
ITO gap	80 μm
MgO thickness	7000 Å
Barrier rib height	130 μm
Gas pressure	400 Torr

Table 2. Experiment Design.

Thickness of the bus electrode	5 and 20 μm
Position of the bus electrode	In and out
Thickness of the dielectric layer	30 and 45 μm

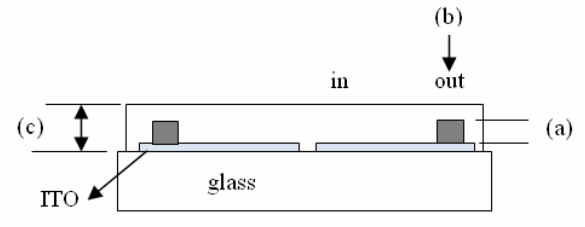

Fig. 1. Three design factors in the front panel of the PDP, which were chosen as the experimental factors: (a) thickness of the bus electrode, (b) position of the bus electrode, and (c) thickness of the dielectric layer.

A 7,000 Å-thick MgO layer was formed on the dielectric layer on the front panel as a result of the electron beam evaporation. Barrier ribs were manufactured via chemical etching, and green phosphors were printed into the cell volumes. The front and rear substrates were assembled and pumped at 350 ℃ for several hours, and filled with a gas mixture of Ne-5% Xe in 400 Torr.

The discharge and luminous characteristics of the panel were measured with the application of 25 kHz of sustained pulses with a 25% duty ratio. All the characteristics of the panel were observed at the median of the measured voltage margin. The luminance (cd/㎡) was measured with a luminance calorimeter (BM-7, TOPCON), and the electrical power consumption (W) was calculated using the following equation:

$$P = P_{on} - P_{off}, \quad \text{Eq. 1}$$

wherein P_{on} and P_{off} are the power consumptions when all the cells are on and off, respectively. The luminous efficiency was estimated using the following equation:

$$\eta = \frac{\pi L S}{P}, \quad \text{Eq. 2}$$

wherein L is the luminance, S is the total area of the discharge cells, and P is the power consumption. The evolution of the emission lights within a discharge cell was observed using ICCD (C8484-05G, Hamamatsu), and 200 V of sustained pulses were applied at a frequency of 35 kHz and a 25% duty ratio.

3. Results and discussion

Table 3 shows the estimated data on the sustained voltage (V_s) and the luminous efficiency (lm/W) of the PDP for each experimental condition shown in Table 2. There were eight experiments in all, and the estimated data was analyzed using a statistical technique. These eight experimental conditions had a 2x2x2 design, and there were three kinds of main effect plots for the three design factors shown in Table 2. Fig. 2 shows the main effect plot of the three design factors, i.e., the thickness and position of the bus electrode and the thickness of the dielectric layer for the sustained voltage. The lower value of the sustained voltage was obtained for the condition of the higher bus thickness

in the bus position and the lower dielectric thickness. The difference between the averaged values at the lower- and higher-level conditions (in other words, the main effect) was similar for the three design factors. Therefore, it can be said that the three design factors in the experiment had a similar degree of effect on the sustained voltage. These data must be analyzed, however, in ways that are not based on the viewpoint of statistics. As the main effect plot merely shows the averaged value, it does not show the interaction effect between the design factors. Therefore, the interaction effect between them was also analyzed in Fig. 3. A strong interaction effect between the thickness and position of the bus electrode was found in the upper left plot indicated by the dot. As shown in the main effect plot in Fig. 2, the in-bus position had a lower sustained voltage than the out bus position. This was true not only for the 5㎛-thick bus cases but also for the 20㎛-thick bus cases. There was a big difference, however, between the gradients of the straight lines for the 5㎛- and 20㎛-thick bus cases. In the case of the 20㎛-thick bus case, the sustained voltage had the lowest value, which significantly differed from the other conditions. This means that the sustained voltage can be reduced dramatically when the two conditions, the in bus position and the 20㎛bus thickness, are met at the same time. To analyze the effect of another factor, the dielectric thickness, the estimated data in Table 3 were divided into two cases, 30㎛ and 45㎛-thick dielectric layer cases. Figs. 4 and 5 show that the interaction effect between the position and thickness of the bus electrode is similar for different thicknesses of the dielectric layer, except that the sustained voltage was generally higher in the thicker dielectric layer case, as shown in Fig. 5.

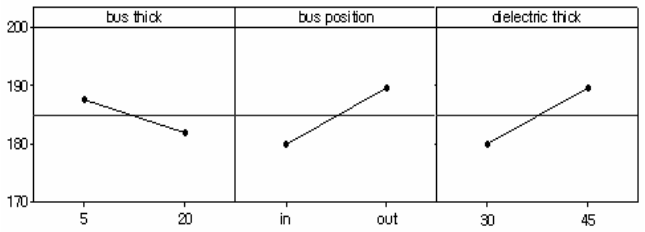

Fig. 2. Main effect plot of the design factors for the sustained voltage.

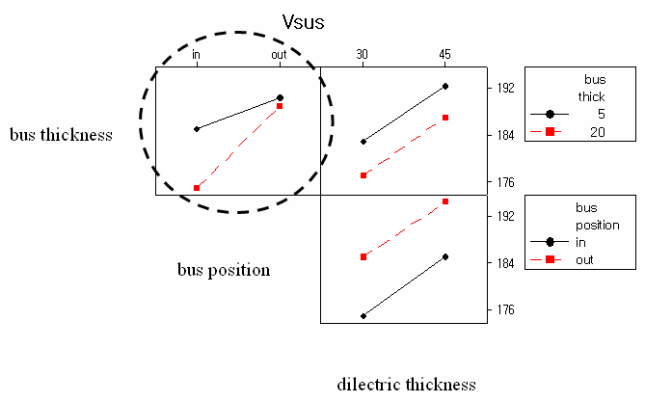

Fig. 3. Interaction plot of the design factors for the sustained voltage.

Table 3. Estimated Data on the Vsus and lm/W for Each Condition.

StdOrder	bus thick	bus position	dielectric thick	Vsus	lm/W
1	5	in	30	180	1.5
2	20	in	30	170	1.4
3	5	out	30	186	1.6
4	20	out	30	184	1.5
5	5	in	45	190	2.1
6	20	in	45	180	2
7	5	out	45	195	2
8	20	out	45	194	2.1

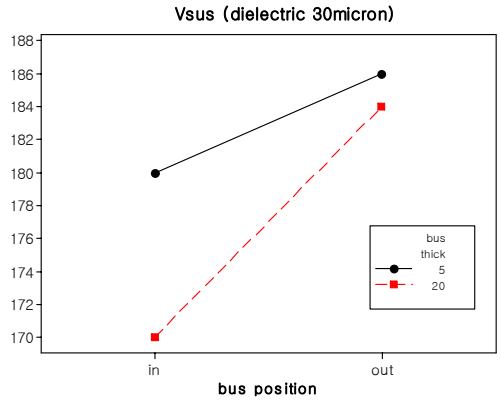

Fig. 4. Effect of the thickness and position of the bus on the sustained voltage (the dielectric thickness was 30 ㎛).

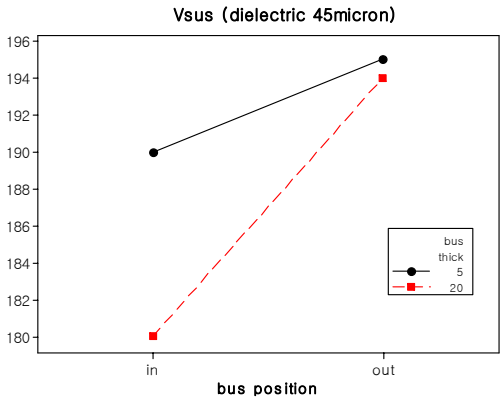

Fig. 5. Effect of the thickness and position of the bus on the sustained voltage (the dielectric thickness was 45 ㎛).

To explain these results, the feature of the PDP cell discharge was first investigated using ICCD. Fig. 6 shows the time evolution of the ICCD pictures of the PDP cell. The discharge started from around the electrode gap between the two ITO electrodes and was propagated into the adjacent ITO electrode area. It was thus assumed that the discharge features around the gap determined the sustained voltage. Fig. 7 is a schematic drawing that illustrates the discharge path in the PDP front panel. There are two paths, the short path via A and the long path via B, but only path A was investigated, as it was through it that the discharge started. As explained in Fig. 8, the equivalent circuit of the discharge path consisted of two C_d and one C_g, a series circuit. In this case,

$$\frac{1}{C_t} = \frac{1}{C_d} + \frac{1}{C_g} + \frac{1}{C_d} \qquad \text{Eq. 3}$$

and

$$C = \varepsilon \frac{A}{d} \qquad \text{Eq. 4}$$

wherein C is the capacitance, ε is the dielectric constant, A is the cross-sectional area, and d is the length of the path. From Q = CV (Q is the charge accumulation), V is proportional to 1/C, so V, which was applied to the circuit, was divided into each component proportionate to d/ε, assuming that A was the same. Using the general value of C_d and C_g, 15 and 1, and assuming that the thickness of the dielectric

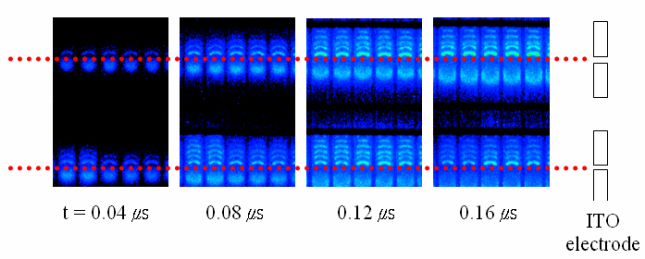

Fig. 6. Time evolution of the ICCD pictures of the PDP cell.

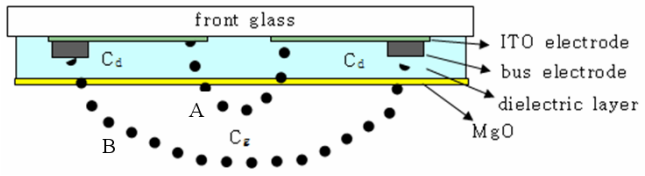

Fig. 7. Schematic drawing illustrating the discharge path in the PDP front panel.

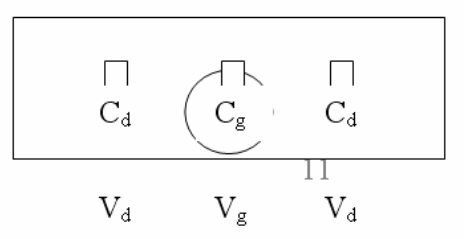

Fig. 8. Equivalent circuit of the discharge cell. C_d and C_g are equivalent capacitances of dielectric and gas, respectively.

Table 4. Estimated Voltage Distribution for Path A in Fig. 7.

Case	d/ε for Dielectric	d/ε for Gas	V_d/V_g
No bus	30/15	100/1	4%
5㎛-thick bus	25/15	100/1	3.3%
20㎛-thick bus	10/15	100/1	1.3%

layer was 30 ㎛ and the discharge length of the gas through path A was 100 ㎛, the distribution of V through path A in Fig. 7 is estimated in Table 4. Comparing the three cases, that with no bus, that with a 5㎛-thick bus, and that with a 20㎛-thick bus, on the ITO electrode through discharge path A, V_d was the lowest for the 20㎛-thick bus case, which means it had the lowest sustained voltage due to the lowest voltage loss in the dielectric layer. This can explain the interaction effect between the thickness and the position of the bus electrode in Fig. 3.

Next investigated was the luminous efficiency data in Table 3. Fig. 9 is a main effect plot of the design factors for luminous efficiency. The effect of the dielectric thickness was clearly much bigger than the thickness and position of the bus electrode. Fig. 10 is an interaction plot of the design factors for luminous efficiency. Although there was a weak interaction effect between the thickness and position of the bus electrode, it was negligible compared to the effect of the dielectric thickness. Therefore, it must only be explained why the luminous efficiency increased as the dielectric thickness increased from 30 to 45 ㎛. The investigation of the time evolution of the discharge of the PDP cell in Fig. 6 showed that the discharge occurred all over the cell area after the initial stage in the discharge process. Therefore, the entire ITO electrode area must be considered in the investigation of the power consumption and luminance efficiency. In this case, the displacement capacitance between the sustained electrode is expressed as:

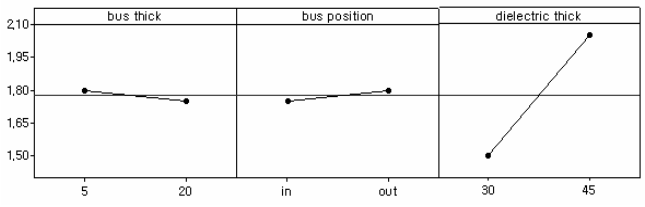

Fig. 9. Main effect plot of the design factors for luminous efficiency.

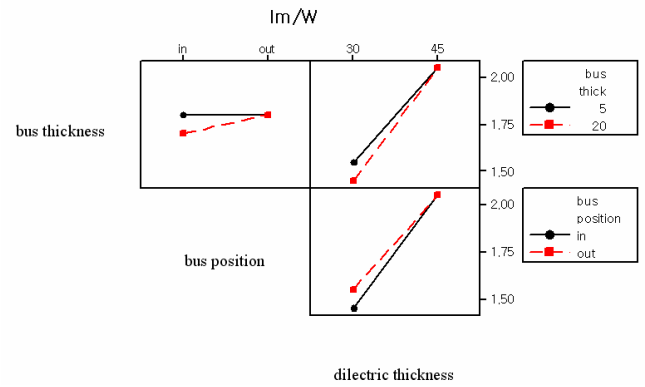

Fig. 10. Interaction plot of the design factors for luminous efficiency.

$$C_t = \oint_A C\, dA = C_1 + C_2 + C_3 + \cdots . \qquad \text{Eq. 5}$$

In Eq. 4, the displacement capacitance C is inversely proportional to d, the dielectric thickness in this case, so the power loss through the displacement capacitance decreases with the increase in the dielectric thickness. This explains why the luminous efficiency increased as the dielectric thickness increased from 30 to 45 ㎛ in Fig. 9.

Combining the results of the investigation of the experimental data on the sustained voltage and the luminous efficiency, the first higher dielectric thickness is recommended for the increase in the luminous efficiency. In this case, the sustained voltage also increased, and it can be decreased by changing the bus position to that near the ITO electrode gap and increasing the thickness of the bus electrode.

4. Conclusion

As there are interaction effects between the thickness and position of the bus electrode and the thickness of the dielectric layer, these factors should be investigated together, and the interaction should be considered. The main effect and interaction were investigated through a full factorial experimental design of the three factors. The analysis of the data showed that the lowest value of the sustained voltage was obtained when the bus electrode was near the ITO electrode gap and when the thickness increased to 20 ㎛. This can be explained with the analysis of the discharge path, wherein the shorter discharge length through the dielectric layer allowed a higher portion of the voltage to be distributed into the discharge gas.

In the case of the luminous efficiency, a higher dielectric thickness is recommended for the increase in the luminous efficiency, which is explained by the fact that the power loss due to the displacement capacitance became lower as the dielectric thickness increased. Combining the results of these two investigations on the sustained voltage and the luminous efficiency, the optimum condition with a low sustained voltage and a high luminous efficiency is proposed.

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