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A Study of a Simple PDP Driver Architecture using the Transformer Network

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ABSTRACT

In this paper, a cost-effective PDP driving circuit using the transformer network is proposed. Compared with the previous works, the half-bridge type energy recovery circuit recovers the reactive energy not to the capacitor but to the source. A single sustain board architecture removes the blocking switches which are placed on the discharge path in parallel, thus reducing the number of devices. A simple reset circuit generates the same waveform as the previous approaches. The circuit configuration and modified driving waveforms are compared with the previous works. The validity of the proposed simplified driver is verified through tests using a 6-inch panel

Keywords: Plasma display panel, Energy recovery circuit, Single sustain driver, Half-bridge

1. Introduction

With large screen sizes, wide viewing angles and high contrast ratios, Plasma Display Panels (PDP) lead the Flat Panel Display (FPD) market along with Liquid Crystal Displays (LCD). However, the rapid development of the manufacturing process and the variety of the backlight units has boosted LCD's as the leading display device, and PDP displays are faced with new challenges such as full HD image quality, low voltage driving, high luminous efficacy and cost reduction. For the high speed addressing, the address driving voltage (V_A) needs to be decreased, while the sustain voltage (V_S) must be increased. Because 60% of a PDP Display's power is consumed during the sustain period, researches on the sustain circuit have been actively continued with the aim of increasing energy recovery [1-10]. Efficiency improvement and cost reduction require a study of the overall system architecture.

In this paper, a cost effective PDP driver system which adopts the transformer network as an energy recovery circuit (ERC) is proposed. Using the positive and negative V_S, the single half-bridge type ERC recovers the reactive panel energy to the source and removes the clamping diodes. The negative blocking switches (S_{NB}) as well as the positive blocking switches (S_{PB}) are removed, thus reducing the device count. A simple reset circuit generates the same waveform as the previous approaches. Because the proposed PDP driver produces the same relative voltage for the three electrodes, the same discharge characteristic is guaranteed.

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2. Conventional System Configuration

Figure 1 shows the conventional PDP driving system architecture. Three main boards exist to induce the

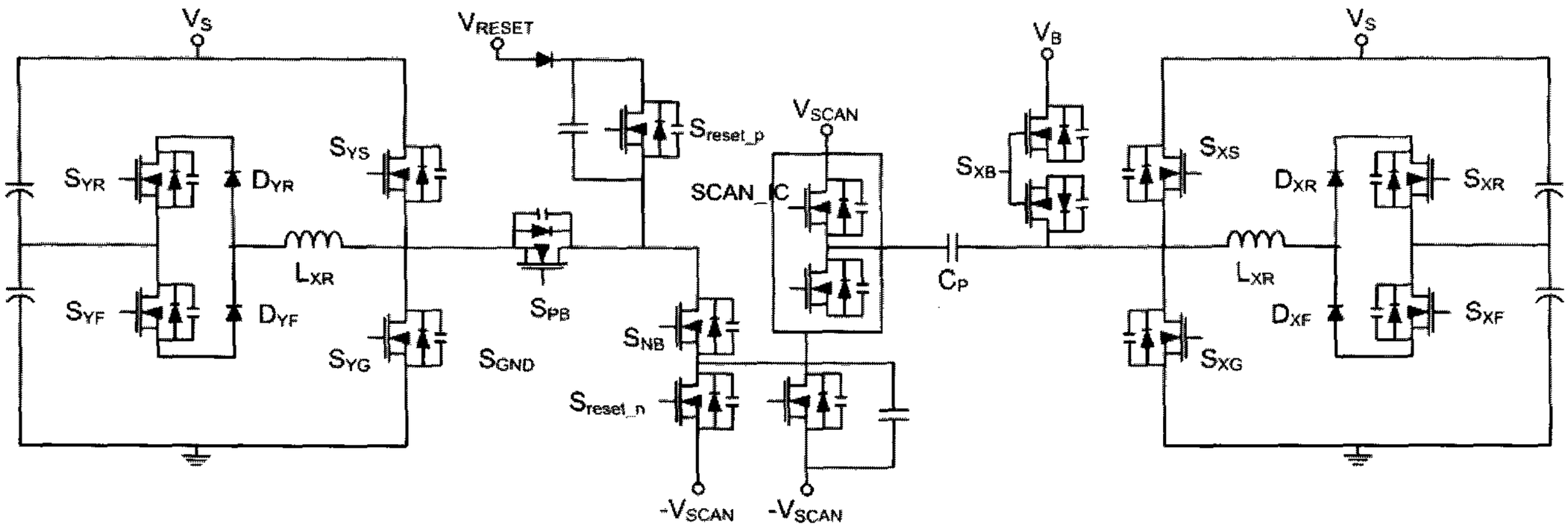


Fig. 1 System architecture of the conventional PDP driver

specific driving waveform on each electrode. Normally the address circuit only operates during the address period and therefore the main research issues are related to the X board and the Y board which are used during the scan and sustain periods. Sustain switches (S_{YR}, S_{YF}, S_{YS}, S_{YG}, S_{XR}, S_{XF}, S_{XS} and S_{XG}) operate to recover the panel energy during the sustain period. The bias voltage switch (S_{XB}) turns on during the negative reset period to erase and set up the wall voltage of the panel well. S_{PB} is used for the charge pump operation for the main reset voltage source, and S_{NB} is used to block the negative source from connection to ground. These are connected directly on the panel discharge path in series. In practice, several switches are connected in parallel to realize S_{PB} and S_{NB} because the current stress is as high as the discharge current. Therefore, the actual number of devices is increased, thus resulting in increased complexity and cost.

3. Proposed System Architecture

The proposed PDP driver with a reduced device count and circuit complexity is shown in Fig. 2. Compared with the full-bridge type of the sustain circuit, the half-bridge type configuration reduces the number of main and auxiliary switches in half. Using the transformer, the resonant source is replaced from the auxiliary capacitors to the transformer. The clamping diodes are removed and the leakage inductance of the transformer (L_{XR}) is utilized as the resonant inductor. With the pairs of opposite sustain sources, S_{PB} and S_{NB} are removed and a simple reset circuit generates the required voltage waveforms. Though the ground switches are introduced, the previously needed high current-rated devices are not required because these switches are not connected on the discharge path in series. All in all, in comparison to the previous works, the board layout is greatly simplified.

3.1 Reset circuit

Figure 3 shows the equivalent reset circuit configuration used in the proposed PDP driver. It consists of one switch (S_{reset_P}), a resistor (R) and a zener diode. The sustain voltage source and zener diode are used for the reset voltage source. Before the reset period starts, the panel voltage is charged up to the V_{SCAN}. With a consecutive turn-on of S_{reset_p}, the panel voltage is increased to (V_S-V_Z). Two control algorithms for the linear-type ramp waveform are described in Fig. 4. In the case of fixed frequency control, if the voltage step resolution is V_S/n, then the required on time in each period is determined as (1);

$$t_{on\_k} = RC_P \times \ln\left((V_S - V_Z)\left(\frac{n+(k-2)}{n}\right)\right) \quad (1)$$

If the duration time of the period is the control variable, then the required period in each voltage is described as (2)

$$T_k = T_1\left((V_S - V_Z)\left(1 - e^{\frac{t_{on}}{RC_P}}\right)^{k-1}\right) \quad (2)$$

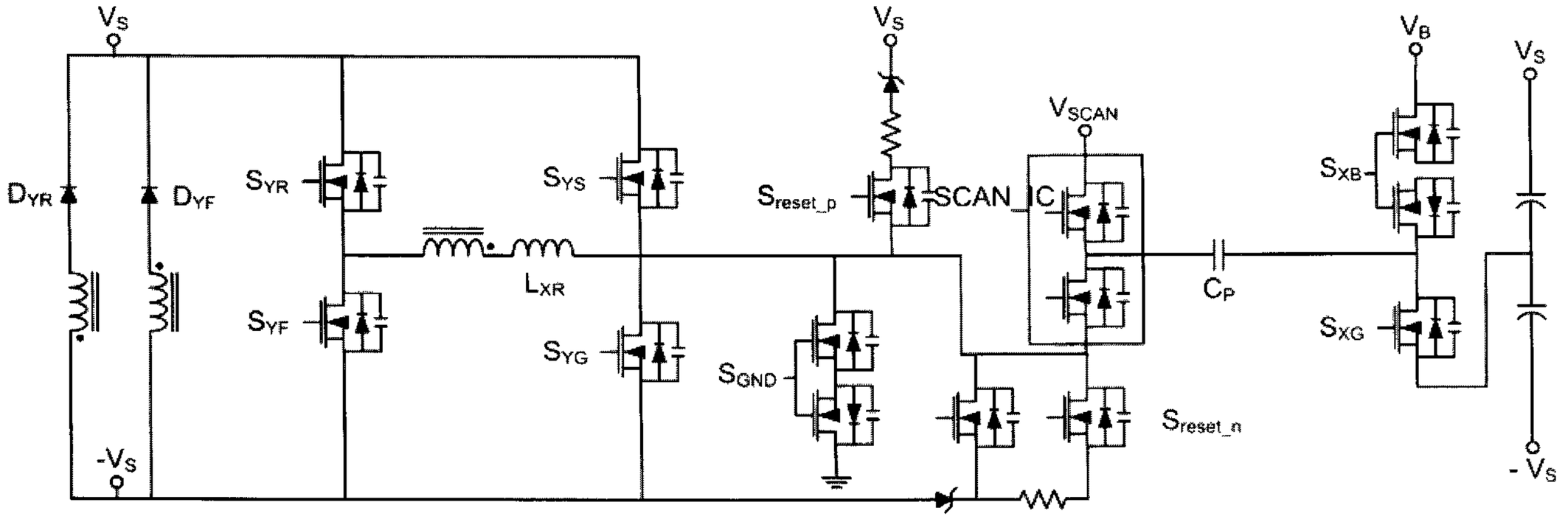


Fig. 2 The proposed PDP driver

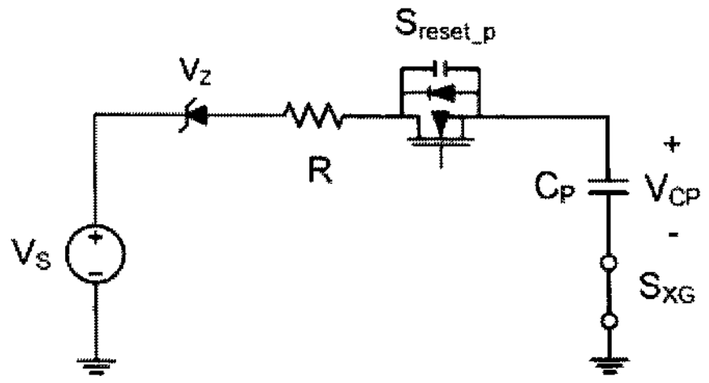
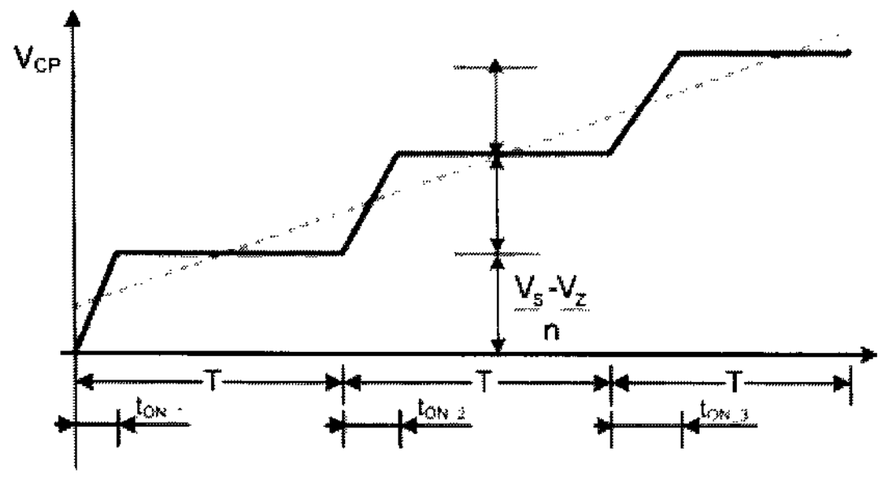
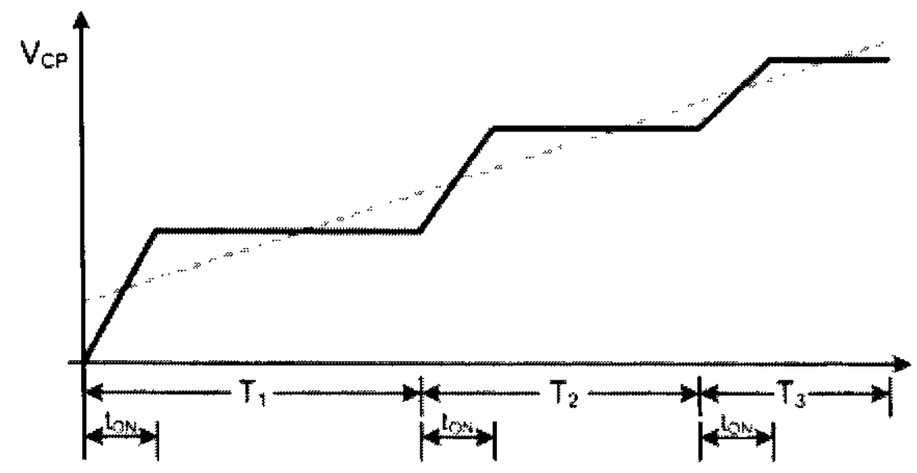


Fig. 3 The equivalent circuit during the reset period



(a) Fixed frequency control



(b) Variable frequency control

Fig. 4 Two control algorithms for the reset voltage waveform

In both cases, increasing the value of R results in a smooth voltage transition, but the final voltage is also decreased. Using the series gate resistor (R_{gate}) is an alternative method to achieve the wide control margin of the ramp voltage waveform. The gate sequence controller (normally an FPGA board) sends the fixed gate sequence to S_{reset_P} and the waveform is adjusted by tuning the R and R_{gate} value. The negative reset waveform is generated using a similar operation as the positive reset waveform.

3.2 Sustain driver

Two main aims of the sustain driver are supplying the discharge energy and recovering the stored reactive energy in the panel. The proposed circuit adopts the half-bridge type ERC, thus achieving a simple board layout. The transformer replaces the auxiliary capacitors and the body diodes of the switches are used for the clamping action. Figures 5 and 6 show the modes of operation and the key waveforms during the sustain period, in which four modes exist in one period. To analyze the circuit simply, all of the devices are assumed to be ideal. During the sustain period, S_{XG} is in the on state. The turns ratio of transformer is defined as n (the secondary side turns vs. the primary side turns).

MODE 1 [$t_0 \sim t_1$]: Before t_0, the panel voltage (V_{CP}) is charged to V_S. The inductor current (I_{lr}) is zero. S_{YS} is turned on at t_0 and the panel starts to discharge. After the discharge is finished, the wall charge is rebuilt for the next discharge.

MODE 2 [$t_1 \sim t_2$]: At t_1, S_{YS} is turned off and S_{YF} on. Negative V_S is used for the soft transition. When the primary side of the transformer conducts, the current starts to flow through the secondary side of the transformer; hence D_{YF} is turned on. nV_S is transferred to the primary side and it is subtracted from the panel's initial voltage (V_S). Thus, $(-2+n)V_S$ is used for the resonance source. V_{CP} starts to decrease to $-V_S$. The panel voltage and inductor current are expressed as (3) and (4), respectively. In (4), R includes the parasitic resistance, R_{DS_ON}, etc.

$$v_{CP} = \frac{\left(-V_S - V_{CP}(t_1) + nV_S\right)}{2\omega L_r C_P} \times \left(\frac{1}{\alpha^2 + \omega^2}\right) \times \left(1 - e^{-\alpha(t-t_1)}\omega\cos\omega(t-t_1) + e^{-\alpha(t-t_1)}\alpha\sin\omega(t-t_1)\right) + V_{CP}(t_1) \quad (3)$$

$$i_{lr} = \frac{\left(-V_S - V_{CP}(t_1) + nV_S\right)}{\omega L_r} \times e^{-\alpha(t-t_1)}\sin\omega(t-t_1) \quad (4)$$

where $\omega_o = \frac{1}{\sqrt{L_r C_P}}$, $\alpha = \frac{R}{2L_r}$, $\omega = \sqrt{\omega_0^2 - \alpha^2}$

MODE 3 [$t_2 \sim t_3$]: When V_{CP} reaches $-V_S$ at t_2, the zero voltage switching (ZVS) condition of S_{YG} is achieved. After S_{YG} turned on, the panel starts to discharge. I_{lr} goes to zero and S_{YF} is turned off under the zero current switching (ZCS) condition.

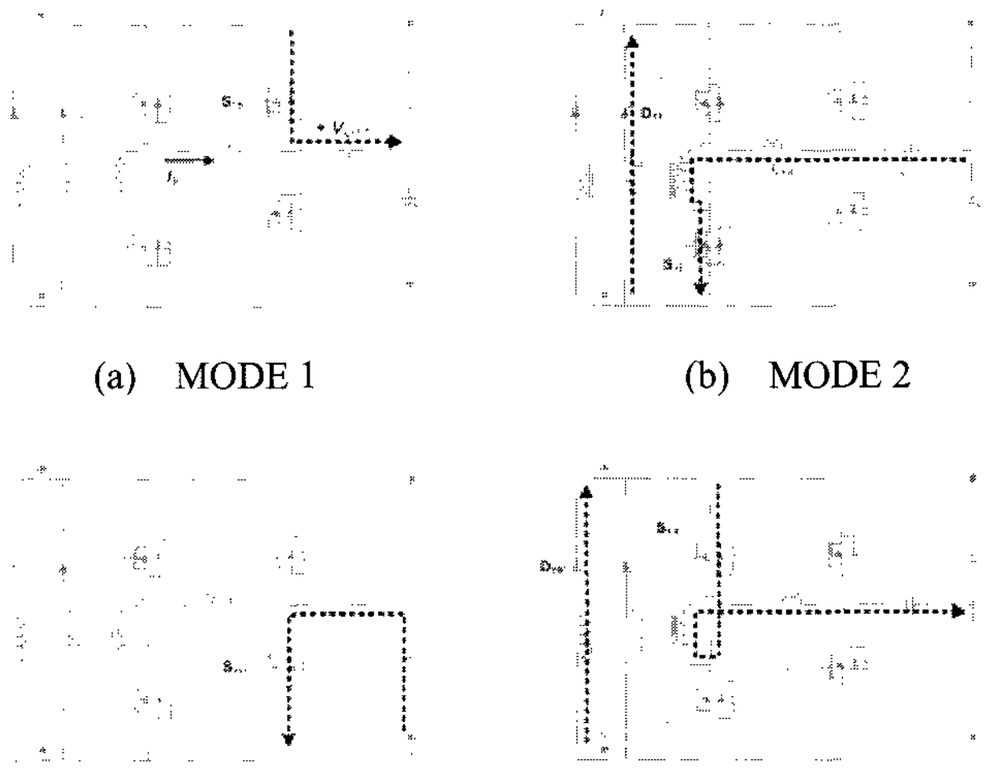
$$v_{CP} = \left(V_S - V_{CP}(t_2)\right)\left(1 - e^{-\frac{t-t_2}{RC}}\right) - V_{CP}(t_2) \quad (5)$$

$$i_{lr} = \frac{-V_S + V_{CP}(t_1)}{R} e^{-\frac{t-t_2}{RC_P}} \quad (6)$$

MODE 4 [$t_3 \sim t_4$]: After the discharge is finished at t_3, S_{XG} is turned off and S_{XR} is turned on. The resonant current flows through the primary side of the transformer; hence D_{XR} is turned on and the voltage of $-nV_S$ is applied to the primary side. Similarly to MODE 2, C_P resonates with L_r and V_{CP} goes to V_S. The panel voltage and inductor current are expressed as (7) and (8), respectively.

$$v_{CP} = \frac{\left(V_S - V_{CP}(t_3) - nV_S\right)}{2\omega L_r C_P} \times \left(\frac{1}{\alpha^2 + \omega^2}\right) \times \left(1 - e^{-\alpha(t-t_3)}\omega\cos\omega(t-t_3) + e^{-\alpha(t-t_3)}\alpha\sin\omega(t-t_3)\right) + V_{CP}(t_3) \quad (7)$$

$$i_{lr} = \frac{\left(V_S - V_{CP}(t_3) - nV_S\right)}{\omega L_r} \times e^{-\alpha(t-t_3)}\sin\omega(t-t_3) \quad (8)$$



(a) MODE 1 (b) MODE 2

(c) MODE 3 (d) MODE 4

Fig. 5 Operating mode transition and equivalent circuit

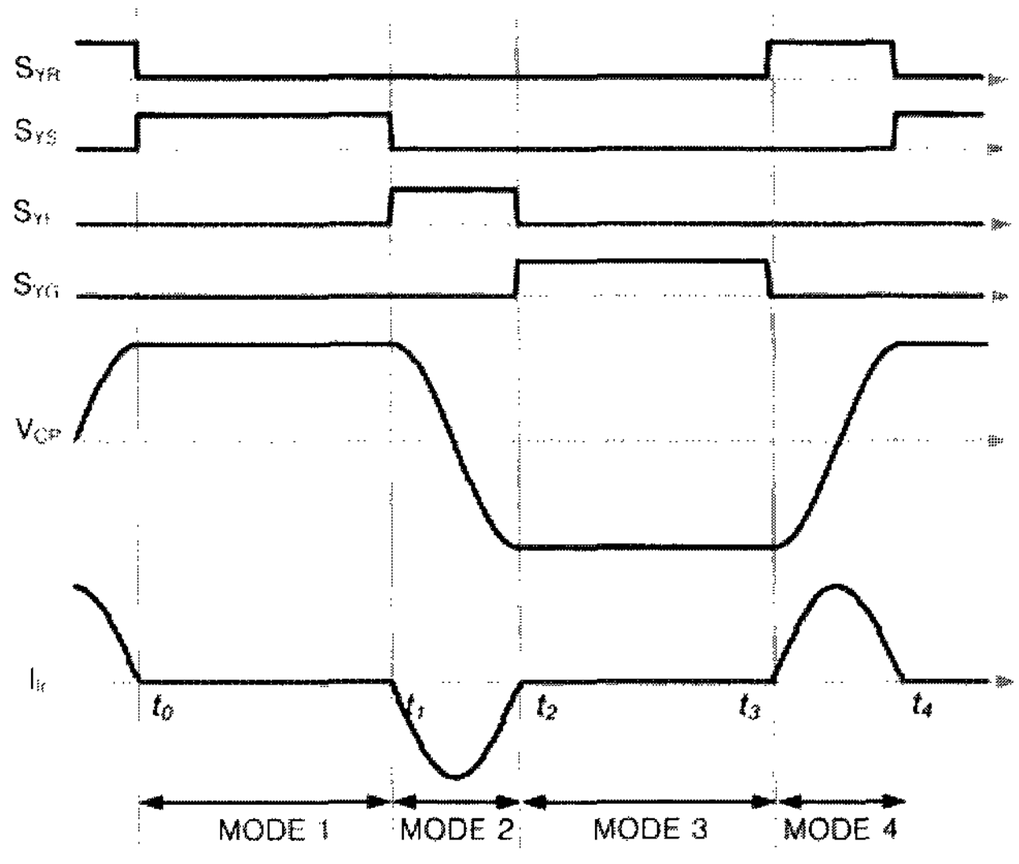
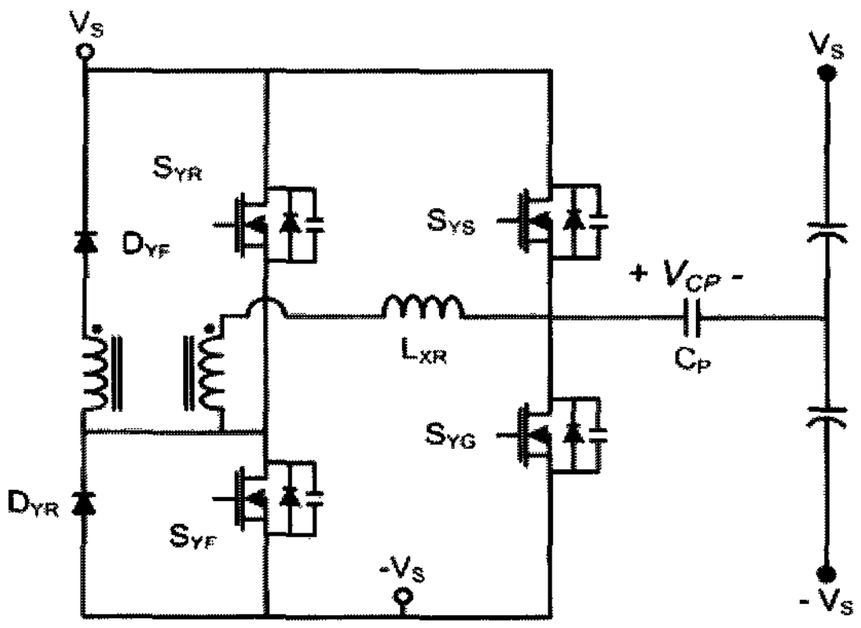


Fig. 6 Key waveforms

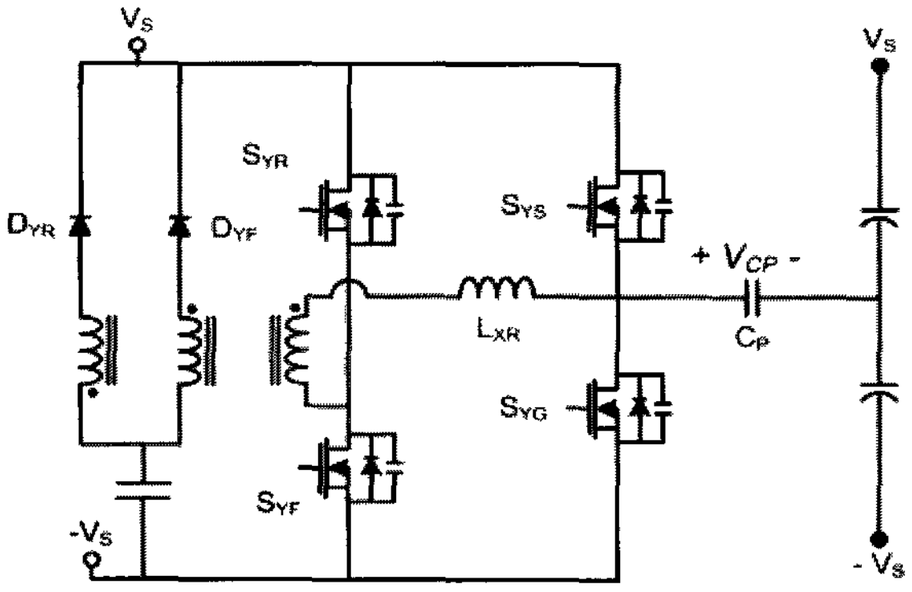
Using the transformer network, the single half bridge-type sustain driver reduces the number of devices. Table 1 shows the comparison of the device count between the previous and proposed works. The blocking switches are removed and the resonant inductor is replaced by the leakage inductance of the transformer. The energy recovery source is substituted from the auxiliary capacitors to a single transformer. The floating ground

condition of the auxiliary switches in the previous topology is removed; hence the switch gate driver is simplified. Using the transformer turns ratio with the current injection method, the design freedom is enhanced for the ZVS and ZCS of the switches.

Figure 7 shows the alternative circuits of the proposed sustain driver. A simple two winding transformer reduces the complexity, as shown in Fig. 7(a). Using the auxiliary capacitor, the voltage stress of D_{XR} and D_{XF} is reduced by half, but the conduction loss is increased.



(a) two winding transformer type



(b) voltage stress reduction type

Fig. 7 Alternative circuits of the proposed sustain driver

Table 1 Comparison of the number of devices

	Switch	Diode	Inductor	Recovery Source
Previous circuit	15	8	2	Capacitor (4)
Proposed circuit	11*	2	0**	Transformer (1)

* reduce the blocking switches (2 S_{NB} and 2 S_{PB})

** use the leakage inductance of the transformer

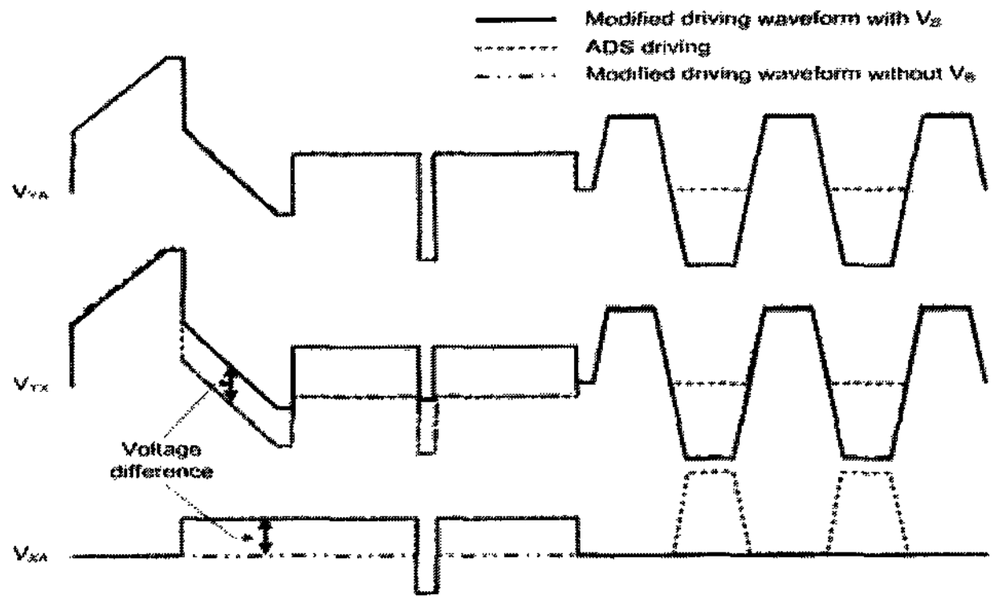


Fig. 8 Comparison of ADS and modified method for the proposed driving system

3.3 Driving waveforms

Before the operation of the proposed driver, the driving voltage waveform on each electrode needs to be studied with the previous works. Figure 8 shows the various waveforms of the conventional address display separated (ADS) method and modified ADS method for the proposed driver. The case of V_B-free driving is also considered. As previously studied in [11], it is able to match the voltage difference between the Y and A electrodes in all cases. However, without V_B, the voltage difference between Y and X (and X and A) exists during the negative reset period. It results in the wrong erase and wall charge build-up operation. Using V_B, there still exists the voltage difference between Y and X, but this exists on the sustain period and does not affect the X-Y sustain discharge. In the case of [11], the address waveform compensation method is proposed. However, this method requires a complex address circuit and more power consumption, which results in a higher cost. The proposed driving system adopts the V_B circuit on the bridge board to reset the panel properly.

4. Experimental Results

To verify the proposed circuit, a 6-inch PDP panel is used. The voltage transition time is fixed to 0.35usec for the conventional circuit and 0.7usec for the proposed circuit. To compare the proposed circuit with the previous work, the number of devices shown in Table 1 are used for the two methods. Table 2 shows the design specification and circuit parameters used in the experiment. The driving

sequence explained in Fig. 8 is applied from the FPGA board to the gate drivers. Because the main issues of this paper focus on the reset and sustain discharge with the proposed driver, the address electrodes are uniformly selected all at once during the address period.

Fig. 9 shows the reset voltage waveform which is generated by the proposed PDP driver. Using the variable frequency control method explained in Fig. 4(b), with an R of 100Ω, the linear-type reset waveform is achieved. Without V_B on the X electrode, the negative reset does not decrease to the required voltage level, thus resulting in a weak address discharge and wall voltage setup.

The panel sustain voltage waveforms during the sustain period, with and without V_B, are shown in Fig. 10. Using V_B during the negative reset period (shown in Fig. 10(a)) uniform light is radiated. Without V_B, the X-A waveform did not erase and setup the wall charge well, it results in the insufficient discharge between the X and A electrode during the sustain period in Fig. 10(b).

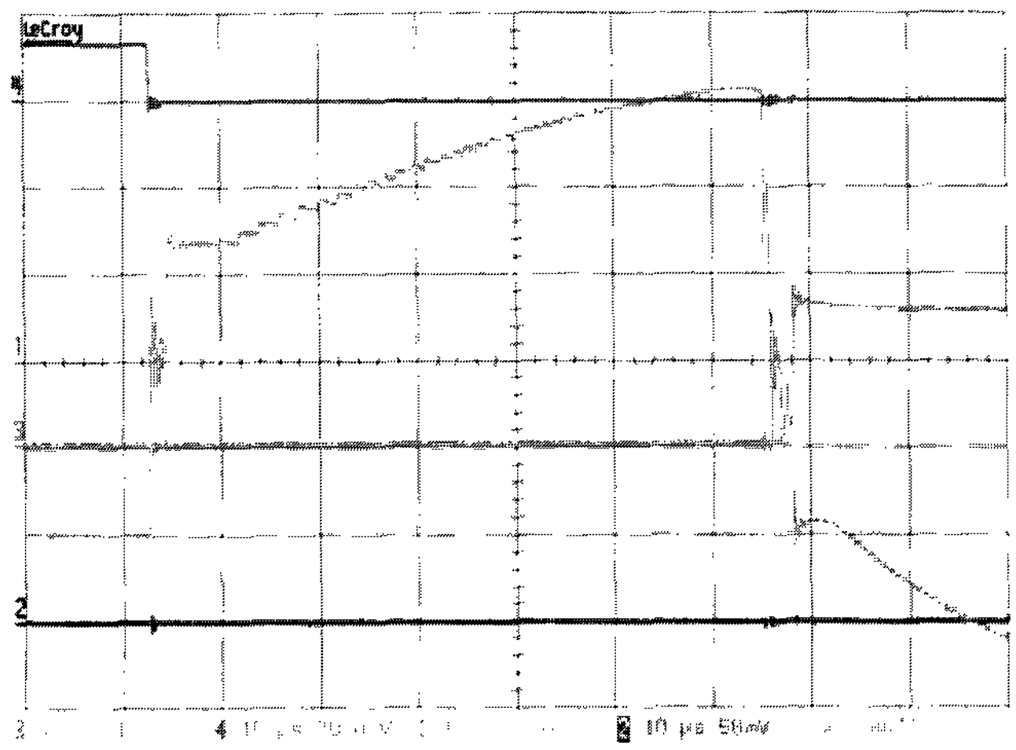
The input current of each driver is compared in Fig. 11. With a voltage variation of 150~180V, the current of the proposed circuit shows similar values as the conventional circuit and little difference is caused by the switching loss of the auxiliary switches.

5. Conclusions

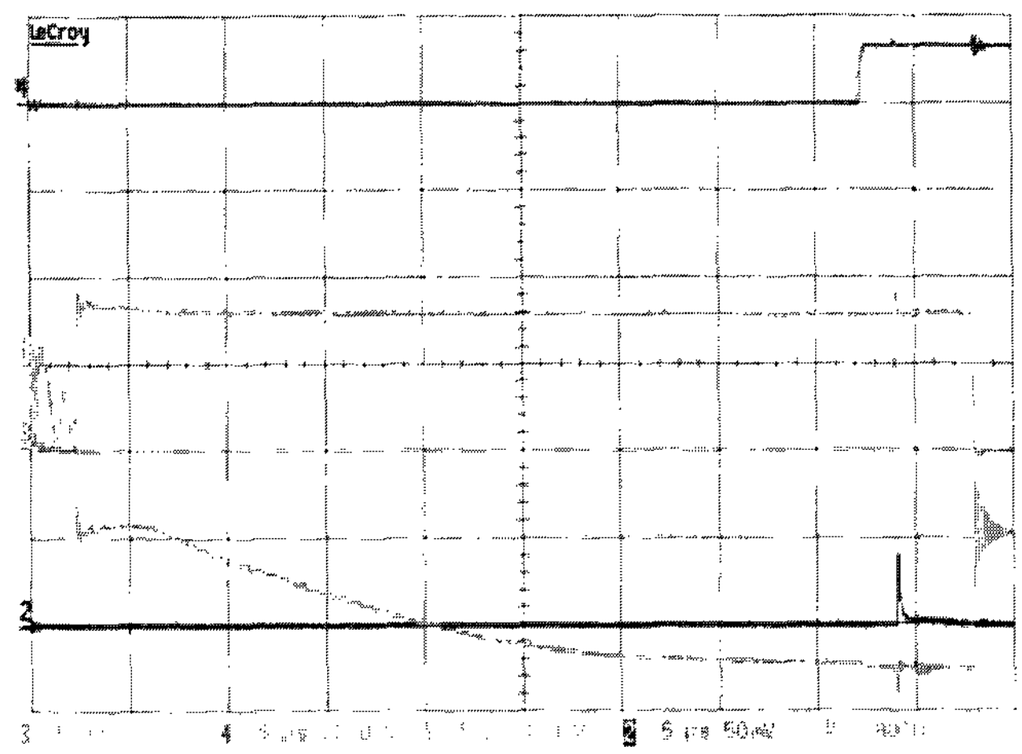
This paper proposes a cost-effective PDP driver using the transformer network. The positive blocking switch (S_{PB}) and negative blocking switch (S_{NB}) are removed by adopting a pair of opposite sustain sources. A simple reset

Table 2 Design specifications and circuit constant

	Proposed circuit	Previous circuit
Switch	FQA50N50	FQA 55N25
Diode	STTH3010A	FML-36S
Resonant source	EI40, n=0.5 (4:8:8), 0.24*26 litz wire. L_r=1uH, L_m=80uH	MPE capacitor, 3.3uF*4
Driver IC	IRS21851SPBF	
Panel	6 inch PDP cells	

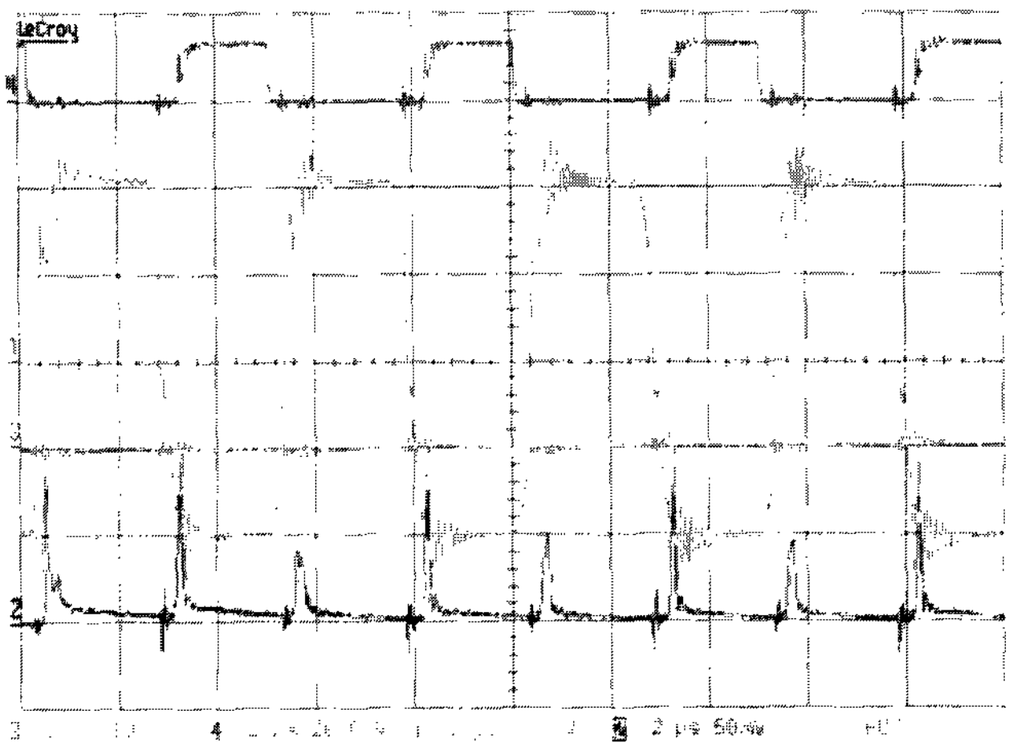


(a) Positive reset voltage waveform

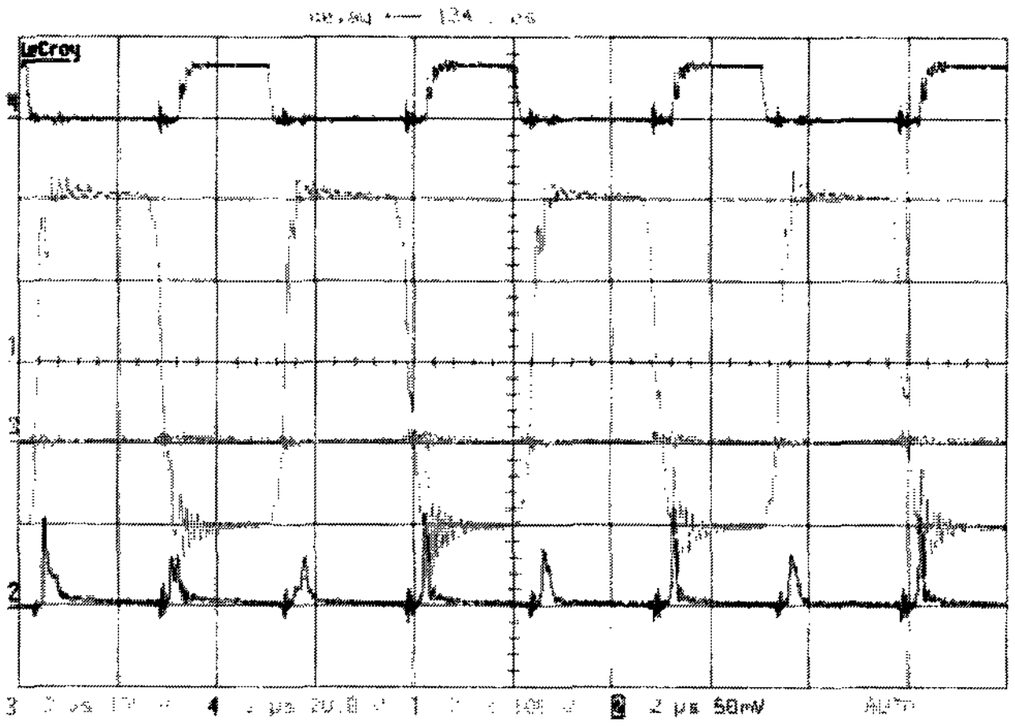


(b) Negative reset voltage waveform

Fig. 9 Reset voltage waveform made by the proposed PDP driver (CH1 : V_{CP}, CH2: light wave, CH3: V_X)



(a) Discharge with V_B



(b) Discharge without V_B

Fig. 10 V_{CP} and light waveform during the sustain period (CH1: V_{CP}, CH2: light waveform, CH4:V_{G_SYG})

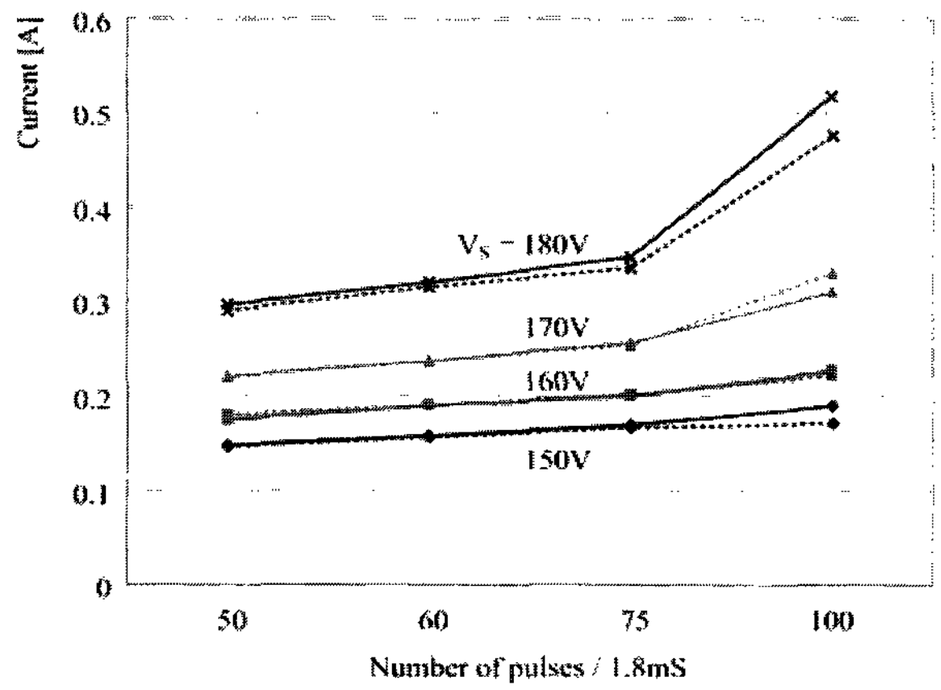


Fig. 11 Input current comparison (dotted line: previous work, solid line: proposed work)

circuit and two reset algorithms are suggested. The transformer replaces the resonant capacitor and reduces the clamping diodes. Therefore, the circuit structure is simplified and the number of devices is reduced. The propriety of the proposed PDP driver is verified through the experimental results of the prototype.

Acknowledgment

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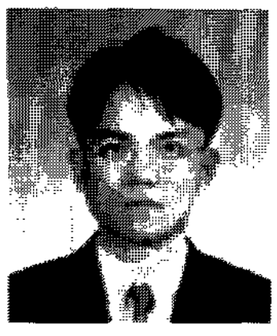

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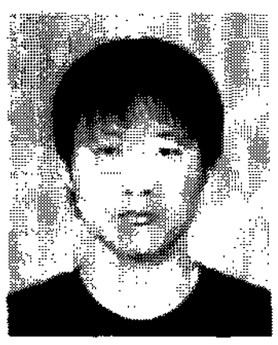

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