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루프 대역폭 조절기를 이용한 빠른 위상 고정 시간을 갖는 이중 루프 위상고정루프

(A Fast Locking Dual-Loop PLL with Adaptive Bandwidth Scheme)

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요 약

본 논문에서는 루프 대역폭을 조절하여 빠른 위상 고정 시간을 갖는 새로운 구조의 이중 루프 위상고정루프를 제안하였다. 위상고정루프가 out-lock 상태일 때는 채널 간격의 1/10보다 더 큰 대역폭을 갖도록 하였으며, in-lock 부근에서는 채널 간격의 1/10 보다 더 작은 좁은 대역폭을 갖도록 하였다. 제안된 위상고정루프는 표준 CMOS 0.35㎛ 공정으로 HSPICE를 이용하여 설계 하였다. 시뮬레이션 결과 PLL의 대역폭을 200KHz 채널 간격 보다 14배 크게 하여 80MHz의 주파수를 변화시키는데 50㎲의 빠른 위상고정 시간을 갖는 것으로 나타났다.

Abstract

A novel fast locking dual-loop integer-N phase locked loop (PLL) with adaptive bandwidth scheme is presented. When the PLL is out-of-lock, bandwidth becomes much wider than 1/10 of channel spacing with the wide bandwidth loop. When the PLL is near in-lock, bandwidth becomes narrower than 1/10 of channel spacing with the narrow bandwidth loop. The proposed PLL is designed based on a 0.35μm CMOS process with a 3.3V supply voltage. Simulation results show the fast lock time of 50μs for an 80MHz frequency jump in a 200KHz channel spacing PLL with almost 14 times wider bandwidth than the channel spacing.

Keywords : Phase locked loop(PLL), dual-loop, fast locking, adaptive bandwidth.

Ⅰ. Introduction

PLL is a key component in wireless communication system frequency synthesizer. Fast locking time is becoming important due to the expected fast channel switching speed in the future wireless communication system. Integer-N PLLs, though simple without inherent spur, sacrifice their bandwidth of narrower than 1/10 of channel spacing for stable operation of PLL and lock time depending on the bandwidth. The lock time of integer-N PLL used in the narrow channel spacing communication system is long because the narrow channel spacing is used as the reference frequency. Various fast locking integer-N PLL architectures have been published but their bandwidths do not exceed 1/10 of the channel spacing[1~2] The PLL architectures with their bandwidth exceeding 1/10 of channel spacing have been studied [3~5]. In [3], the dual-loop PLL consisting of two conventional PLLs and a mixer is used to have a wider input frequency than the channel spacing. Therefore, it can have wider bandwidth than the channel spacing of 200KHz and achieves a locking time of 128μs for a 20.6MHz

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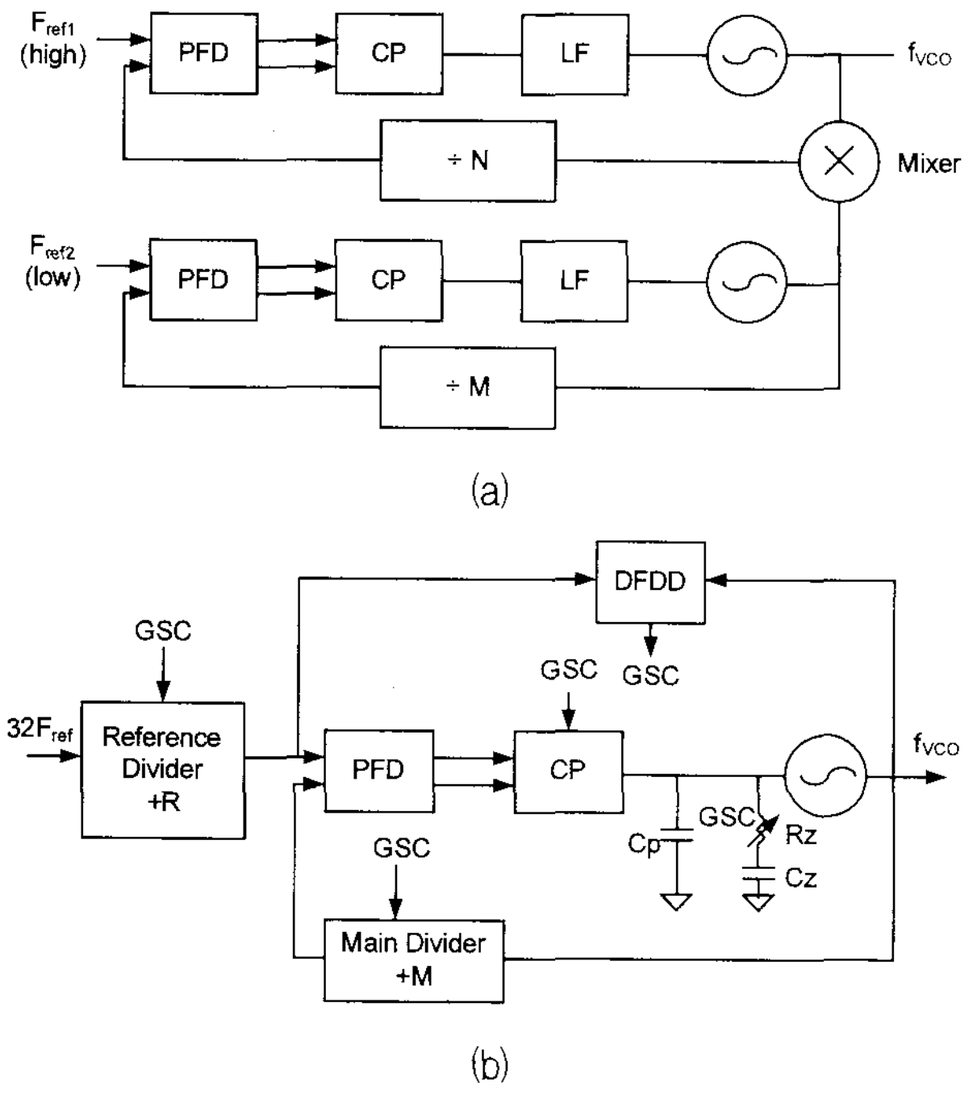

그림 1. 채널 간격 1/10을 초과하는 PLL 구조. (a) 두 개의 PLL과 믹서로 구성된 dual PLL. (b) Gearshift adaptive PLL

Fig. 1. Block diagram of PLLs exceeding 1/10 of the channel spacing. (a) Dual PLL consisted of two PLLs and a mixer. (b) Gearshift adaptive PLL.

frequency jump. However, its complicated architecture requires two PLLs and a mixer as shown in Fig. 1(a). In [4], its bandwidth exceeds 1/10 of the channel spacing of 200KHz according to locking status. The frequency of two input signals to the phase frequency detector gearshifts according to locking status, and then the bandwidth also gearshifts exceeding 1/10 of channel spacing as shown in Fig. 1(b). It requires a complicate gearshift signal generator, and also the lock of phase/frequency at every gearshift step causing a locking time of 228μs for an 80MHz frequency jump. In [5], a hybrid PLL that operates in a narrow-bandwidth integer-N mode during phase lock and in a wide-bandwidth fractional-N mode during transient has been proposed. Its locking time is 20μs for a 64MHz frequency jump at the channel spacing of 1MHz with an additional fractional divider.

In this paper, a novel fast locking dual-loop integer-N PLL with adaptive bandwidth scheme is presented. The proposed PLL is based on two loops: the wide and narrow bandwidth loops. For fast lock, the wide bandwidth loop is used to accelerate locking process, and the narrow bandwidth loop is used to generate the output frequency, N times of channel spacing. The operating principle of the proposed PLL is shown in Section II, The circuit design and simulation results are shown Section III and IV, respectively. Conclusions are given in Section V.

II. Proposed Dual-Loop PLL architecture

Bandwidth of PLL should be wide to reduce locking time but narrower than 1/10 of channel spacing for stable operation of PLL. It means that the channel spacing determines the fastest locking time as shown in Eq. 1[5].

$$t_{lock} = \frac{-2}{BW} \ln\left(\frac{f_{accuracy}}{f_{jump}}\sqrt{1-\zeta^2}\right) \quad (1)$$

where BW is bandwidth, $f_{accuracy}$ is frequency accuracy, f_{jump} is frequency jump and ζ is damping factor. A PLL architecture with wide bandwidth exceeding 1/10 of channel spacing is crucial to make a fast locking integer-N PLL. It should be simple to reduce size and power consumption, and stable while operating. Fig. 2 shows the proposed dual-loop PLL architecture consisting of two phase frequency detectors (PFD) and charge pumps (CP), a divider, a locking status indicator (LSI), a loop filter (LF) and a voltage controlled oscillator (VCO). It makes its bandwidth exceed 1/10 of channel spacing during

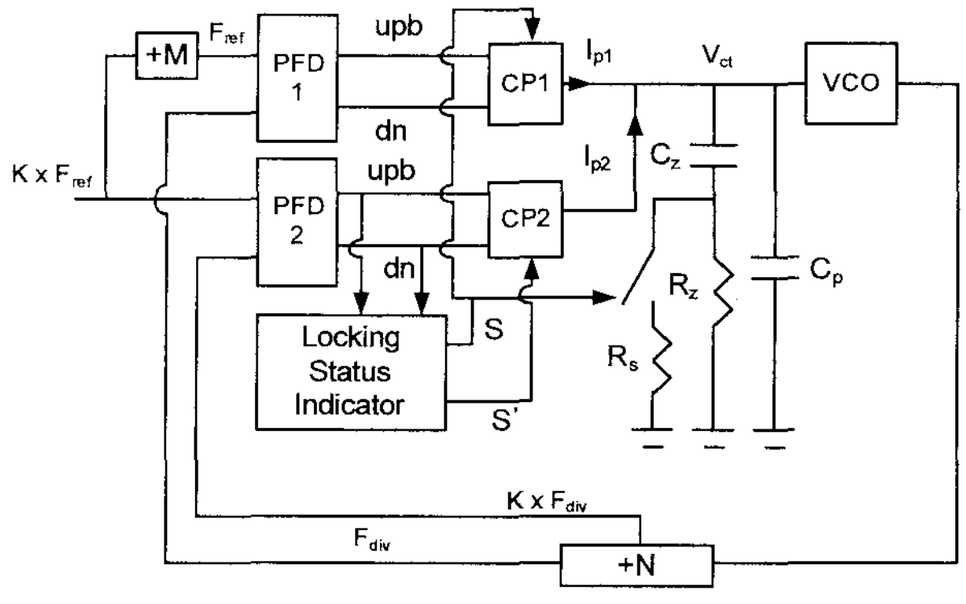

그림 2. 제안된 PLL의 구조

Fig. 2. Proposed architecture of PLL.

locking process. LSI generates signals to control the "on/off" of CPs and the resistance of LF depending on locking status. Input signals of low frequency loop to PFD1 are F_{ref} and F_{div}, where F_{ref} and F_{div} are the channel spacing and divider output. Input signals of high frequency loop to PFD2 are $K \times F_{ref}$ and $K \times F_{div}$, where K is an integer multiple number. The $K \times F_{div}$ is the signal bypassed before divided by K at the divider.

When the PLL is out-of-lock, LSI signal makes bandwidth wide with the loop of PFD2, CP2 and LF having low resistance while CP1 is off. Locking of high frequency signal accelerates in a short time while resulting in near in-lock of low frequency signal as shown in Fig. 3(a). The transfer function of wide bandwidth loop is as follows

$$H_o(s) = \frac{I_{p2}}{2\pi} \cdot \frac{K_{vco}}{s} \cdot \frac{1 + sC_z(R_z // R_s)}{s^2 C_p C_z (R_z // R_s) + s(C_p + C_z)} \cdot \frac{1}{N} \quad (2)$$

When the PLL is near in-lock, LSI changes its signal to make bandwidth narrow with the loop of PFD1, CP1, LF having large resistance while CP2 is off. Locking of low frequency signal occurs as shown in Fig. 3(b). The transfer function of narrow bandwidth loop is as follows

$$H_o(s) = \frac{I_{p1}}{2\pi} \cdot \frac{K_{vco}}{s} \cdot \frac{1 + sC_z R_z}{s^2 C_p C_z R_z + s(C_p + C_z)} \cdot \frac{1}{N} \quad (3)$$

Locking time consists of two parts, fast and slow locking time of wide and narrow bandwidth loops, respectively. The proposed dual-loop architecture makes it possible move from wide bandwidth loop to narrow bandwidth loop smoothly in one time without requiring the several locks of frequency/phase at each step of gearshift.

III. Circuit Design

LSI in Fig. 4 generates signals according to locking status. LSI block consists of a NOR gate, an inverter, a capacitor, and Schmitt trigger. When the PLL is out-of lock, the longer "Low" output signal of NOR gate increases V_a. When the PLL is near in-lock, on the contrary, it decreases V_a. During the transition, Va can be fluctuated due to the irregular pulse period of NOR gate output. With Schmitt trigger, the stable signal S from LSI can be generated. The timing of signal S can be controlled easily by sizing the PMOS and NMOS in inverter,

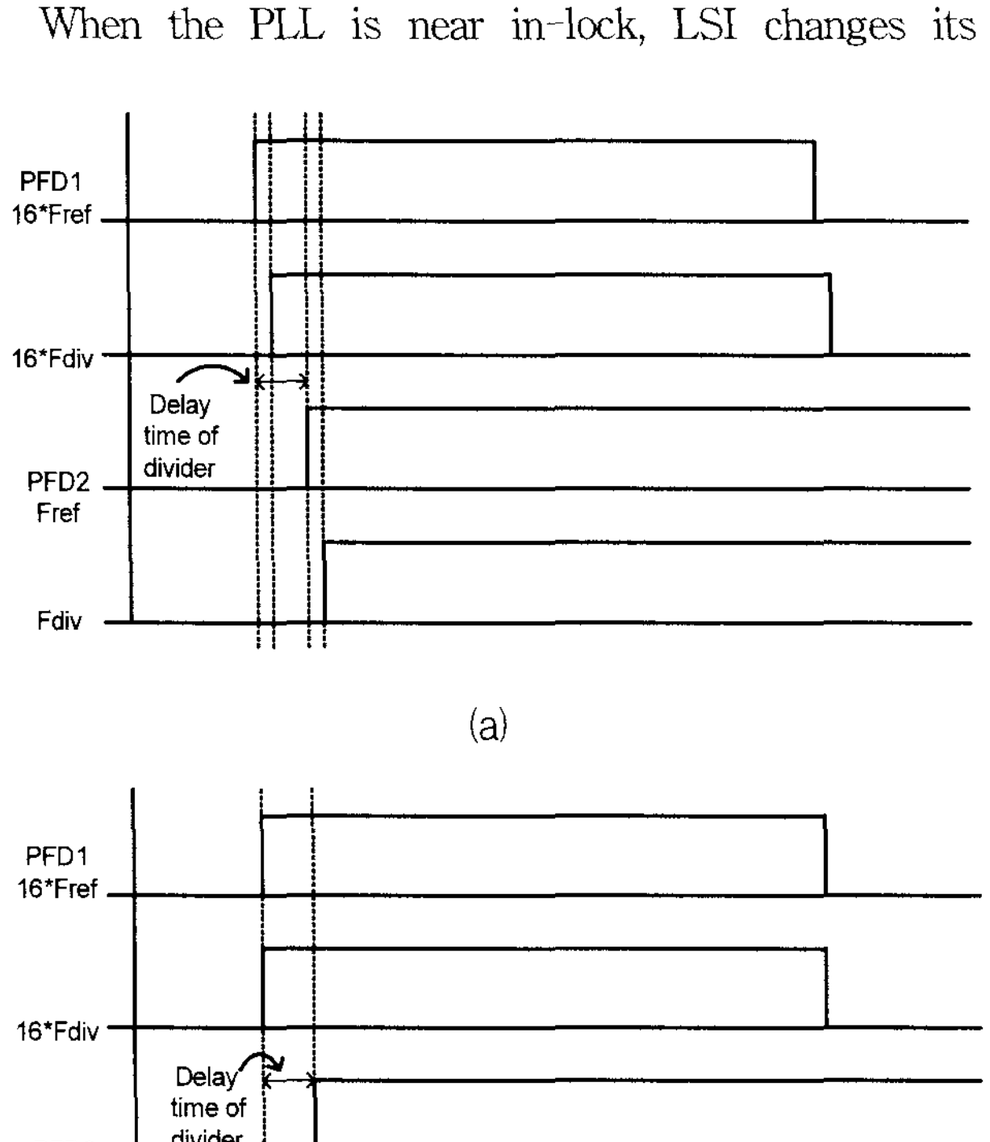

그림 3. 신호들의 고정 상태
(a) out-of-lock 상태의 끝부분 (b) in-lock 상태

Fig. 3. Locking status of signals. (a) At the end of out-of-lock status. (b) In-lock status.

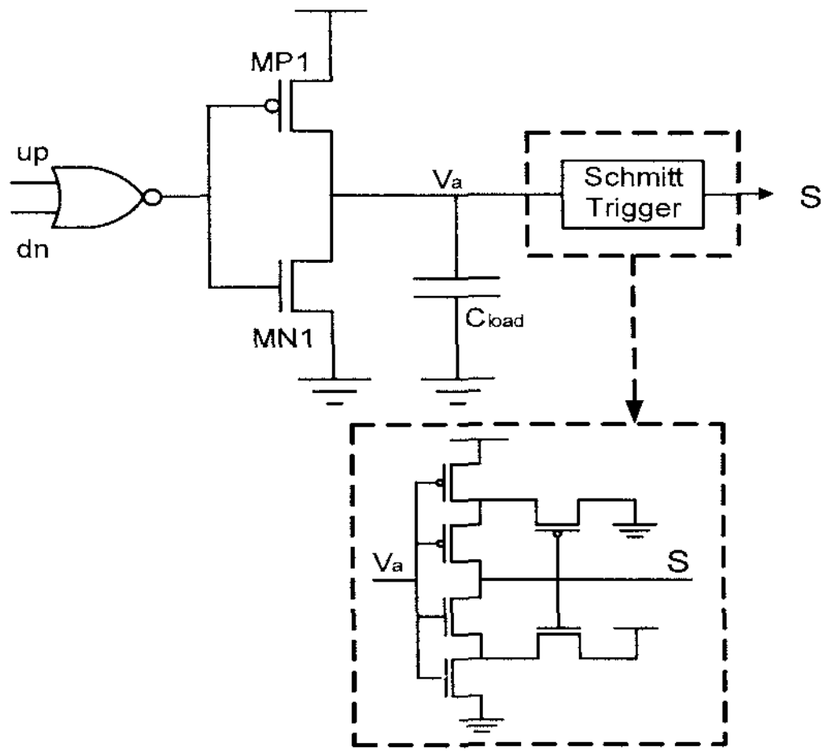

그림 4. LSI 블록과 슈미트 트리거

Fig. 4. LSI block & Schmitt trigger.

and the capacitor.

The voltage controlled resistor (VCR) is used to control the delay time of the VCO as shown in Fig. 5. The LF output voltage, V_{ctrl}, is converted into a current used for controlling the delay time of VCO through VCR. The VCR converts its input voltage variation into a large current variation and then it can generate a wide range of VCO frequency. The VCO is made of 3 differential delay cells which have full output voltage swing and low output phase noise.

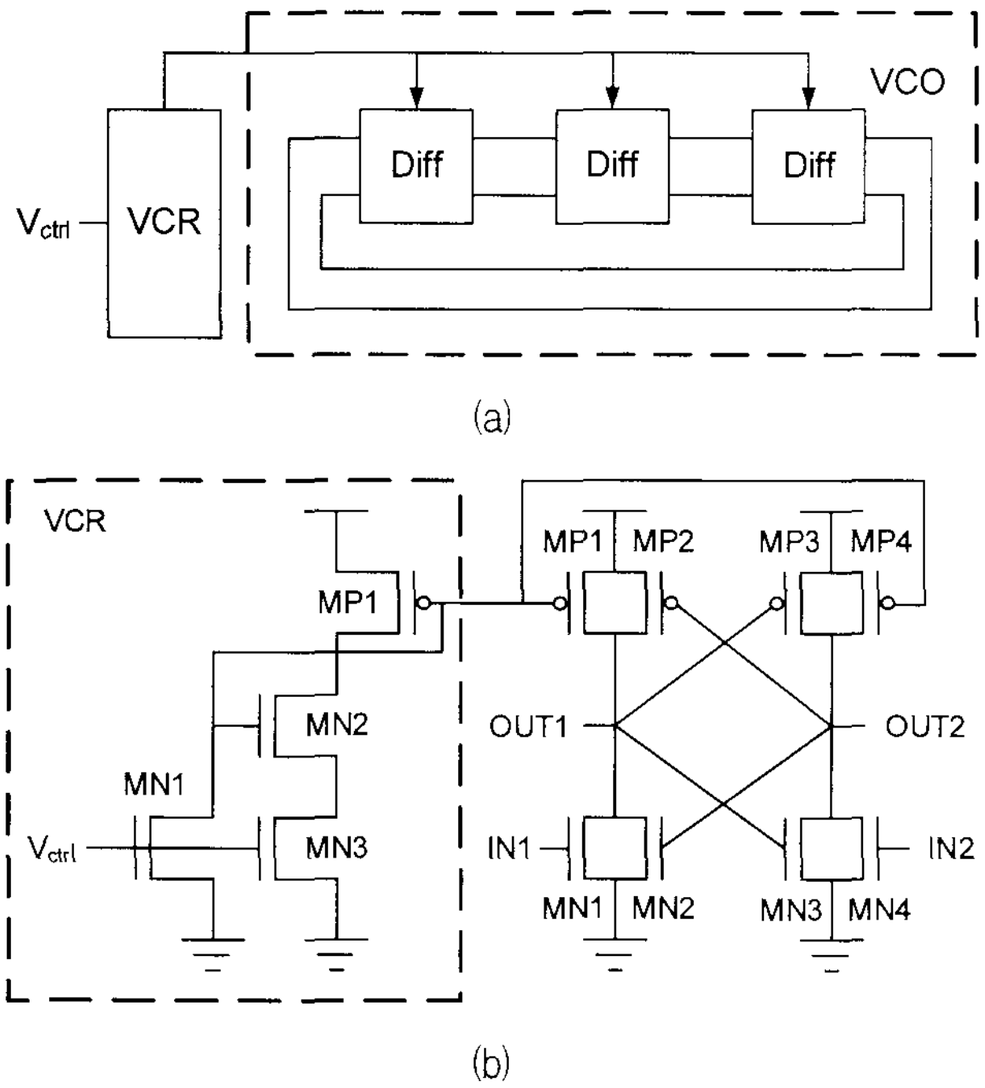

그림 5. (a) VCO의 블록도 (b) VCO의 VCR과 지연셀 회로

Fig. 5. (a) Block diagram of VCO. (b) Circuits of VCR and delay cell of VCO.

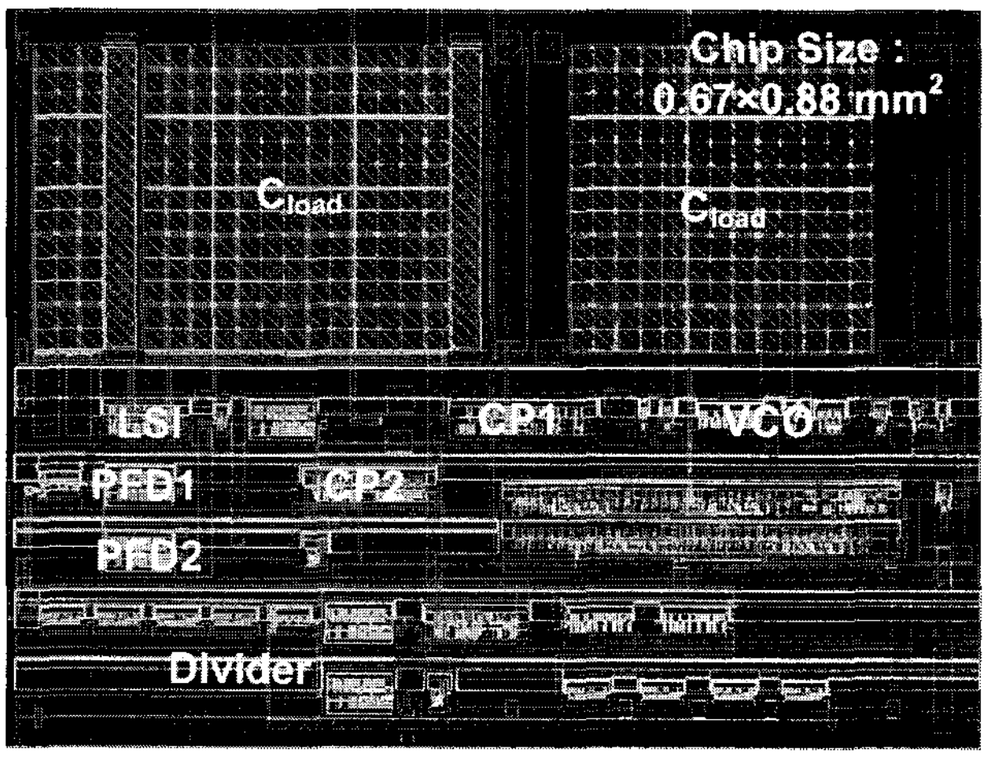

그림 6. 제안된 PLL의 레이아웃

Fig. 6. Proposed PLL Layout.

A pair of PMOS and NMOS transistors, MP2 and MP3, MN2 and MN3, respectively, is added to the delay cell to constitute CMOS latches. These latches makes the delay cells have short on-time for which to exhibit low output phase noise. MP1 and MP4 connected to the VCR control the driving current in the delay cell.

Fig. 6 shows the layout of the proposed PLL. Its size is 0.67x0.88mm^2 without capacitors and resistor of LF.

Ⅳ. Simulation results

Fig. 7 shows the simulation results of VCO input voltage with LSI signal S at K=4, 8 and 16. The number of N changes from 4096 to 4496 at 100μs for 80MHz frequency jump. The parameters used in simulation are 200KHz as a F_{ref}, N=4096/4496 and VCO gain of 137MHz/V. LF is made of 4 KΩ and 1K Ω resistors, 4nF of C_z and 500pF of C_p. The current of CPs are I_{p1}=600uA and I_{p2}=5mA. Table 1 shows the bandwidth and locking time of the proposed PLL in response to the 80MHz frequency jump with F_{ref} of 200KHz. The signal S showing only one time status change demonstrates the smooth transition from out-of-lock status to in-lock status. Even though there is a slight difference in phase and frequency of low frequency signal as shown in Fig. 3 (a), the locking time of narrow bandwidth loop is longer than that of wide bandwidth loop as shown in Fig. 7 (d).

When the PLL is out-of-lock, many cycles of K x F_{ref} (equivalent to 29-20μs in time) are required to make the PLL near in-lock status but its portion in total lock time becoming small as K increases. The 6

표 1. N=4496 상태에서 제안된 PLL의 대역폭과 위상 고정시간

Table 1. Bandwidth and locking time of the proposed PLL at N=4496.

	Bandwidth(kHz)	Locking Time(μs)
	Out-of-lock / in-lock	Out-of-lock / in-lock = Total Locking Time
K=4	77.8 / 16.07	29 / 35 = 64
K=8	148 / 18.94	23 / 30 = 53
K=16	271 / 19.58	20 / 30 = 50

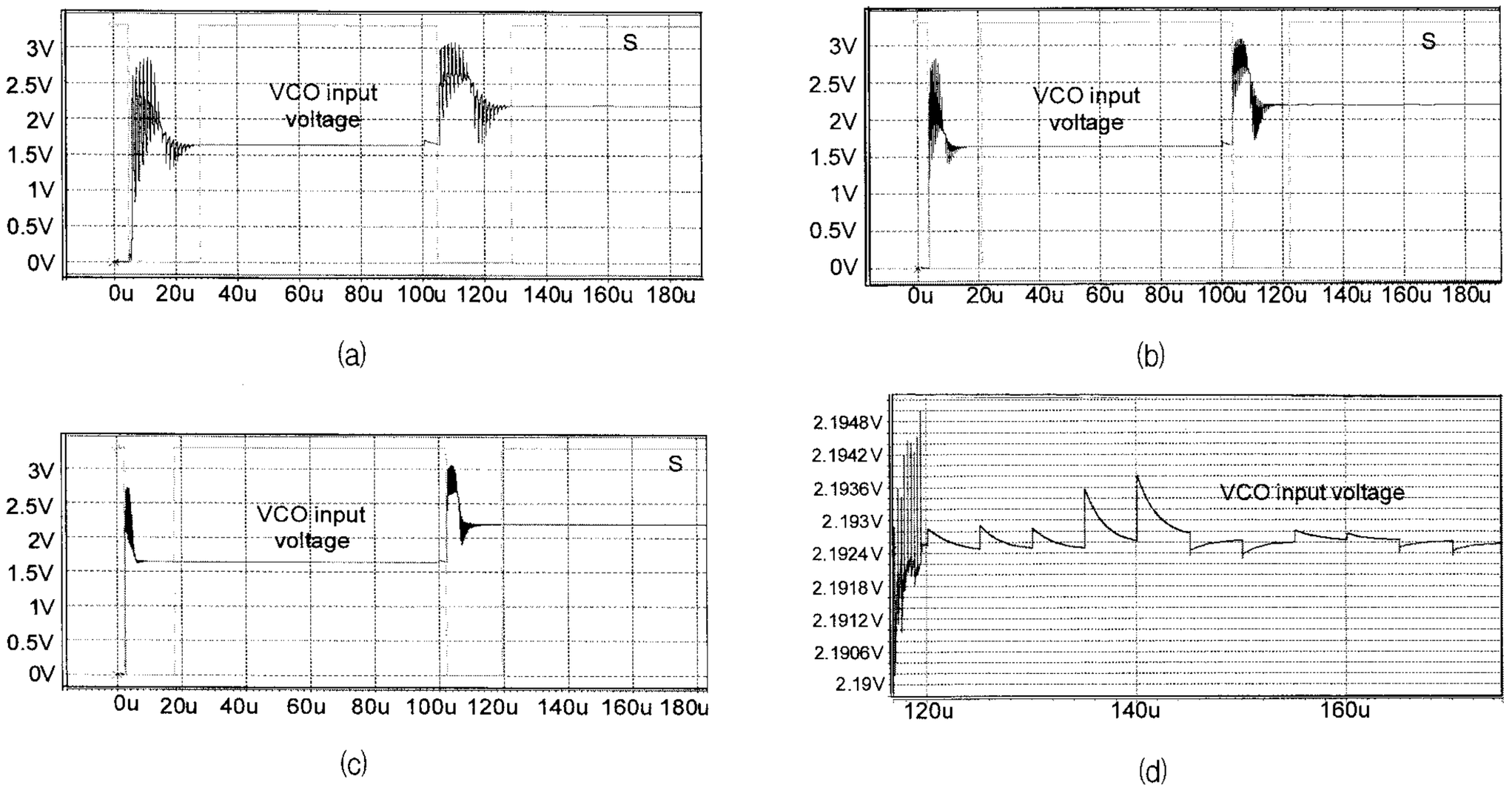

그림 7. VCO 입력 전압의 시뮬레이션 결과 (a) K=4 일때 VCO의 입력전압. (b) K=8 일때 VCO의 입력 전압 (c) K=16 일때 VCO의 입력 전압 (d) K=16일때 VCO 입력 전압의 확대 그림

Fig. 7. Simulation results of VCO input voltage. (a) VCO input voltage at K=4. (b) VCO input voltage at K=8. (c) VCO input voltage at K=16. (d) Enlarged VCO input voltage at K=16.

or 7 cycles of F_{ref} are required to make the PLL in-lock status but it takes a long locking time due to the comparing time step of 5μs with its 200KHz of F_{ref}. Although faster locking time can be obtained by increasing the number of K, the maximum number of 16 is determined because the total locking time can't be much further reduced due to the relative long locking time of narrow bandwidth loop.

V. Conclusion

A novel fast locking dual-loop integer-N PLL with adaptive bandwidth scheme is presented in this paper. When the PLL is out-lock, bandwidth becomes much wider than 1/10 of channel spacing with the wide bandwidth loop. When the PLL is near in-lock, bandwidth becomes narrower than 1/10 of channel spacing with the narrow bandwidth loop. The wide and narrow bandwidth loop accelerates locking process and generates the output frequency, N times of channel spacing, respectively. Simulation results show the fast locking time of 50μs for an 80MHz frequency jump in a 200KHz channel spacing PLL with almost 14 times wider bandwidth than the channel spacing. Compared with the gearshift PLL of 228μs locking time for an 80MHz frequency jump, and dual-loop PLL of 128μs locking time for a 20.6MHz frequency jump, the proposed PLL achieves the much smaller locking time of 50μs.

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