論 文
57-6-11

Voltage-Stacking Cell을 이용한 고이득 부스트 컨버터

A High-Gain Boost Converter using Voltage-Stacking Cell

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Abstract - This paper suggests anon-isolated high-gain boost converter using voltage-stacking cell. The voltage gain can be increased by adjusting number of voltage-stacking cells and transformer turns-ratio. Test results with 1kW prototype converter show that the voltage gain is three or four times higher than conventional boost converter at unity transformer turns-ratio and about 90% of efficiency is recorded under full load condition.

Key Words : Fuel-cell, Boost converter, DC/DC converter

1. Introduction

Fuel-cells are clean and efficient energy sources that are promising in a near future. They can be an alternative energy source of electrically powered devices such as transportation, communication, computing, and residential systems[1]. Fuel-cells produce low voltages so the input voltages and currents can easily have same order of magnitude in kilowatts applications. Thus, it is necessary to design a step-up converter to interface the fuel-cell to various loads[2]. Two types of converter topologies can be used for boost operation, isolated and non-isolated converter. The isolated converter produces a high voltage gain but they have disadvantages in view of size and cost. Recently, the non-isolated converters have been considered to reduce the size and cost of power conversion units in applications where electrical isolation is not required. The voltage gain is too high to use the conventional boost converter so several approaches have been proposed to increase the voltage gain[3]. However, most of them require many switch blocks, which results in cost increase or reliability degradation. In this paper, a non-isolated high-gain boost converter using voltage-stacking cell is proposed. The voltage-stacking cell provides another power path to increase the voltage gain. From the circuit analysis, the input-to-output relationship is derived as the function of number of voltage-stacking cells and transformer parameters. Based on this relationship, the proposed converter has been designed and verified.

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接受日字 : 2008年 3月 11日
最終完了 : 2008年 5月 19日

2. Proposed method

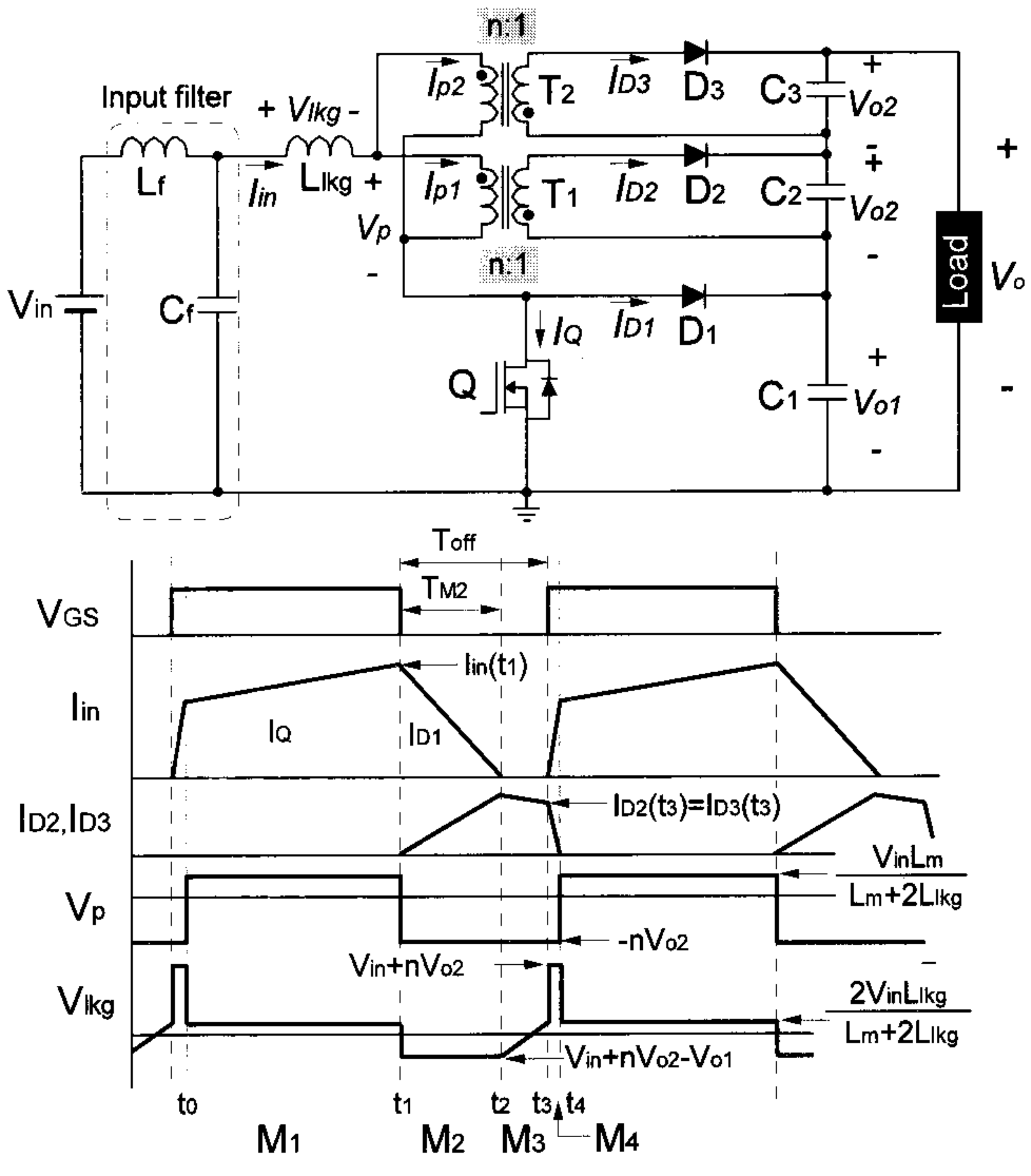

그림 1 제안된 회로와 주요 동작 파형
Fig. 1 Proposed circuit and its key waveforms

Fig. 1 is the proposed circuit and the key waveforms are depicted together in this figure. Each voltage-stacking cell has similar structure with flyback converter. The proposed circuit has two voltage-stacking cells and can be expanded to N cells if needed. Q and D_1 are elements for boost converter that transfers one part of input energy to the output and absorbs the leakage inductance energy. Total leakage inductances of transformers T_1 and T_2 are depicted as L_{lkg}, which is half value of transformer leakage inductance. L_f and C_f are for preventing input source from large pulsating currents. Before mode analysis T_1 and T_2 are assumed to be identical. The mode diagrams of the proposed method are shown in Fig. 2.

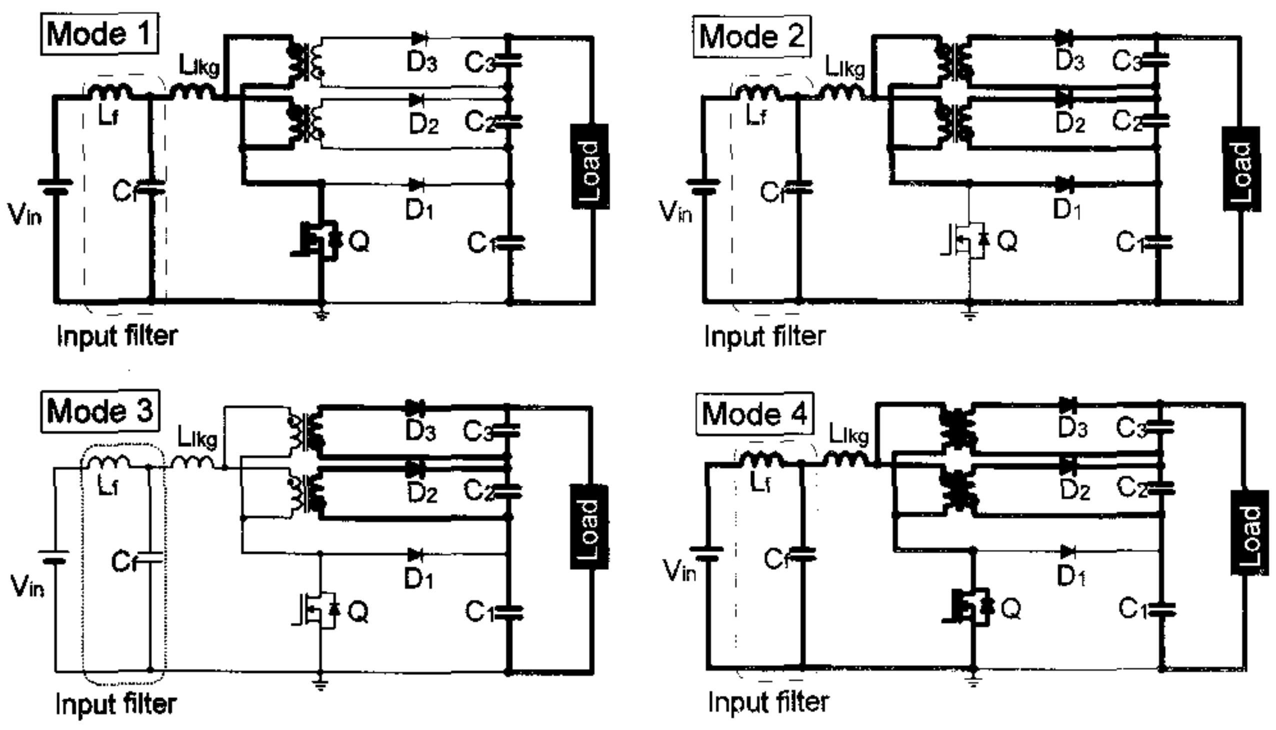

그림 2 동작 모드 다이어그램

Fig. 2 Operational mode diagrams

Mode 1 begins at to when Q is turned on. The input current of I_{in} flows through both transformer primary sides and Q. The diodes of D_1, D_2, and D_3 are blocked because the cathode voltages are higher than the anode voltages. During this mode, energies are stored in L_{lkg} and transformers, and I_{in} is increased with the slope of $V_{in}/(L_{lkg}+L_m/2)$, where L_m is the primary inductance of transformer. When Q is turned off, I_{in} starts to flow through D_1 and the stored energies of T_1 and T_2 are transferred to the output capacitors of C_2 and C_3 through D_2 and D_3. During mode 2, I_{in} ramps down with the slope of $(V_{in}+nV_{o2}-V_{o1})/L_{lkg}$. I_{D2} and I_{D3} are increased with the slope of $n(V_{o1}-V_{in}-nV_{o2})/2L_{lkg}$ because Iin flows through T_1 and T_2, evenly divided by half. After I_{in} decreased to zero at t_2, I_{D2} and I_{D3} stops increasing and starts to flow with the slope of $-n^2V_{o2}/L_m$. When Q turns on again, V_{lkg} changes to $V_{in}+nV_{o2}$ and I_{D2} and I_{D3} starts to decrease until zero with the slope of $-n(V_{in}+nV_{o2})/2L_{lkg}$. The duration of mode 2, T_{M2} is essential parameter for deriving input-to-output relationship and it can be obtained by assuming that L_m is so large that the current slopes of I_Q and $I_{D2}(=I_{D3})$ during modes 1 and 3 are neglected and the duration of mode 4 is also neglected due to fast transition. Then $I_{in}(t_1)$ is approximately equal to $2I_{D2}(t_3)/n$. Also, I_{D1}, I_{D2}, and I_{D3} are charging currents of the output capacitors and they should have a same value in steady state because all of the output capacitors supply same load current. From these conditions, the following equation can be obtained.

$$\frac{1}{2}I_{D2}(t_3)T_{M2}+(T_{off}-T_{M2})I_{D2}(t_3)=\frac{1}{2}\times\frac{2I_{D2}(t_3)}{n}\times T_{M2} \quad (1)$$

The solution of eq. (1) provides that T_{M2} is $2T_{off}/(2n+1)$.

3. Input-to-output relationship

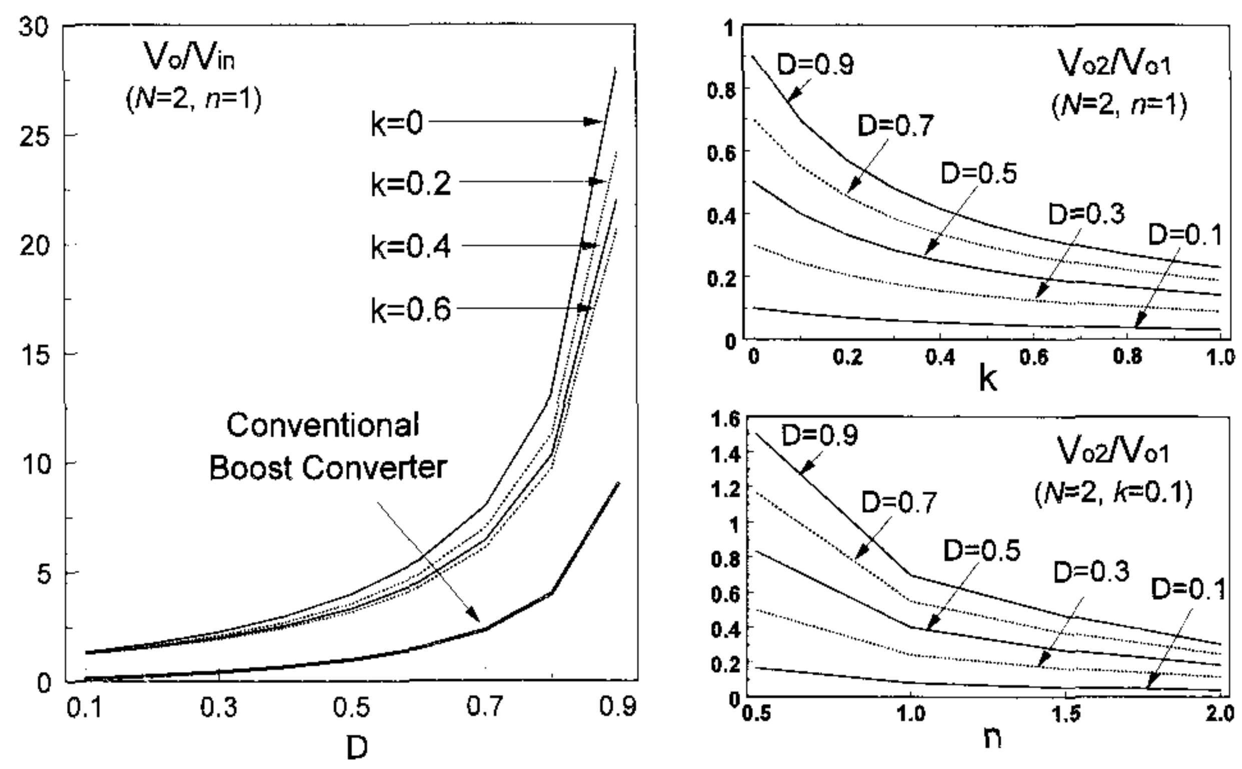

그림 3 듀티비와 변압기 파라미터에 따른 입출력 전달비

Fig. 3 Input-to-output transfer-ratio according to duty ratio and transformer parameters

The input-to-output relationship can be obtained by applying volt-sec balance conditions to both transformer and leakage inductances. By neglecting the small transition time of mode 4, the volt-sec balance conditions of transformer and leakage inductance can be written as eqs. (2) and (3) respectively.

$$D\left(V_{in}\frac{L_m}{L_m+2L_{lkg}}\right)=n(1-D)V_{o2} \quad (2)$$

$$D\left(V_{in}\frac{2L_{lkg}}{L_m+2L_{lkg}}\right)=\frac{2}{2n+1}(1-D)(V_{o1}-V_{in}-nV_{o2}) \quad (3)$$

where D is duty ratio. In eq. (3), the factor of $2/(2n+1)$ is result from the fact that the current flowing in leakage inductance is reduced to zero during T_{M2}. Therefore the input-to-output relationship is

$$V_o=V_{o1}+2V_{o2}=V_{in}\left(1+\frac{D}{1-D}\frac{(1+2/n)L_m+(2n+1)L_{lkg}}{L_m+2L_{lkg}}\right) \quad (4)$$

This relationship can be generalized as eq. (5) with N voltage-stacking cells.

$$V_o=V_{o1}+NV_{o2}=V_{in}\left(1+\frac{D}{1-D}\frac{(1+N/n)L_m+(2n+1)L_{lkg}}{L_m+NL_{lkg}}\right) \quad (5)$$

From eq. (4), input-to-output transfer-ratio is plotted in Fig. 3 according to duty ratio, $k(\equiv L_{lkg}/L_m)$, and n. This plot shows that the proposed converter has higher gain than general boost converter and can be operated in wide input range. The gain is somewhat affected by the leakage inductance and the amount of energies transferred through voltage-stacking cells is increased as the leakage inductance becomes decreased. V_{o1} affects the voltage stress of main switch so that excessive voltage stress and switching loss of switch can be alleviated through proper design of n.

4. Experimental results

The proposed circuit has been designed with 1kW(400V/2.5A) and 20kHz switching frequency at V_{in}=50V. Considering the current stress at full load condition, the maximum duty has been selected as 0.7. To reduce the switching loss of switch, the voltage stress has been limited under 190V. This condition gives V_{o2}/V_{o1} is 0.55 and n becomes determined as 1. The transformers are implemented with PQ5050 core(48T:48T), whose primary and leakage inductances are 300μH and 10 μH, respectively. Four FDP46N30's are used for switch in parallel and FES16J's are used for diodes.

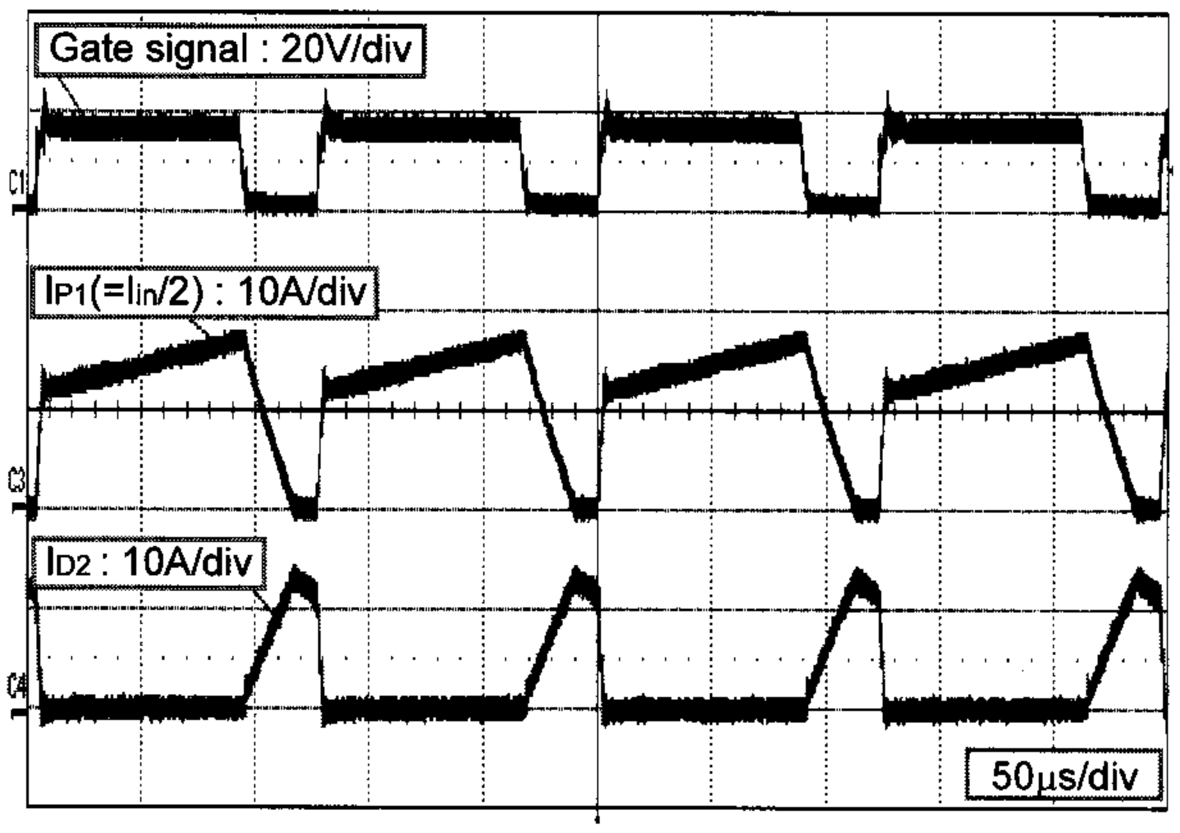

그림 4 전부하조건에서 측정된 스위칭 파형

Fig. 4 Measured switching waveforms under full load condition

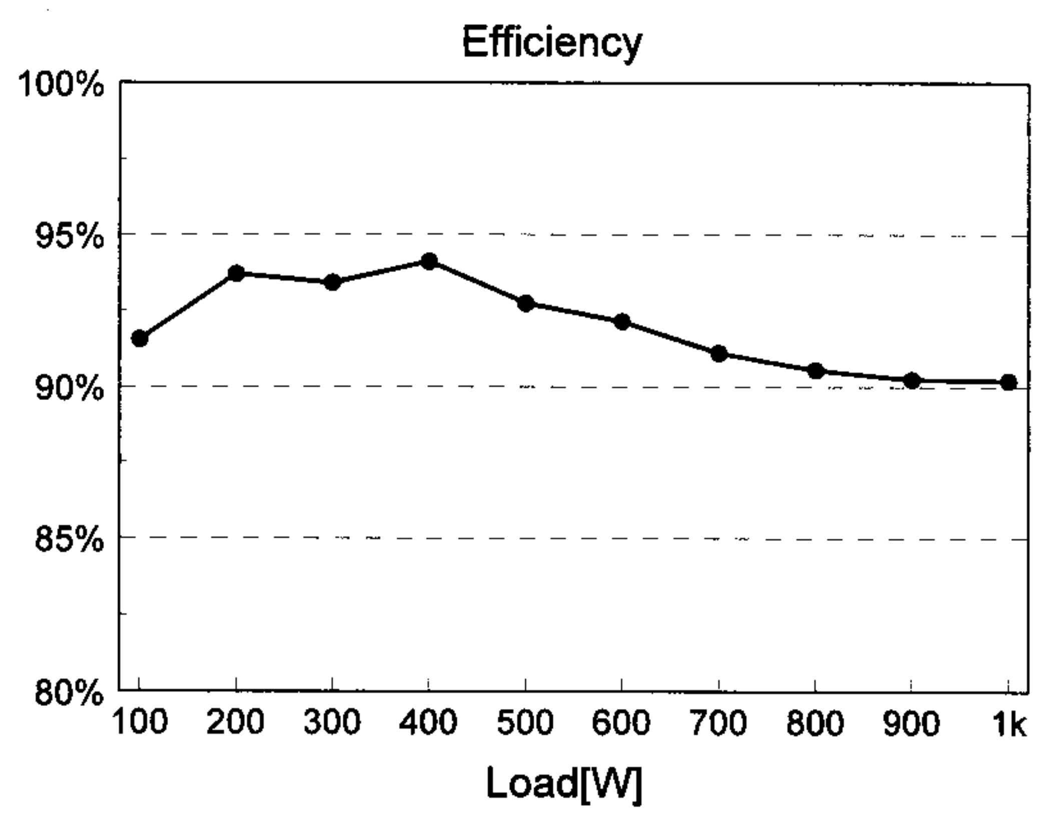

그림 5 부하에 따른 효율

Fig. 5 Efficiency plot under load changes

Figs. 4 and 5 are the measured switching waveforms under full load condition and efficiency plot. The measured waveforms are well agreed with theoretical analysis and the time taking for I_{in} to be reduced from peak to zero is approximately $2T_{off}/3$. The efficiency is about 90% at full load condition using WT210(Yokogawa co.) power meter 3255(Prodigit co.) electric load and the minimum operating voltage of input source is measured about 23V.

5. Conclusions

A high-gain boost converter using voltage-stacking cell is proposed and analyzed in this letter. Its input-to-output relationship can be derived as the function of number of voltage-stacking cells and transformer parameters from the circuit analysis. To verify the performances, a 1kW prototype converter has been implemented based on the input-to-output relationship equation and its transformers were designed to reduce the switch voltage stress considering efficiency. Experimental results show that the voltage gain can be obtained three or four times higher than conventional boost converter and about 90% of efficiency is measured under full load condition.

Acknowledgement

The research work described in this paper was supported by the Advanced Human Resource Development Program of MOCIE (Ministry of Commerce, Industry, and Energy) through the Research Center for Intelligent Micro-Grid in Myongji University.

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