DOI: 10.3745/KIPSTA.2008.15-A.4.211

NMOSFET의 제조를 위한 습식산화막과 질화산화막 특성에 관한 연구

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요 약

본 논문에서는 핫 케리어 효과, 항복전압 전하, 트랜지스터 Id Vg 특성곡선, 전하 트래핑, SILC와 같은 특성들을 비교하기 위하여 HP 4145 디바이스 테스터를 사용하여 습식 산화막과 질화 산화막으로된 0.26㎛ NMOSFET를 만들어 측정하였다. 그 결과 질화 산화막으로 만들어진 디바이스가 핫 케리어 수명(질화 산화막은 30년 이상인 반면에 습식 산화막 소자는 0.1년임), Vg의 변화, 항복전압, 전계 시뮬레이션, 전하 트래핑 면에서도 습식 산화막 소자보다 우수한 결과를 얻을 수 있었다.

키워드 : 핫 케리어

A Study on Characteristics of Wet Oxide Gate and Nitride Oxide Gate for Fabrication of NMOSFET

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ABSTRACT

In this paper we fabricated and measured the 0.26㎛ NMOSFET with wet gate oxide and nitride oxide gate to compare that the charateristics of hot carrier effect, charge to breakdown, transistor Id_Vg curve, charge trapping, and SILC(Stress Induced Leakage Current) using the HP4145 device tester. As a result we find that the characteristics of nitride oxide gate device better than wet gate oxide device, especially hot carrier lifetime(nitride oxide gate device satisfied 30 years, but the lifetime of wet gate oxide was only 0.1 year), variation of Vg, charge to breakdown, electric field simulation and charge trapping etc.

Keyword : Hot Carrier

1. Introduction

In spite of the dramatically advances in MOSFET device miniaturization during past decades, criteria of device optimization for reliability are not still well established. When the size of the device is decreased, the hot carrier degradation presents a severe problem for long-term device reliability[1]. The degradation of device performance arising from hot carrier effects can be suppressed by various methods. Most involve modifying the conventional MOSFET structure or strengthening the gate oxide and the Si-SiO_2 interface against hot carrier damage[2].

The fabricated device has W/L=15/0.26㎛NMOSFET, shallow trench isolation, 7.0nm wet and/or nitride gate oxide.

2. Method and Simulation

2.1 Hot carrier effect

The scaling of device dimension and supply voltage with high performance and reliability has been the main subject in the evolution of VLSI technology. The scaling of device parameters such as channel length(Leff), oxide thickness(Tox), junction depth(Xj) and supply voltage(Vdd) results in the significant changes in performance and reliability characteristics of devices and circuits. Without scaling rules, it has been very difficult to satisfy complex requirement, hence, scaling theory has been introduced to

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논문접수 : 2008년 3월 12일
수 정 일 : 1차 2008년 5월 9일, 2차 2008년 5월 19일
심사완료 : 2008년 5월 19일

guideline the design of device parameters. The first scaling theory maintains the electric field constant, i.e. both horizontal and vertical dimensions and supply voltage are scaled by a factor S(S>1) in order to maintain constant electric field within MOSFET.

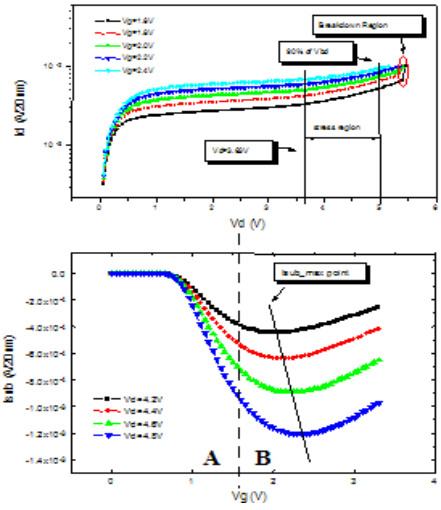
The MOSFET structures become susceptible to high field related reliability problems such as hot-electron induced device degradation and dielectric breakdown. As a solution to reduce the hot carriers, new hot-carrier resistant structures suchas the DDD(Double Diffused Drain) and LDD(Lightly Doped Drain) structures have been introduced. The LDD type structure has been successfully used in 4Mb, 16Mb, 64Mb, 256Mb DRAM devices with gate length 0.15~0.40㎛. However, even using LDD, it is difficult to achieve high reliability and high performance at a 5volt power supply. For this reason, power supply voltage reduced to under 5volt, for example, to 3.3volt.Up to this time, the selection of optimal power supply voltage was based on optimizing the trade off between operation speed and reliability. As VLSI technology continues to develop, however, we are now facing power consumption problems in today's potable high-end products. In fact, it seems that power consumption is the most important limitation to the today's battery operated VLSI chips. Furthermore, as the density and size of the chip and systems continue to increase, the difficulty in cooling adds a significant cost to the system or provides a limit on the amount of functionality[3]. An important point is that most important parameter controlling power consumption is the supply voltage[4]. The selection of optimal power supply voltage is now based on optimizing the trade off between operation speed and power consumption. Hence, the standard supply voltage should continue to decrease from 5volt to, 3.3, 2.5, 1.5volt, and finally to sub -1.5volt in the future battery operated systems. Device structures, device operation, and circuit design to obtain high speed under low supply voltage become more important.In order not to lose operation speed by reducing power supply voltage, threshold voltage should be reduced. The main subject in the low voltage, low power technology is scaling of device dimensions to deep submicron regime with high performance and good short channel immunity[5]. Hence, as the device dimension penetrates into the sub-0.1㎛ regime, the control of both threshold voltage and source drain punch through becomes the most important factors in designing low voltage/low power device.

As the MOS devices are scaled down, the channel doping concentration continuously increases to prevent the short channel effects, and it becomes very difficult to realize a low threshold voltage while maintaining a good control of short channel effects. This high channel doping leads to undesirable increased threshold voltage and parasitic junction capacitance[6]. The increase of threshold voltage and capacitance limits the performance of circuit at low voltage operation, and the advantage in delay time dueto reduction of channel length is diminished. To overcome this problems, it is very important to design a vertical doping profile of substratestructure, hence, the concept of substrate engineering was introduced[7].

To insure the circuit or product reliability in actual operating environment, a circuit simulation including the hot-carrier induced device degradation is essential. The accurate reliability simulation is a problem tightly coupled with investigation of physical mechanismsfor hot carrier, mathematical modeling of degradation behavior and implementation of the model into circuit simulator. Thus we performed hot carrier effect simulation for nMOS transistor[8].

2.2 Substrate current

In spite of the impressive advances in MOSFET device minimization during the last three decades, device optimization criteria for reliability are not still well established. The original equation for substrate current(ISUB) based on lucky electron model can model the substrate current properly[9]. However, the functional form of this formulation is inconvenient for device characterization and design. It is widely used a bell-shaped plot(Fig. 1.) to characterize the substrate current by plotting ISUB against gate voltage with drain electric field. voltage as a parameter. The initial rise is due to the increase of drain current and the fall is due to the decrease of channel



(Fig. 1) Isub_max extraction

The substrate current is result from holes generated by impact ionization, hence, it is a measure of hot electron currents in the channel. The original equations properly model the substrate currents and drain saturation voltage.

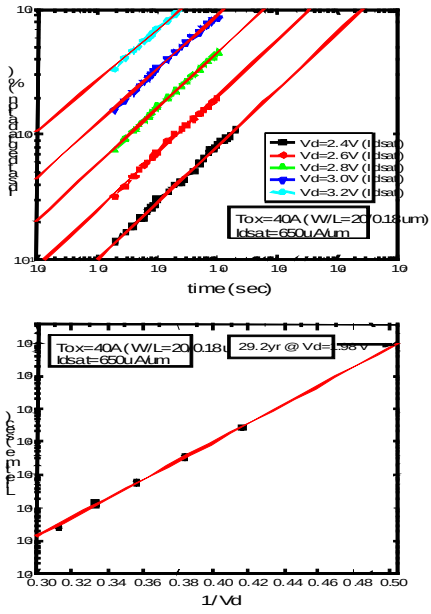
However, the functional form of these equations is inconvenient for design criteria. The minimization of substrate current and drain saturation voltage while maximizing drain saturation current isimportant in device design.

Hot carrier induced interface state generation is a major reliability concern for modern short channel nMOSFET's. Since this is one of the major problems for device scaling, there have been numerous papers. However, the exact time dependence of the degradation is not still well understood. As far as the authors know, the following simple power-law dependence on both stress time and substrate current is perhaps the only model which used to fit the empirical behavior of degradation.

$$\Delta = C\ (ISUB / In)m \ * (ID \ * t / W)n \qquad (1)$$

Here Δ represents the hot carrier induced degradation, which is the function of interface state density in the damaged region. In the equation, C is a proportional constant, W is the effective channel width, ISUB and ID are the substrate and drain current, m and n are the empirical parameters representing the power-low dependence on substrate current and on stress time, respectively[10].

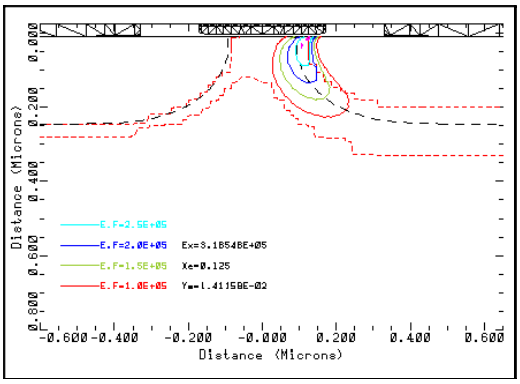
Ids vs. Vd curve used to extract 90% breakdown voltage in various drain voltage sweep. This condition is used to determine to evaluation transistor gate length. Next the gate voltage was determined to extract worst case stress condition. As above mentioned, ISUB_max extract method is used to extract worst H.C.E measurement condition. Normally, Vg is 40~50% for Vd. Finally, extract lifetime(τ : 10% degradation time of Idsat) from 1/Vds and Isub/W.



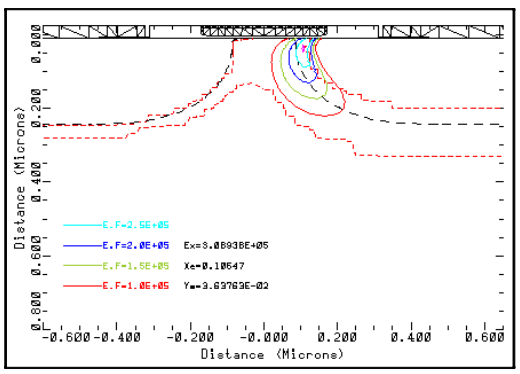
(Fig. 2) Life time extraction method

2.3 Simulation

The beneficial effects of including nitrogen in gate oxide well known. Advantages cited are an improvement to charge to breakdown, NFET hot electron immunity, and reduction of boron penetration. But, there are also major drawbacks to these process[11]. Growing the same oxide thickness with nitrogen-containing compounds may require a lager thermal budget. Nitridation reduces the low field electron mobility and generally introduces fixed positive charge. Oxynitrides have been pay attention due to their superior performance and reliability properties compared to conventional SiO_2. In particular, oxidation in N_2O ambient was found to be exceptionally attractive due to the absence of hydrogen(H) in the processing ambient, which is a potential source of electron traps if incorporated in the dielectric. (Fig. 3) shows the simulation of H.C.E electric field. Bias condition is Vd=2.5V, Vgs=1.0V, Vs=0.0V, Vb=-1.0V. The gate length is



(a) Simulation of WET_OX.



(b) Simulation of NIT_OX.

(Fig. 3) Hot carrier simulation

0.30㎛. As a result of simulation WET_OX Emax= 3.18MV/cm and NIT_OX Emax=3.07MV/cm. This result shows NIT_OX Emax is located in inner channel than Normal condition.

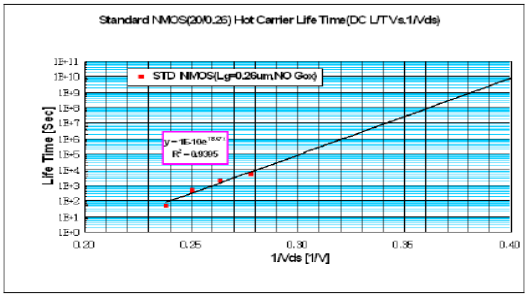
3. Experimental

Buffer oxide and SiN layer was deposited and etched the field area for active area definition. Trench etching was performed after thin SiN layer was etched. Filling the trench gap with HDP oxide, and densification at high temperature, then CMP was carried out for planarization. SiN and pad oxide were removed by wet etching. Channel ion implantation performed to control threshold voltage after HDP densification(1050℃). The fabrication process of MOSFETs was based on 0.26㎛ technology with 7.0nm wet and NO annealed oxide(fabricated by wafer split). The gate electrode was patterned by the KrF lithography. The following nLDD ion implantation carried out with As+P nLDD. The boron ions were implanted(tilt 30o) for forming self-aligned pocket profiles. Then 65nm Si3N4 sidewall spacer was formed and then deep source /drain implantation(As) was carried out. The final process was RTA annealing at 1000℃ for 10seconds(to activate arsenic ions).

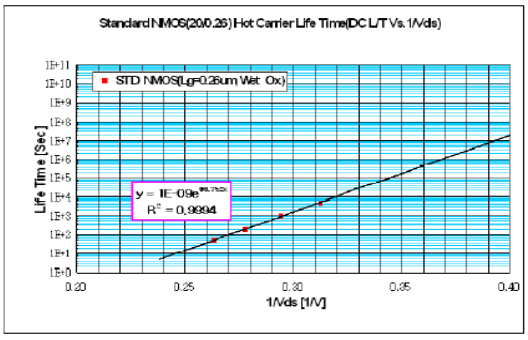
Also, p-type(100) oriented Si substrates with resistivities 0.1Ω were used to evalute the characteristics of oxide layer film. After growing thermal oxidation with 4000Å on p-type wafer, followed STI process and cleaning was carried out for isolate each device. Wet gate oxide formed with 800℃, 30min wet ambient whereas nitride oxide gate formed by additional annealing from 800℃ to 900℃ with 5% NO gas ambient after first gate oxidation (thickness=67Å). The N+ gate electrode was patterned by the KrF lithography to fabricated MOS capacitor.

4. Results

As the channel and oxide fields increase, hot carrier emission imposes serious limitations on the long-term reliability of scaled ULSI circuits. Studies of device degradation to date have been mostly based on channel hot carrier injection, which is very localized in nature. (Fig. 4) and (Fig. 5) shows the hot carrier lifetime of wet and NO oxidation devices. We can observed that processed NO heat thermal device lifetime was superior than wet oxidation. The hot carrier lifetime was 0.1 year with wet oxidation, and NO oxidation was 30 years. The existence of H_2O in gate oxides has also been found to increase their susceptibility to hot carrier degradation, for reasons closely related to those involving atomic hydrogen. The degradation is tend to be due to the diffusion of either H, OH, H_2 or H_2O. Such a Si-H bonds can easily be broken by big energy electrons and hot electrons or holes. However nitride oxide exhibit stronger resistance to interface state generation under hot carrier injection and provide a barrier to various dopants. The increased stability of the $Si-SiO_2$ interface is due to the file-up of nitrogen at the interfacial region. The nitride atoms are thought to terminate dangling Si bonds at the $Si-SiO_2$ interface. (Fig. 6) shows the result of thermal oxidation Qbd with 900℃, 30min heat treatment(5%, NO ambient) and wet oxidation. We can observed that there is no existence Qbd increment with NO heat treatment. (Fig. 7) shows the characteristics of gate voltage vs drain current in NMOSFET. We can observed that transconductance and DIBL characteristics are equivalent wet oxidation to nitride oxidation dielectric. (Fig. 8) shows the characteristics of charged trapping in oxide layer with various heat or dielectric condition by current stressing. Vg variation is very small when increase NO heat treatment in this figure. This is due to after hole was trapped. This is due to decreased electron-hole pair by electron injection which substitute strained Si-O combination to Si-N combination with NO heat treatment. (Fig. 9) shows the characteristics of stress induced leakage current with wet oxidation and

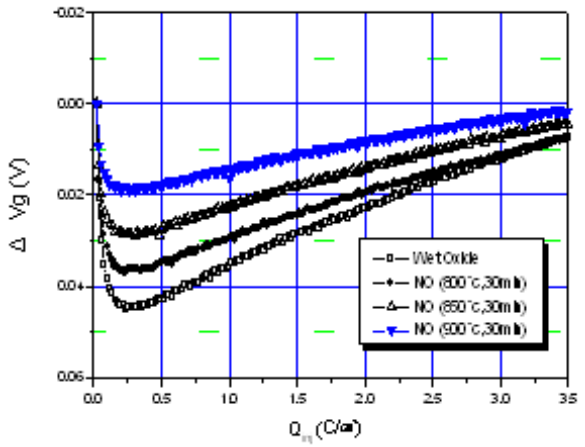


(Fig. 4) Hot carrier lifetime of standard NMOS with wet oxide. (L/T=0.1year, @Vds=2.63V)

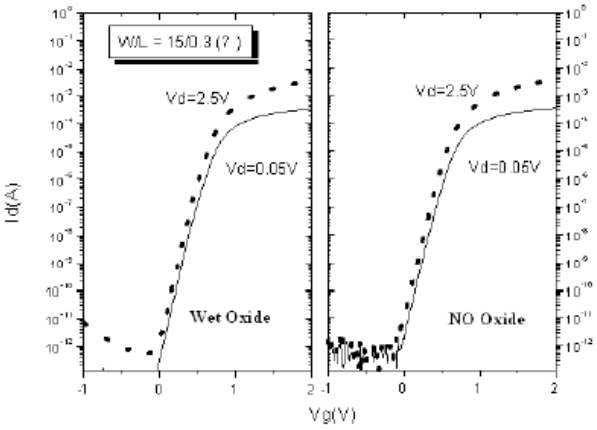


(Fig. 5) Hot carrier lifetime of standard NMOS with NO annealed oxide.(L/T=0.1year, @Vds=2.63V)

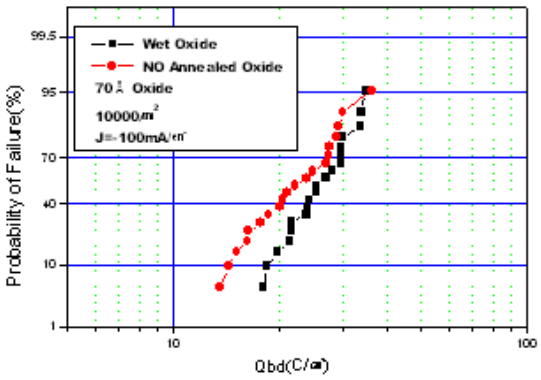
NO oxidation conditions. NO annealed leakage current lower than wet oxidation without NO annealed. This means that the degradation of hot carrier characteristics can be improved with NO annealed oxide.



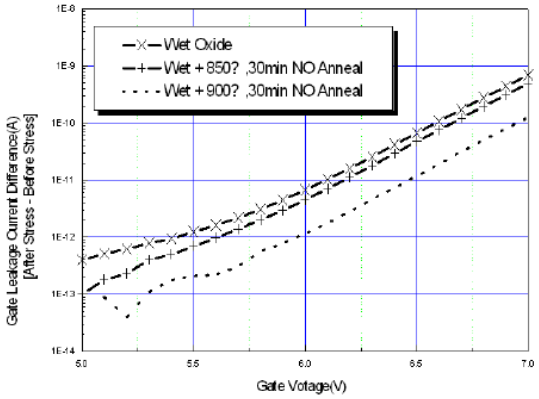
(Fig. 6) Qbd characteristics of wet oxide and NO annealed oxide.



(Fig. 7) Vg vs Id transistor charactersitics of wet oxide and NO annealed oxide.



(Fig. 8) Charge trapping phenomena with various NO heat treatments.



(Fig. 9) SILC characteristics of wet oxide and NO annealed oxide.

5. Conclusions

We fabricated and tested the 0.26㎛ NMOSFET with wet gate oxide and nitride oxide gate to compare that the characteristics of hot carrier effect, Qbd, Id_Vg characteristics, charge trapping and SILC. As a result we find that the characteristics of nitride oxide gate device better than wet gate oxide device due to nitride atoms are terminate dangling Si bonds at the Si-SiO_2 interface. This result will be helpful for long-term reliability of scaled ULSI device.

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