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Digital Control of Phase-Shifted Full-Bridge PWM Converter

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ABSTRACT

This paper presents the modeling and design of a digital controller for a phase-shifted full-bridge converter (PSFBC) in a discrete-time domain. The discretized PSFBC model is first derived and then analyzed considering the sampling effect and the system parameters. Based on this model, the digital controller is directly designed in a discrete-time domain. The simulation and experimental results are provided to show the validity of the proposed modeling and controller design.

Keywords : Zero voltage switching, Digital control, Phase shifted full-bridge PWM converter

1. Introduction

Recently, numerous soft switching techniques for switching power converters have been proposed. These techniques reduce switching losses enabling high frequency operation and consequently reducing the overall system size. Among those, the phase-shifted full-bridge converter (PSFBC) has been used as one of the most popular topologies for many applications.

Digital control offers a number of advantages over analog control. It is easier to implement the computational functions and has more flexible in designing and modifying the controller. Also, it is less sensitive to noise and environmental variations. As the price/performance ratio of digital processors continues to decrease, digital controllers are becoming a viable and competitive option. Studies on the digital control of PSFBCs were recently presented[1],[2]. However, the studies considered only the implementation of the digital controller.

This paper presents the analysis and design of a digital controller for a PSFBC in the discrete-time domain using a small signal model presented in [3],[4]. The transfer function in the discrete-time domain is first derived. Then, the effects on the sampling time and parameter variations are investigated. Based on this model, the digital controller is specifically designed in the discrete- time domain. The simulation is carried out to verify the validity of the theoretical analysis and design. The experimental verifications are performed for the prototype PSFBC with a rating 100W/100kHz. The control algorithms designed by the proposed approach are implemented on the TMS320F2812 digital signal processor (DSP). The simulated and experimental results show the validity of the proposed model and design approach.

2. Phase-shifted Full-bridge Converter

2.1 Phase-shifted full-bridge converter

Fig.1 shows the digital control system of the PSFBC, which consists of a power stage, DSP controller and signal conditioning circuit.

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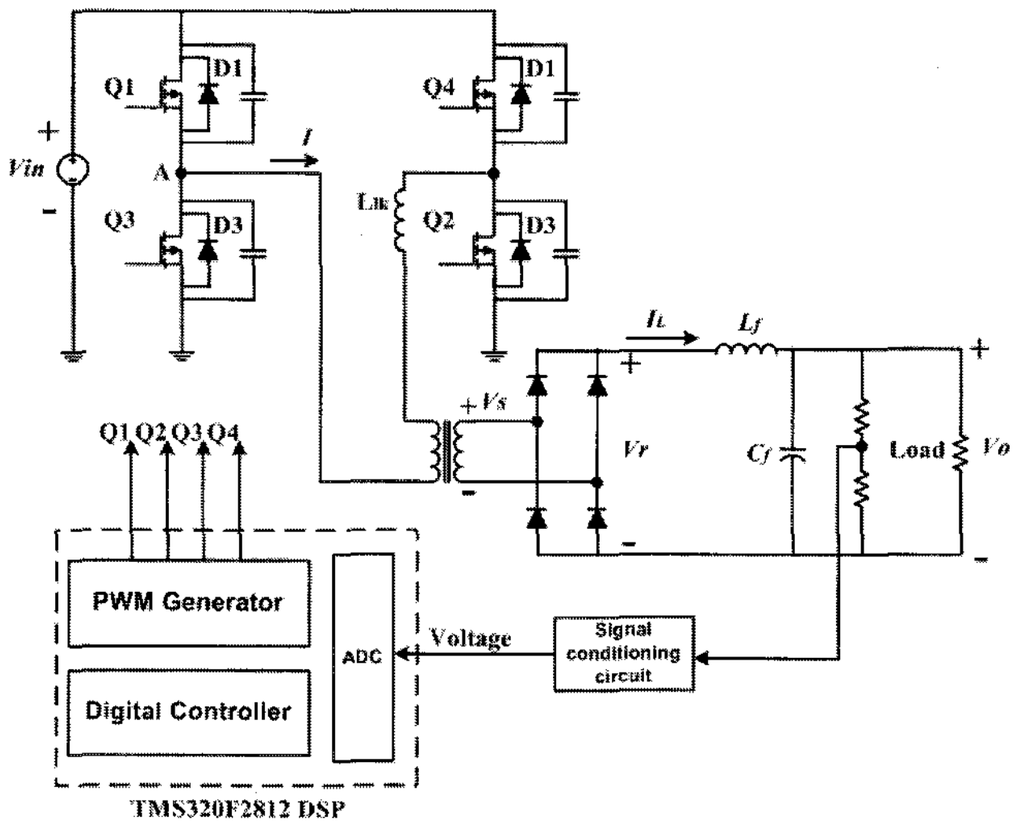

Fig. 1 Phase-shifted full-bridge PWM converter

To achieve zero voltage switching (ZVS), this converter utilizes the transformer leakage inductance L_{lk} and MOSFET's output capacitance. Also, it has a different switching pattern from that of conventional converters for ZVSs. The operation of the PSFBC is described in [3].

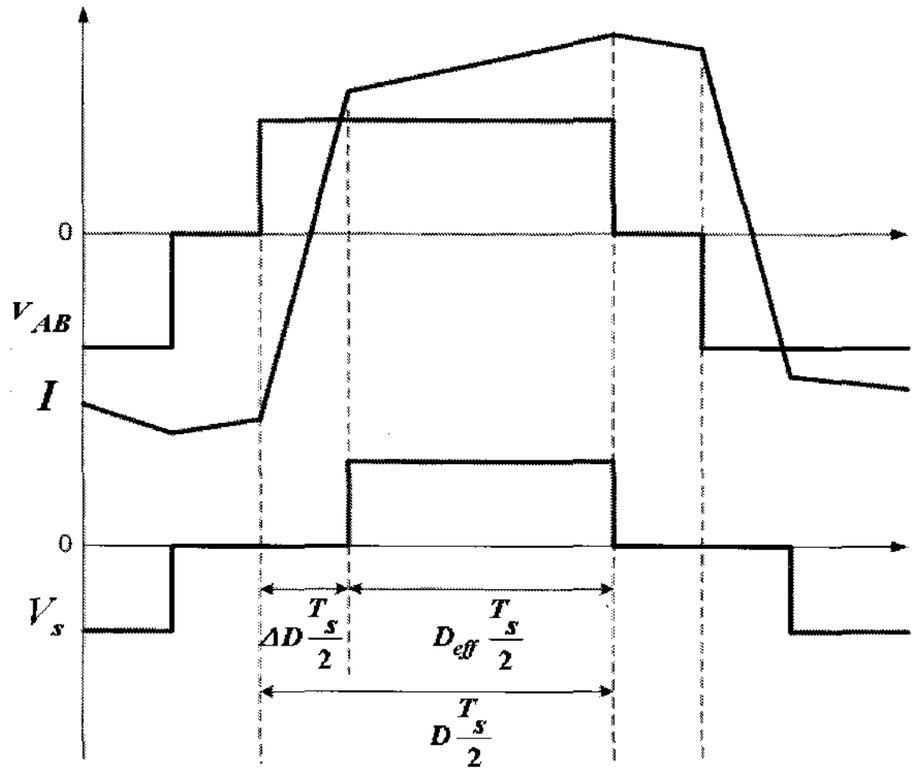

Fig. 2 Waveforms of voltage and current

Fig. 2 shows the waveforms of the current I and voltage V_{AB} in primary and the voltage across the secondary of the power transformer. The load range at which the converter operates with ZVS increases with the leakage inductance. However, the large leakage inductance reduces the effective duty cycle of the secondary voltage D_{eff}, which can be expressed as [5]

$$D_{eff} = D - \Delta D \tag{1}$$

where D and ΔD are the duty cycle of the primary voltage set by the control and loss of the duty cycle, respectively. The loss of the duty cycle is also given as

$$\Delta D = D - D_{eff} = \frac{2nL_{lk}}{V_{in}T_s}\left(2I_L - \frac{(1-D)V_oT_s}{2L_f}\right) \tag{2}$$

where n, T_s and I_L are the transformer turns ratio, the switching period and output filter inductor current, respectively.

2.2 Small-signal model

Fig. 3 shows the small-signal circuit model of PSFBC, which can be derived from the averaged small-signal model of the PWM buck converter considering the change of the duty cycle caused by the change of the filter inductor current I_L and input voltage V_{in} [5]. The effective duty cycle of the secondary voltage can be expressed as

$$d_{eff} = D_{eff} + \hat{d}_{eff} \tag{3}$$

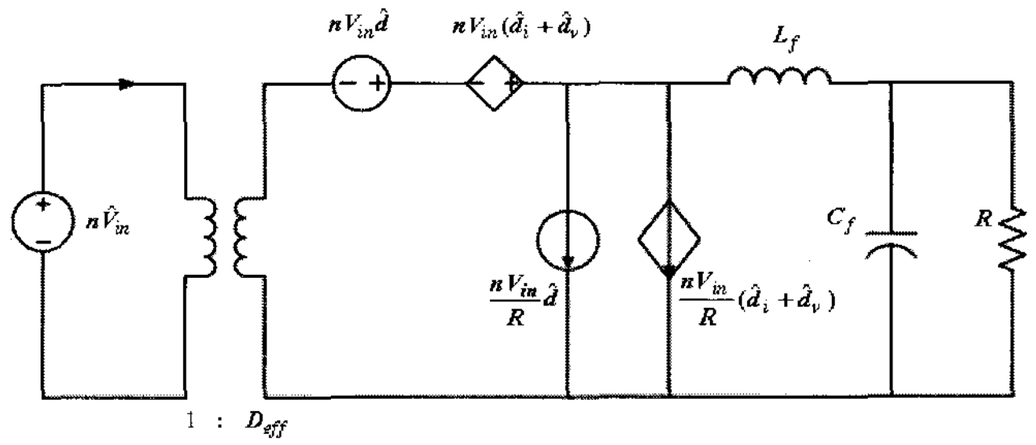

Fig. 3 Small-signal equivalent circuit

The effective duty cycle depends not only on duty cycle d of the primary voltage but also on current I_L of the output filter inductor, leakage inductance L_{lk}, input voltage V_{in}, and switching frequency f_s. Assuming that the leakage inductance and switching frequency are constant, the total change of the effective duty cycle is given as

$$\hat{d}_{eff} = \hat{d} + \hat{d}_i + \hat{d}_v \tag{4}$$

where $\hat{d}_i$ and $\hat{d}_v$ are the duty cycle variations due to the

change of the filter inductor current and input voltage, respectively. They are represented as [5],

$$\hat{d}_i = -\frac{4nL_{lk}f_s}{V_{in}}\hat{i}_L \tag{5}$$

$$\hat{d}_v = \frac{4nL_{lk}f_s}{V_{in}^2}\hat{v}_{in} \tag{6}$$

From the small-signal model of Fig. 3, the control-to-output transfer function is given as

$$G(s) = \frac{\hat{v}_O}{\hat{d}} = \frac{nV_{in}}{LC}\frac{1}{s^2 + s\left(\frac{L}{R} + R_dC\right) + \left(\frac{R_d}{RLC} + \frac{1}{LC}\right)} \tag{7}$$

where $R_d = 4n^2L_{lk}f_s$.

3. Analysis and Design of the Digital Controlled System

There are, in general, two approaches in designing a digital controller: the digital redesign and direct-digital approach [6]. In this paper, the controller is designed using the direct-digital approach and then it is compared using the digital redesign approach. The parameters used in the controller design are summarized in Table 1.

Table 1 System parameter

Parameter	Symbol	Value	Unit
Input voltage	V_{in}	48	V
Output voltage	V_{out}	12	V
Power	-	100	W
Turn ratio (Ns/Np)	n	0.5	-
Switching frequency	f_s	100	kHz
Output filter inductance	L_f	30	uH
Output filter capacitance	C_f	150	uF
Transformer leakage inductance	L_{lk}	5	uH

3.1 PSFBC model in discrete-time domain

The PSFBC model in the continuous-time domain is first transformed into the discrete-time domain. Then, the controller is directly designed using the discrete-time domain model. Fig. 4 shows a block diagram of the digital control loop, where $G_c(z)$ is the transfer function of the digital controller, ZOH denotes the zero order holder, $G(s)$ is the transfer function of the PSFBC and K_d and T_s denote the voltage sensing gain and sampling period. $H(z)$ is the discrete-time transfer function of the computation delay.

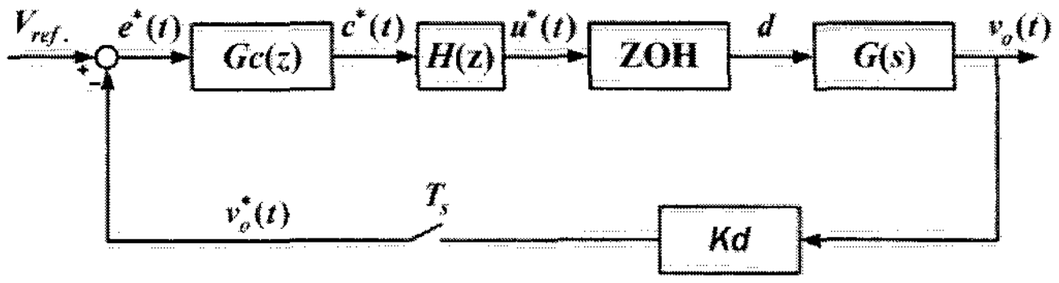

Fig. 4 Block diagram of digital control loop

The discrete-time transfer function $G(z)$ of the PSFBC considering the ZOH and K_d is derived as

$$G(z) = Z\left[\frac{1-e^{-sT_s}}{s}\cdot G(s)\cdot K_d\right] = \frac{\gamma}{\beta}\cdot\frac{b_1z + b_0}{z^2 + a_1z^1 + a_0} \tag{8}$$

where $Z[\bullet]$ denotes the z-transform of $[\bullet]$, and

$$a_1 = -2e^{-\frac{\alpha}{2}T_s}\cos\sqrt{\beta-(\alpha/2)^2}\,T_s, \quad a_0 = e^{-\alpha T_s},$$

$$b_1 = 1 - e^{-\frac{\alpha}{2}T_s}\cos\sqrt{\beta-(\alpha/2)^2}\,T_s - \frac{\alpha/2}{\sqrt{\beta-(\alpha/2)^2}}e^{-\frac{\alpha}{2}T_s}\sin\sqrt{\beta-(\alpha/2)^2}\,T_s,$$

$$b_0 = e^{-\alpha T_s} - e^{-\frac{\alpha}{2}T_s}\cos\sqrt{\beta-(\alpha/2)^2}\,T_s + \frac{\alpha/2}{\sqrt{\beta-(\alpha/2)^2}}e^{-\frac{\alpha}{2}T_s}\sin\sqrt{\beta-(\alpha/2)^2}\,T_s,$$

$$\alpha = \frac{1}{RC} + \frac{R_d}{L}, \quad \beta = \frac{R_d}{RLC} + \frac{1}{LC}, \quad \gamma = \frac{nV_{in}}{LC}.$$

$H(z)$ is not included in (8) and it will be considered in Section 3.3.

3.2 Effects of leakage inductance

Fig. 5 shows the root loci of the closed-loop system using (8) for various L_{lk} to examine the effect of leakage inductance L_{lk}. Only loop gain K is considered in the feedback loop for this analysis. It can be shown in Fig. 5 that the critical value of loop gain K also increases as leakage inductance L_{lk} increases. The large leakage inductance may improve the relative stability.

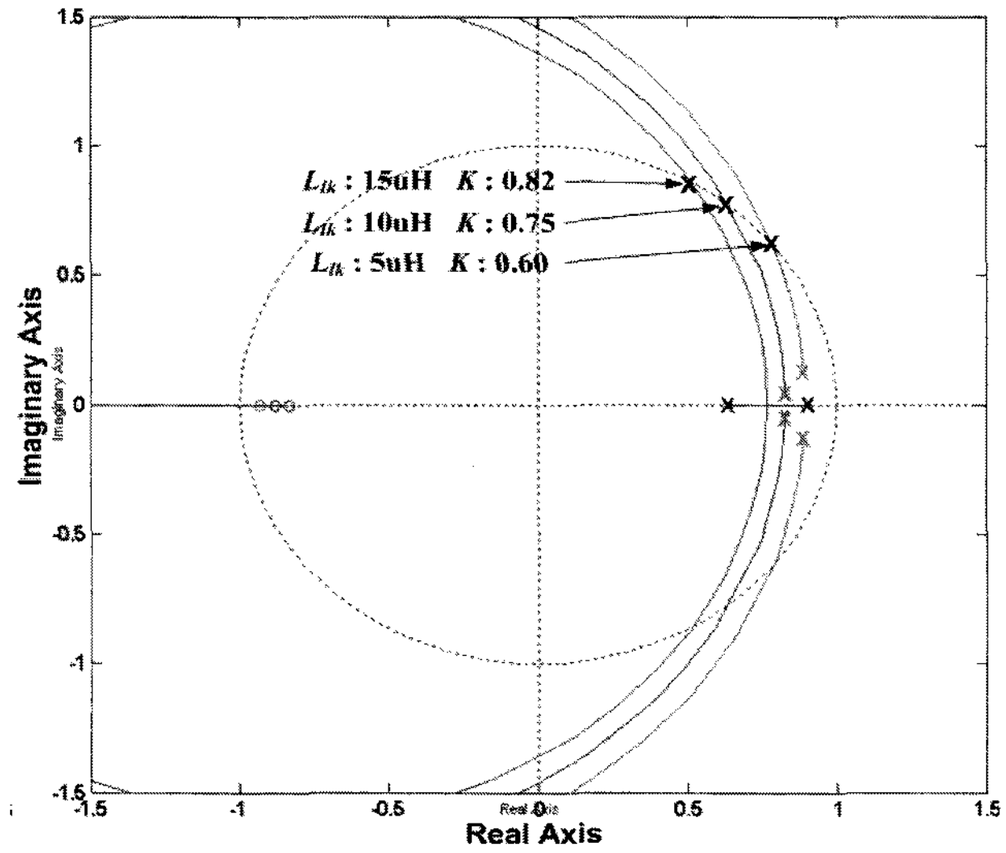

Fig. 5 Root loci of the closed-loop system (Characteristic equation :1+K•$G(z)$=0)

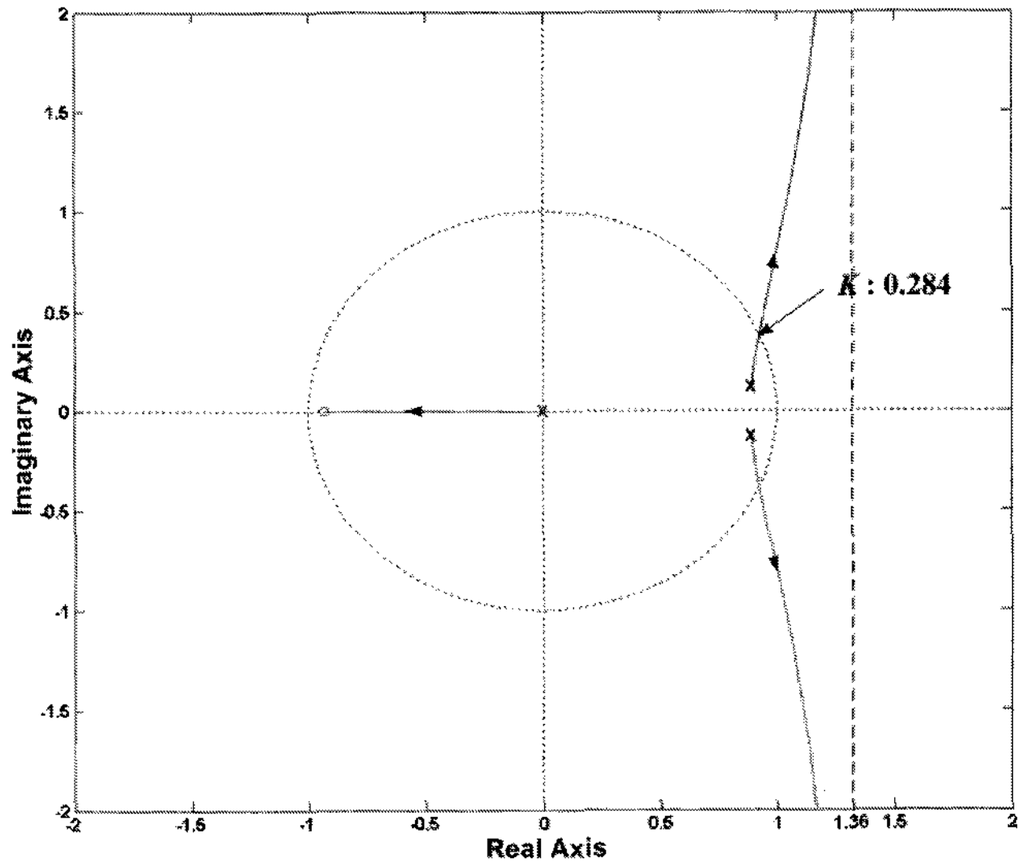

Fig. 6 Root loci of the closed-loop system considering computation delay(Characteristic equation : 1+ K•$G'(z)$=0)

On the other hand, the leakage inductance also causes duty loss. As shown in Fig. 2, the finite slope in the rising and falling edges of the primary current reduces the duty available cycle in the secondary. The large leakage inductance shows the negative effect of increasing the duty loss because it causes longer rising and falling edges.

3.3 Effects of time delay

The computation delay, T_d is the time delay between the sampling instant of the A/D converter and the updated instant of the subsequent PWM duty ratio [7]. This must be considered for the design of the controller. Transfer function $H(z)$ of the computation delay can be included into discrete-time transfer function $G(z)$ in (8). If T_d is an integral multiple of the sampling period T_s, the transfer function of the computation delay in the discrete-time domain can be simply expressed as

$$H(z) = z^{-k} \tag{9}$$

where k = 1, 2, 3, …. Thus, discrete-time transfer function $G'(z)$ with the delay of one sampling period is given as

$$G'(z) = \frac{\gamma}{\beta} \cdot \frac{b_1 z + b_0}{z(z^2 + a_1 z^1 + a_0)} \tag{10}$$

The root loci of the closed-loop system with the computation delay of one sampling period are shown in Fig. 6.

Like Section 3.2, loop gain K is only considered. The root loci are affected by the addition of the open loop pole at z=0. The complex conjugate poles of the closed loop system asymptotically approaches 90° and 270° asymptotes which intersect at z=1.36 and the critical value of loop gain K is 0.284. Thus, the computation delay decreases the stability margin of the system.

3.4 Effects of sampling time

The effects of sampling time are investigated in this section. The digital PI controller is used to regulate the output voltage and can be expressed as

$$G_c(z) = \frac{K_P z - (K_P - K_I T_s)}{z - 1} \tag{11}$$

The characteristic equation of the closed-loop system including controller is given as

$$d_3 z^3 + d_2 z^2 + d_1 z + d_0 = 0 \tag{12}$$

where

d_3=1 ,

$$d_2 = \frac{\gamma}{\beta} K_P \left(1 - e^{-\frac{\alpha}{2}T_s} \cos\sqrt{\beta - (\alpha/2)^2}\, T_s - \frac{\alpha/2}{\sqrt{\beta - (\alpha/2)^2}} e^{-\frac{\alpha}{2}T_s} \sin\sqrt{\beta - (\alpha/2)^2}\, T_s \right)$$

$$-2e^{-\frac{\alpha}{2}T_s} \cos\sqrt{\beta - (\alpha/2)^2}\, T_s - 1,$$

$$d_1=\frac{\gamma}{\beta}K_P\left(e^{-\alpha T_S}+\frac{\alpha}{\sqrt{\beta-(\alpha/2)^2}}e^{-\frac{\alpha}{2}T_S}\sin\sqrt{\beta-(\alpha/2)^2}\,T_s-1\right)$$
$$+K_IT\left(1-e^{-\frac{\alpha}{2}T_S}\cos\sqrt{\beta-(\alpha/2)^2}T_s-\frac{\alpha/2}{\sqrt{\beta-(\alpha/2)^2}}e^{-\frac{\alpha}{2}T_S}\sin\sqrt{\beta-(\alpha/2)^2}T_s\right)$$
$$+e^{-\alpha T_S}+2e^{-\frac{\alpha}{2}T_S}\cos\sqrt{\beta-(\alpha/2)^2}\,T_s,$$

$$d_0=-e^{-\alpha T}-\frac{\gamma}{\beta}(K_P-K_IT)\left(e^{-\alpha T}-e^{-\frac{\alpha}{2}T_S}\cos\sqrt{\beta-(\alpha/2)^2}\,T_s\right.$$
$$\left.+\frac{\alpha/2}{\sqrt{\beta-(\alpha/2)^2}}e^{-\frac{\alpha}{2}T_S}\sin\sqrt{\beta-(\alpha/2)^2}T_s\right).$$

Fig. 7 shows the stable region of the closed loop system for various proportional gain K_P and sampling times T_s. This figure can be obtained using (10), where K_I is set to zero. When the sampling time is 0.01ms, the boundary value for K_P guarantees the stable operation of the system is 0.6.

Fig. 8 presents the stable region of the closed loop system for various controller gains K_P, K_I and sampling times T_s. It is noted in this figure that a sufficiently fast sampling time below 0.01ms is required to guarantee the stability in a wide range of K_P, and K_I.

3.5 Design of digital controller

Since the control algorithms implemented in the experimental system have the computation delay of one sampling period, the controller should be designed using (10). The PI controller given in (11) is used to improve the steady-state performance with relative stability. The digital controller can be designed by the frequency response method in the w-plane.

$$z=\frac{2+wT}{2-wT} \tag{13}$$

Applying the w-transformation of (13) the plant $G'(z)$ is transformed into

$$G'(w)=\frac{0.017w^3+8.904\times10^4\,w^2-3.769\times10^{10}\,w+3.833\times10^{14}}{0.027\,w^3+7.945\times10^5\,w^2+1.643\times10^{10}\,w+2.176\times10^{14}} \tag{14}$$

Fig. 9 shows the bode plots for the uncompensated and compensated systems, where the closed loop bandwidth is set as 2.16 kHz with a phase margin of 54°.

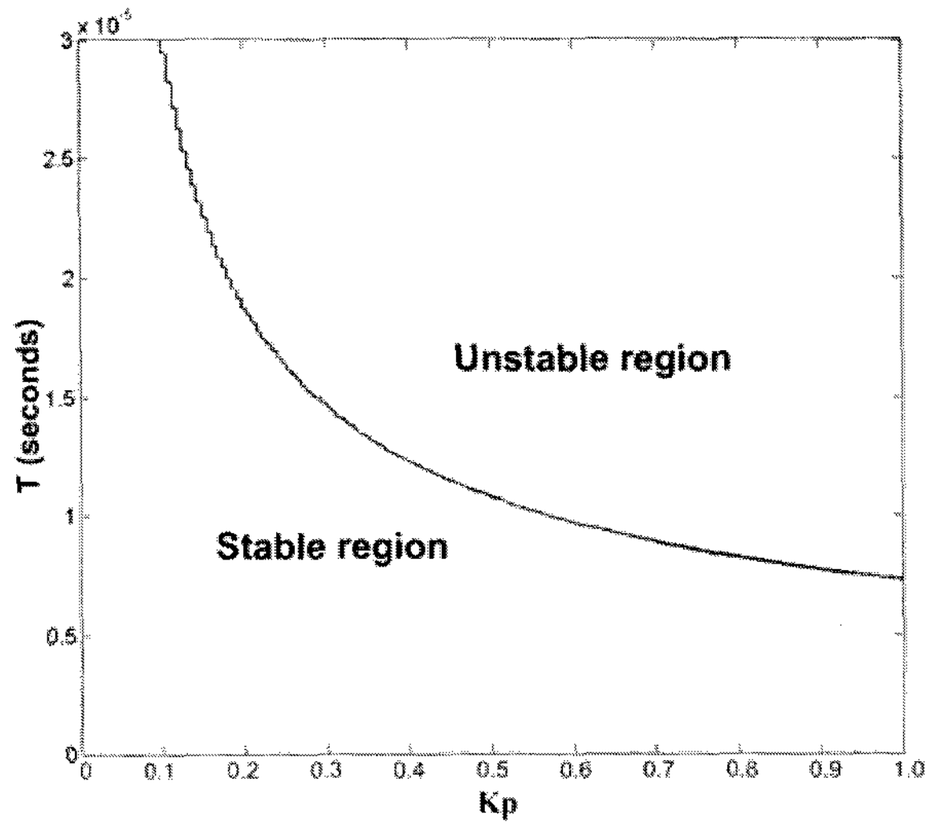

Fig. 7 Stable region for various K_p and T_s values

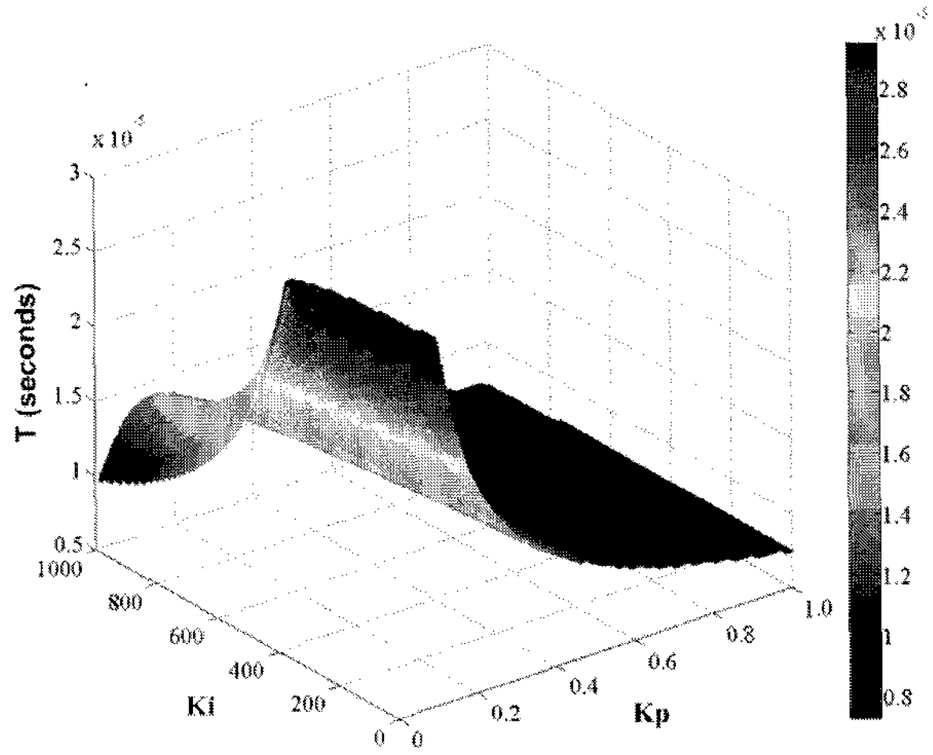

Fig. 8 Stable region for various K_I, K_P and T_s values

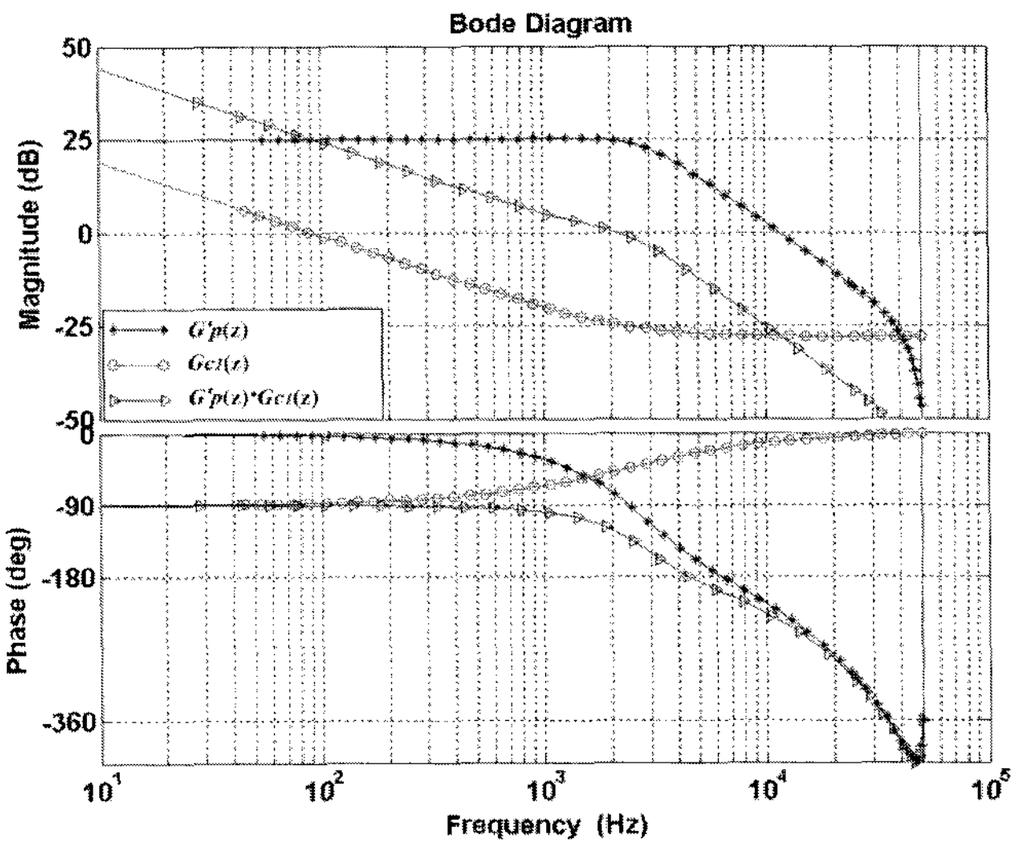

Fig. 9 Bode plots of direct digital designed system

The gain margin is 10.1dB at 4.45 kHz. The transfer function of the PI controller satisfying these design specifications can be obtained directly in the discrete-time domain and is given as

$$G_{c1}(z) = 0.0432\frac{z-0.859}{z-1} \tag{15}$$

where K_P and K_I are 0.0432 and 574, respectively. In this design, the sampling time and maximum overshoot of the control system can be predicted as 0.6ms and 10.9%, respectively.

For performance comparison, a PI controller with similar specifications was designed using the digital redesign approach. The frequency response of the control system in the continuous-time domain is shown in Fig. 10 (plot 1), where the system bandwidth is set as 2.79 kHz with a phase margin as 52°. The gain margin is 7.9dB at 4.47 kHz. The controller providing these closed loop characteristics can be given as

$$G_{c2}(s) = \frac{K_P(s-K_I/K_P)}{s} = 0.056\frac{s-13210}{s} \tag{16}$$

where K_P and K_I are 0.056 and 739, respectively. The settling time and maximum overshoot for this design can be predicted as 0.39ms and 10.4%, respectively. For the implementation of the digital control system, the analog controller is transformed into a digital form. There are several discretization methods [6]. The controller of (16) is discretized using the step invariant method and the result is given as

$$G_{c2}(z) = 0.056\frac{z-0.867}{z-1} \tag{17}$$

Plot 2 of Fig. 10 is the frequency response for $G'(z)$ with the redesigned controller $G_{c2}(z)$. The system bandwidth and the phase margin are 2.71[kHz] and 37.3°, respectively. It is known in this figure that the difference of the phase margin between the plot 1and 2 is 15.9°. The reason for this is that the sample and hold and computation delay were not considered in the redesigned system.

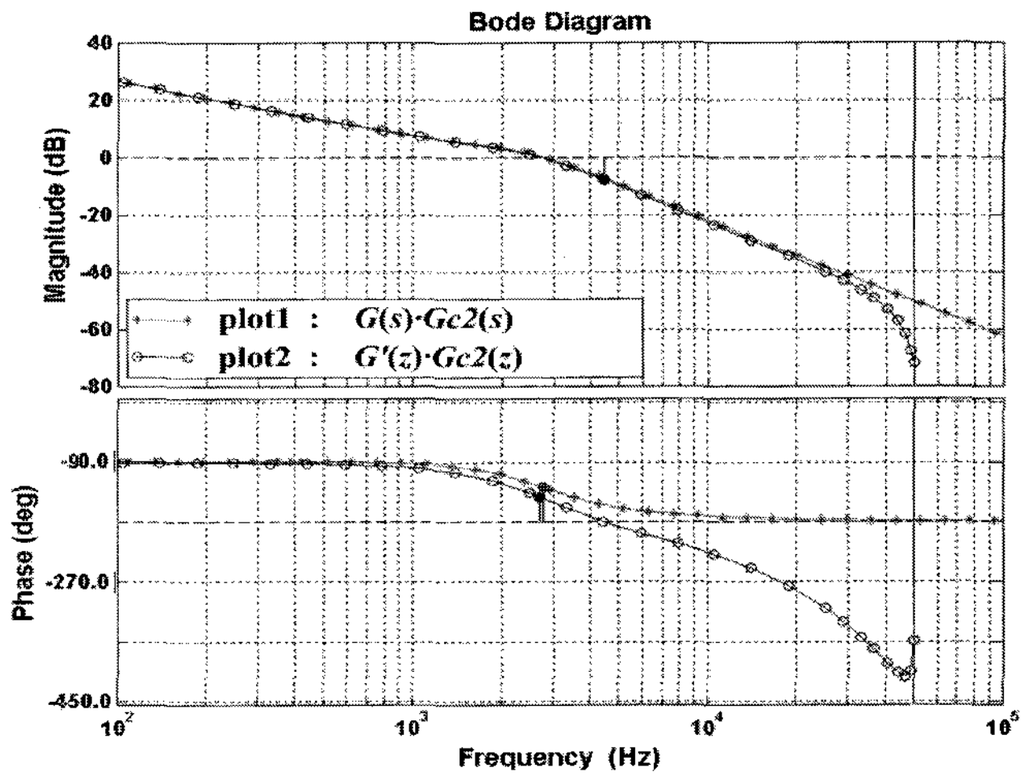

Fig. 10 Bode plots of the digital redesigned system

4. Simulations and Experiments

4.1 Simulated results

The simulation studies were performed using a PSIM7 simulator. Fig. 11 shows the output voltage waveforms of the control system using the digital redesigned(V_{O1}) and direct digital designed(V_{O2}) controllers under the step load changes.

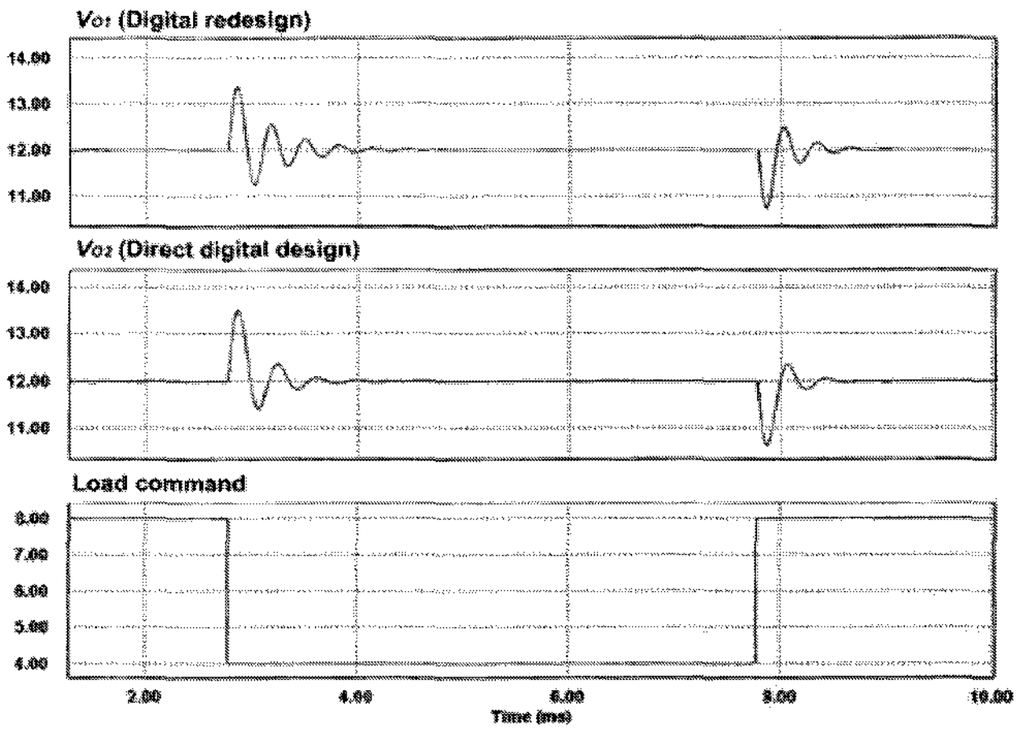

Fig. 11 Simulated step-load responses

The parameters of the controllers are shown in (15) and (17), respectively. The load current was abruptly changed from 4[A] to 8[A]. As shown in Fig. 11, the settling time (2% of steady-state voltage) and the maximum overshoot of the output voltage V_{O1} is 10ms and 11%. The settling time and the maximum overshoot of the digital redesigned

system using the controller given in (15) were predicted as 0.3ms and 10.4%. These differences in the designed and actual control performances are caused by ignoring the effect of the sample and hold, and the computation delay. The settling time (2% of steady-state voltage) of the output voltage V_{O2} is 0.7ms and the maximum overshoot was 12% of the output voltage. It is noted that the closed loop control system shows a satisfactory time domain response.

4.2 Experimental results

Fig. 12 shows a photograph of the experimental PSFBC with a rating of 100W/100kHz, where the design parameters are given in Table. 1. The digital controller is implemented on a DSP TMS320F2812.

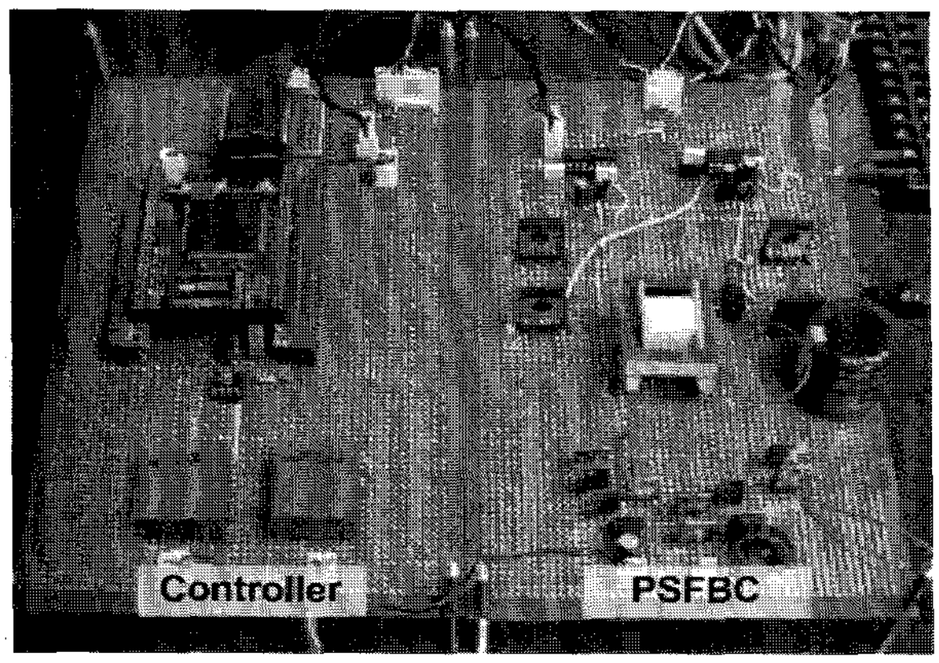

Fig. 12 Photograph of the PSFBC system

Fig. 13 shows the measured experimental results, where the trace on Ch2 is the voltage V_r across the secondary rectifier, and the traces on Ch3 and Ch4 are the primary voltage and current of the transformer, respectively.

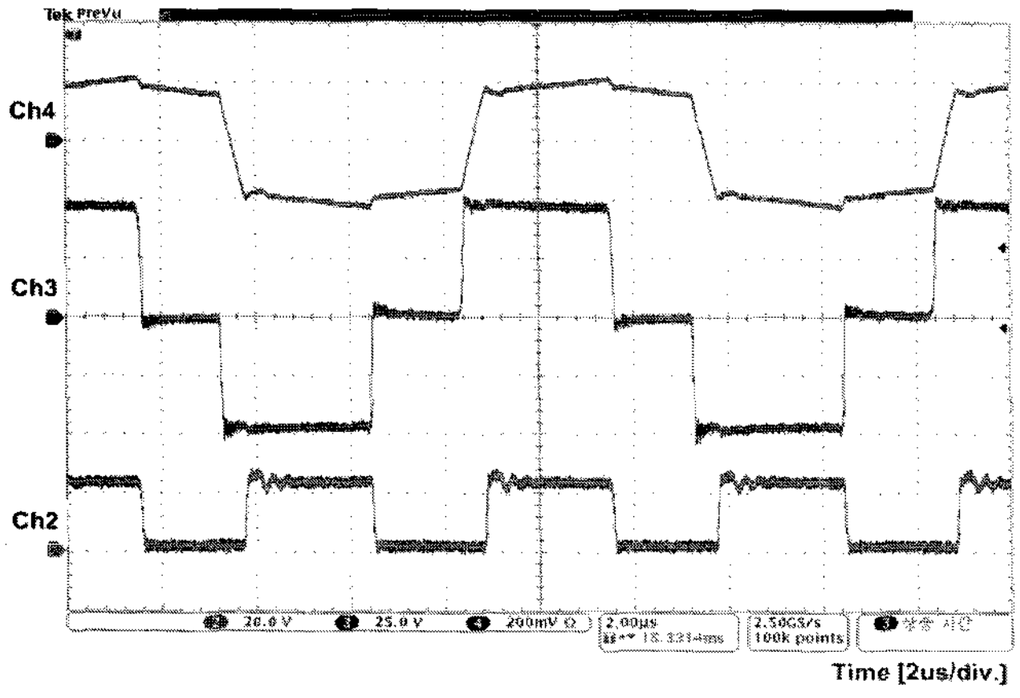

Fig. 13 Key waveforms for the experimental system
(Ch4 : primary current [2A/div.], Ch3 : primary voltage [25V/div.] Ch2 : voltage V_r of the rectifier [20V/div.])

Fig. 14 shows the drain and gate voltages of switch Q2, respectively. The ZVS for switches Q1 and Q3 of the leading leg in the PSFBC is easily achieved using the energy of large filter inductor L_{lf}. But, the switches Q4 and Q2 of the lagging leg use only the energy restored in the leakage inductance for operating the ZVS [3].

Therefore, the ZVS in the lagging leg is lost in a low load current. In Fig. 14, the traces on Ch1 and Ch2 are the drain and gate voltages of switch Q2, respectively. The mini- mum range of the ZVS in this PSFBC system is calculated at 3.5 [A] [3]. As shown in Fig. 14, after the drain voltage of Q2 becomes low, the gate voltage becomes high. It is noted that the ZVS is achieved for lagging switch Q2.

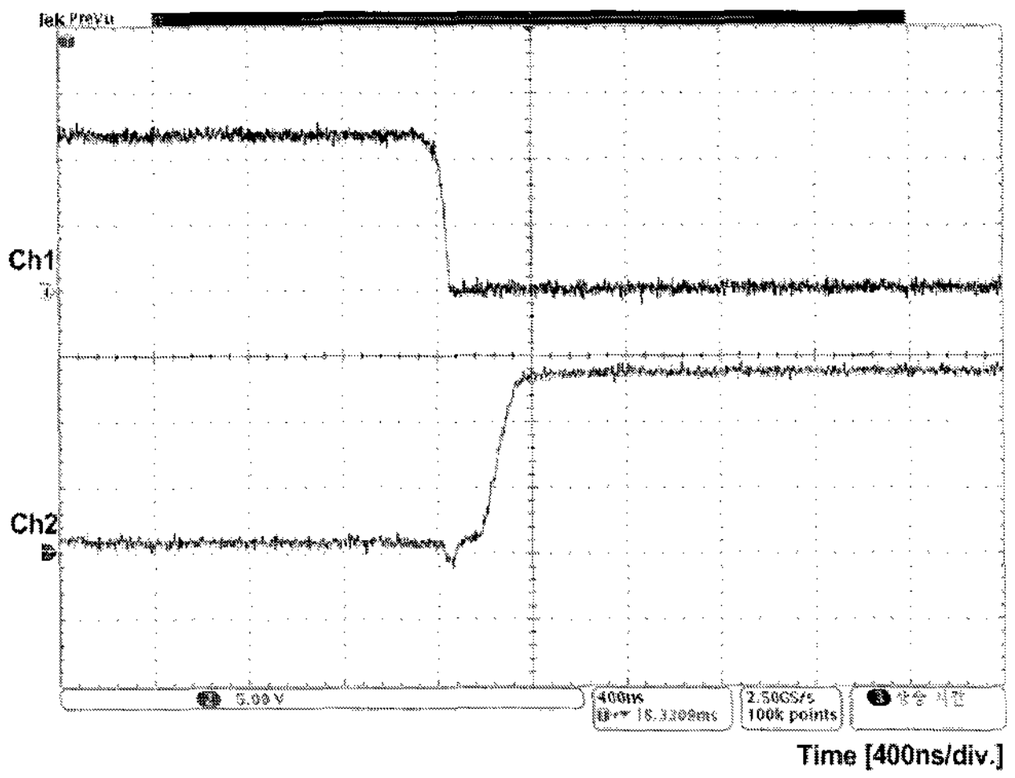

Fig. 14 Measured drain and gate voltage of switch Q2
(Ch1 : drain voltage [20V/div.], Ch2 : gate voltage [5V/div.])

Fig. 15 and 16 show the output voltage responses for the step load change in the both digital redesign and the proposed approaches, respectively, where the trace on Ch2 is the output voltage and Ch4 is the output current.

In Fig. 15, after the load current is changed from 8[A] to 4[A], the settling time (2% of steady-state voltage) of the output voltage is measured as 1.6ms and the maximum overshoot is 16%.

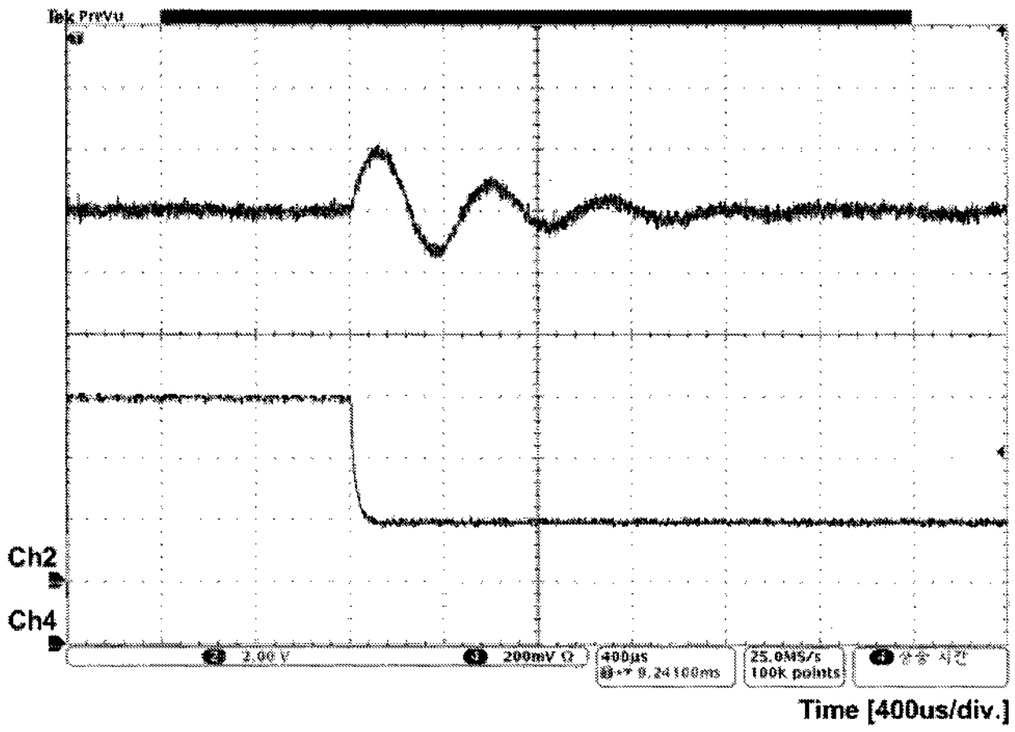

Fig. 15 Measured step-load response of the digital redesigned system(Ch2 : output voltage[2V/div.], Ch4 : output current[2A/div.])

In Fig. 16, the settling time (2% of steady-state voltage) of the output voltage is 1ms and the overshoot is 18%. The settling time presents about 60% of that using the digital redesign approach. The difference of the maximum over-shoot can be ignored.

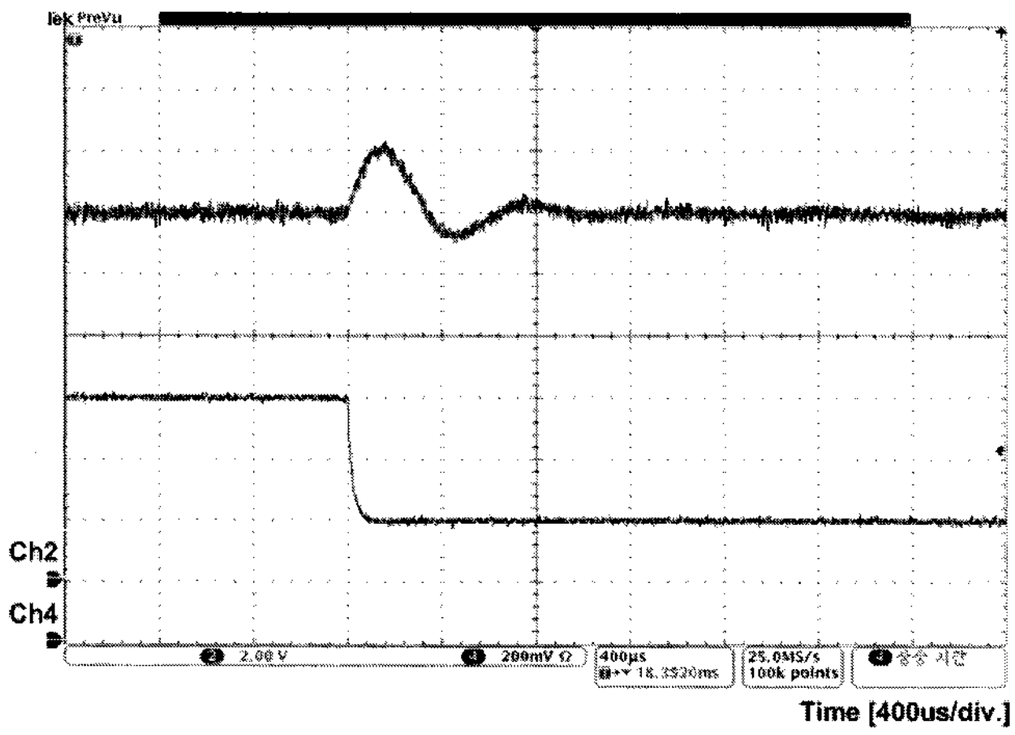

Fig. 16 Measured step-load response of the direct designed system(Ch2 : output voltage[2V/div.], Ch4 : output current[2A/div.])

5. Conclusions

In this paper, the digital control of a PSFBC was presented. The transfer function in the discrete-time domain is first derived using a small-signal model, and the effects on the sampling time and converter parameter were then analyzed. It is noted from this analysis that the relative stability was improved as the leakage inductance increased. However, since the large leakage inductance may cause duty loss and narrow ZVS range, it should be carefully selected. The proposed controller was specifically designed in the discrete-time domain using the discretized PSFBC model and implemented using the DSP-based digital controller. The performance of the proposed controller is compared with the conventional controller using the digital redesign approach. It was shown from the simulation and experimental results that the proposed controller provides better performance than the conventional controller using the digital redesign approach, because the time delay and sampling effects were considered in the controller design.

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