Power-Gating Structure with Virtual Power-Rail Monitoring Mechanism

Hyoung-Wook Lee, Hyunjoong Lee, Jong-Kwan Woo, Woo-Yeol Shin, and Suhwan Kim

Abstract—**We present a power gating turn-on mechanism that digitally suppresses ground-bounce noise in ultra-deep submicron technology. Initially, a portion of the sleep transistors are switched on in a pseudo-random manner and then they are all turned on fully when VVDD is above a certain reference voltage. Experimental results from a realistic test circuit designed in 65nm bulk CMOS technology show the potential of our approach.**

Index Terms—**Leakage, sub-threshold, power-gating, ground-bounce noise, deep sub-micron**

I. INTRODUCTION

As the gate length of a transistor gets shorter, its power consumption, due to the increased leakage current between the transistor's source and drain when no signal voltage is applied at the gate gets, larger. This can occur, for example, when a mobile phone is on standby awaiting calls and processing no data. A tremendous increase in transistor leakage current is the primary disadvantage of technology scaling. Leakage affects not only the standby and active power consumption of a CMOS system, but also circuit reliability, since leakage is strongly correlated to process variations. The influence of leakage current on circuit performance depends on: the operating conditions (e.g., standby or active), the circuit style (e.g., logic or memory), and the environmental conditions (e.g., the supply voltage) [1-2].

There are several different approaches to tackling leakage. Power gating is one well-known way of reducing leakage and it continues to be applied to very-deep submicron CMOS technologies. There has been a lot of work on the multi-threshold voltage CMOS (MTCMOS) technique, which uses a MOSFET switch to gate, or cut off, a circuit from its power rail(s) during standby mode [3-6].

Without a clear understanding of the technique, however, the negative effects of power gating, such as, inductive noise and the range of device options, make it difficult to realize the potential benefits. Ground bounce is induced by an instantaneous power mode transition of a sleep transistor in a power gating structure [7-8].

We present a power gating structure that digitally suppresses ground-bounce noise in ultra-deep submicron technology. We evaluate this approach with a test structure in 65nm CMOS bulk technology, using single-threshold devices for both logic and sleep transistors. We also present simulation results from this structure that show the potential benefits of our approach.

II. POWER GATING STRUCTURE

Leakage is power consumed by the circuit when it is

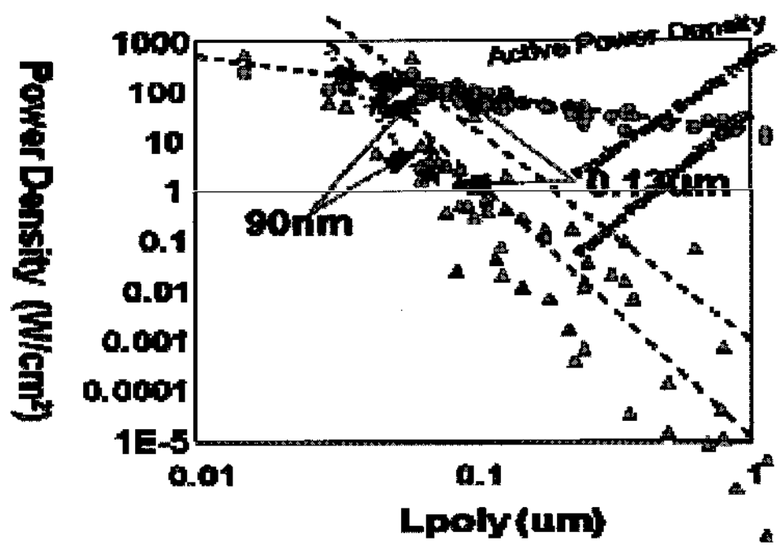

Fig. 1. Leakage power (sub-threshold and gate) is increasing at an exponential rate and is growing much faster than dynamic (or switching) power.

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off, and this problem has emerged as the most critical design challenge for current and future integrated circuits, because it limits the frequency, yield and power of most of the IC industry's leading designs. In early complementary metal-oxide semiconductor (CMOS) circuits, leakage was negligible. However, leakage power increases exponentially, as device dimensions are scaled down and leakage is expected to determinate the power requirement of 65nm process devices.

Leakage has several different components, but, the largest are related to sub-threshold operation as shown in Fig. 1. The equation for sub-threshold leakage current is

$$I_{leakage} = I_{s0} e^{(V_{gs}-V_{th})/nV_T}(1-e^{-V_{ds}/V_T}) \quad (1)$$

Where

$$I_{s0} = K(W_{eff}/L_{eff})V_T^2 \quad (2)$$

$$V_{th} = V_{th0} - \gamma V_{bs} - \eta V_{ds} \quad (3)$$

and V_{gs} is the transistor-gate to source voltage; V_{ds} is the drain to source voltage; V_{th0} is the zero bias threshold voltage; γ is the linearized body-effect coefficient; V_{bs} is the source to body voltage; η is the DIBL (drain induced barrier lowering) coefficient; n is the sub-threshold swing coefficient; V_T is the thermal voltage; K is a process constant; W_{eff} is the effective transistor width; and L_{eff} is the effective transistor channel length.

Leakage control techniques focus on controlling one or more terms in these equations. The most prevalent techniques can be categorized as reducing V_{gs}, increasing V_{th0}, lowering V_{bs}, and reducing V_{ds}. Several different methods for controlling these terms are described below, and we describe how they relate to equation (1) to (3).

The use of MTCMOS power gating is a well-known technique for reducing sub-threshold leakage power in standby mode, while still permitting high-speed operation in active mode. Power gating is a design technique in which a power-gating transistor is inserted in the stack between the logic transistors and either power or ground, as shown in Fig. 2, thus creating a virtual supply rail (VVDD).

All the logic transistors contain all low-V_{th} transistors to achieve the fastest switching speeds, while the sleep

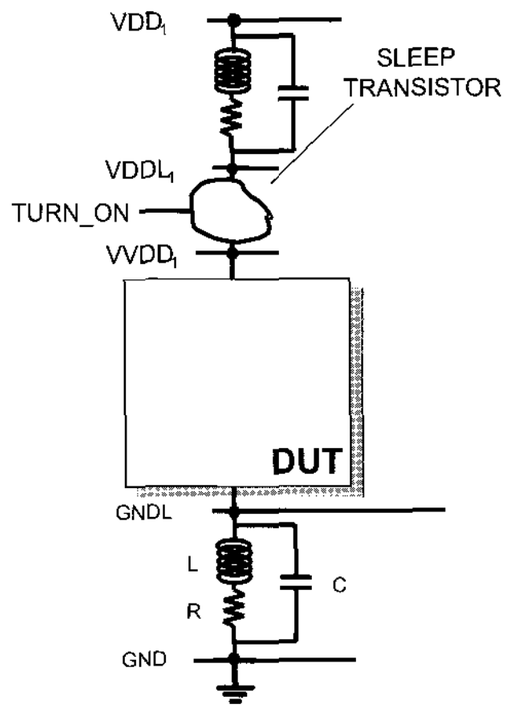

Fig. 2. MTCMOS power-gating circuit topology.

transistors are built using high-V_{th} transistors to minimize the leakage. Power-gating, which can be implemented without using multiple thresholds, reduces leakage lowering the gate-to-source voltage, which in turn drives the logic transistors deeper into their cutoff region. This occurs because of the stack effect. The source terminal of the top-most transistor in the logic stack is no longer at supply, but rather at a voltage somewhat below supply due to the presence of the power gating transistor.

III. Ground Bounce Noise Reduction

Many vendors of low-power embedded products containing multiple processors now include a power-gating capability in the form of 'sleep' modes, which typically operate under software control. When the operating system detects a long idle loop, one of the several processor cores continues to run at its maximum operating frequency, while the other cores are power-gated off.

By turning off the sleep transistor during the sleep period, however, all the internal capacitive nodes of the logic transistors and VVDD nodes are discharged to a steady-state value near ground (GND). During a power-mode transition, an instantaneous charge current passes through the sleep transistor, which is operating in its saturation region, and creates current surges elsewhere. Because of the self-inductance of the off-chip bonding wires and the parasitic inductance inherent to the on-chip power rails, these surges result in voltage fluctuations in the power rails. If the magnitude of the voltage surge or droop is greater than the noise margin of a circuit, that circuit may erroneously latch to the wrong value or switch at the wrong time [7-8,10].

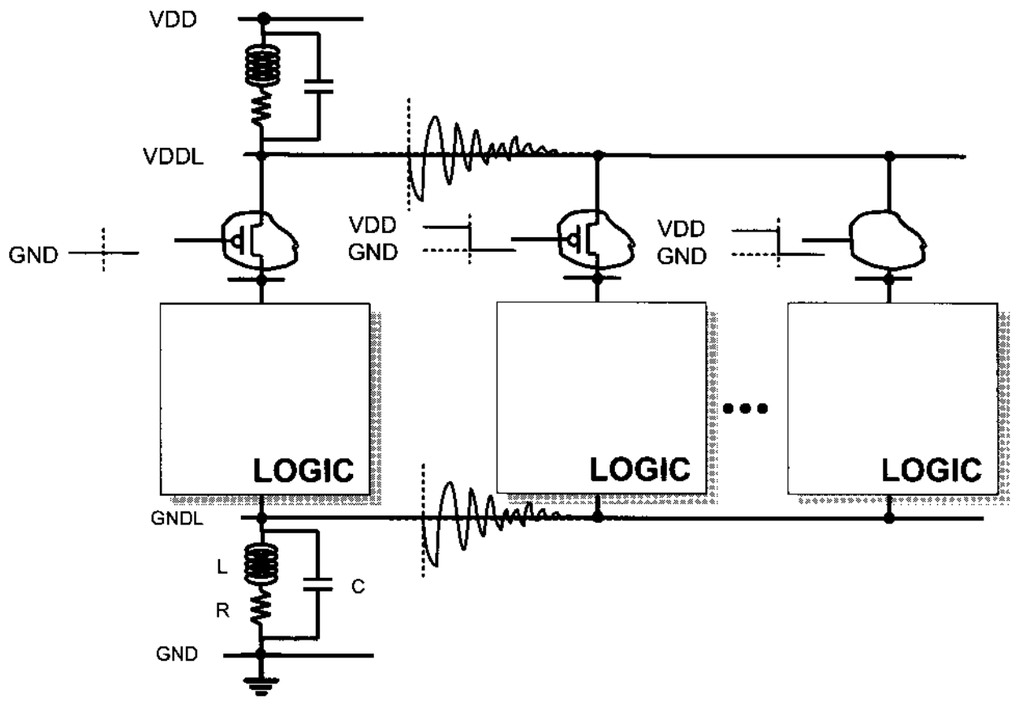

Fig. 3. A system-on-a-chip (SoC) employing multiple power-gating structures to control sub-threshold leakage power.

Inductive noise, also known as simultaneous switching noise, is a phenomenon that has been traditionally associated with input/output buffers and internal circuitry. In the past, inductive noise originating from power-mode transitions between the active and standby modes of a power gating structure was not considered serious; but it is likely to become an important issue in the design of a system-on-a-chip (SOC) that employs multiple power gating domains to control leakage power. As shown in Fig. 3, inductive noise can induce ground bounce in nearby circuits which should still be operating normally. The noise immunity of a circuit decreases as its supply voltage is reduced. It is therefore essential to consider using a technique such as power gating to address the problem of ground bounce in low-voltage CMOS circuits.

The 'wakeup latency' of an arithmetic unit is the time required to bring a circuit out of sleep mode, until it is operating at 95% of its maximum operating frequency for a given supply voltage. In measuring this latency [9], the inductive noise due to clock gating is effectively excluded, since the performance degradation due to the clock gating itself is around 5%. Initially, we turned off the sleep transistor by setting $|V_{gs}| = 0$ and waiting until all internal nodes and the VVDD node were completely discharged. Then, we turned on the sleep transistor by setting $|V_{gs}|$ = VDD and measured the shortest wake-up latency that did not lead to failure. This test was repeated for a range of supply voltages. The resulting wake-up times, ranging from 498 ns to 807 ns, as shown in Fig. 4, demonstrate the serious effect on performance of the inductive noise due to the power-gating structure. To make matters worse, the other circuits sharing the same power rails are similarly disturbed.

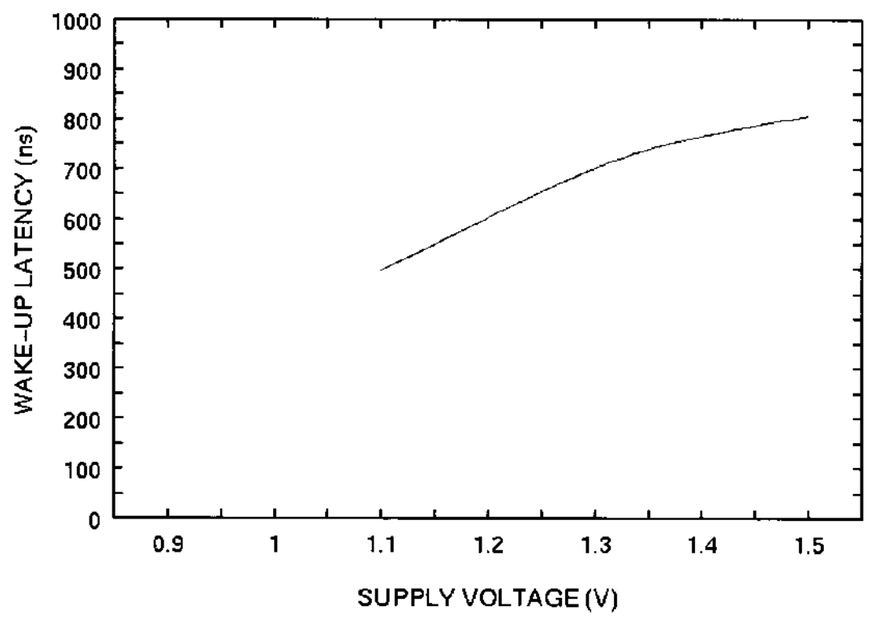

Fig. 4. Wake-up latency (without failure) [9].

The sleep transistor in a power-gating structure can be implemented as a single transistor or a set of transistors. As shown in Fig. 5, a sleep transistor implemented as a set of individual transistors wired in parallel is effectively a single transistor because all the transistors share both a VVDD node and a VDDL rail, and are turned on simultaneously. During a mode transition, the large instantaneous current flowing through the sleep transistor of a conventional power-gating structure causes large voltage fluctuations

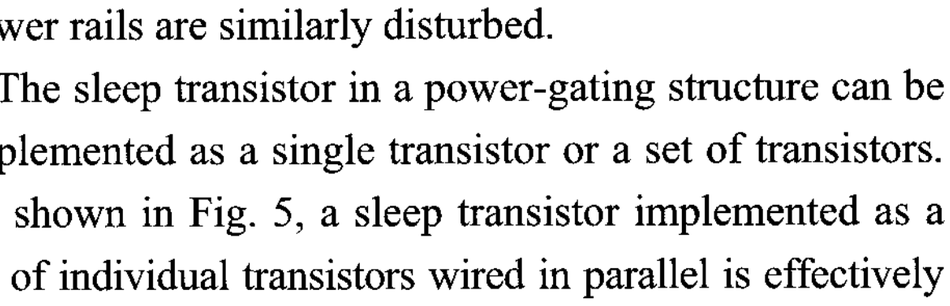

Fig. 5. Sleep transistor or a set of sleep transistors used in a conventional power-gating structure.

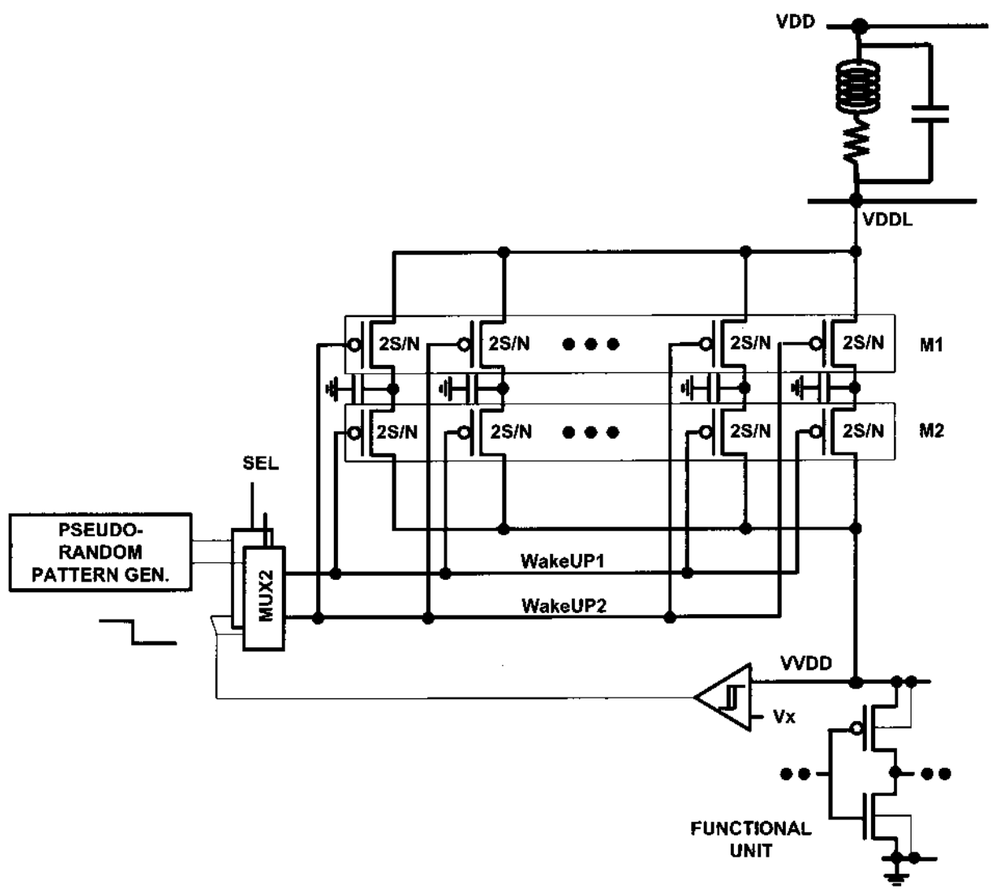

Fig. 6. Initially, a proportion of the sleep transistors is switched on in a pseudo-random manner and then they are all turned on completely when VVDD is above V_x.

in the on-chip power distribution network.

Our approach is to control the amount of charge trapped in the internal parasitic capacitive loads precisely by means of the charge-sharing effect, as shown in Fig. 6. Two PMOS sleep transistors (M1 and M2) are stacked between VDD and VVDD, with a metal-to-metal capacitor (CM2M) between them. To reduce the ground-bounce noise, either M1 or M2 is turned on and off by pseudorandom pulses, while the presence of CM2M allows us digitally to control the amount of charge supplied to the logic during the change from sleep to active modes. In detail, a charge passes from VDD to the metal-to-metal capacitor CM2M via M1 and then to VVDD via M2. By repeating this process, VVDD eventually reaches the level of V_x. At this stage, both M1 and M2 are completely turned on, connecting VVDD to VDD and reducing the turn-on time with minimal ground-bouce noise.

IV. Test Circuitry and Experimental Results

To assess the effectiveness of our power-gating turn-on mechanism in 65nm CMOS bulk LP (Low-Power) technology, we designed the test circuitry shown in Fig. 7. It consists of a 16-bit arithmetic and logic unit (ALU) and 28 power gating cells (PGs). Each power-gating cell includes two stacked PMOS sleep transistors (M1 and M2) with a metal-to-metal capacitor (CM2M), the NMOS data-retention device (M3), and a PMOS charge pumping device (M4).

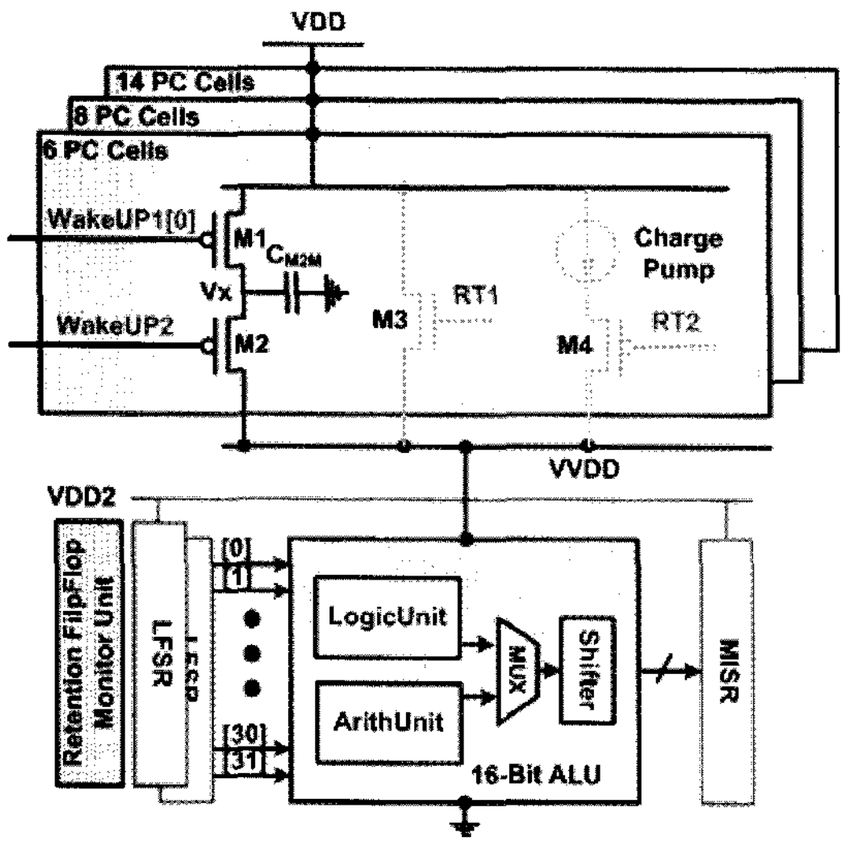

Fig. 7. Block diagram of the test chip designed to evaluate our power gating structure [9].

The ALU is powered by the virtual VDD (VVDD) grid through a sleep transistor, which is sized at less than 5% of the IR drop, so as to minimize the sacrifice in maximum operating frequency. The ALU includes add and subtract units, a shifter and a logic unit. Its critical path is through a 16-bit adder with data inputs supplied by two 16-bit linear-feedback shift registers (LFSRs) that generate pseudo-random patterns. Results are transferred to a multiple-input signature register (MISR).

Unlike a conventional abrupt wake-up, our switched-resistor turns on and off at pseudo-random, and then turns fully on when the VVDD is above a certain reference voltage. This reduces the instantaneous peak current by 27% as well as the turn-on time required for the VVDD to be stabilized.

V. Conclusions

We have studied the ground bounce caused by large charge currents through a sleep transistor during the mode transition of a power-gating structure. A new power-gating turn-on mechanism has been proposed to reduce the magnitude of voltage glitches in the power distribution network, as well as the time required for the network to stabilize.

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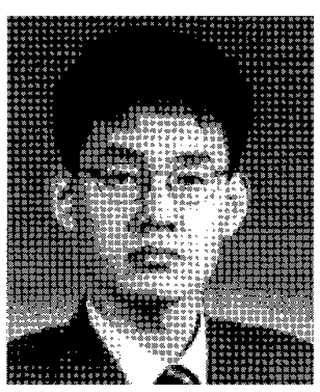

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